LAN9352

2-Port 10/100 Managed Ethernet Switch with 8/16-Bit Non-PCI CPU Interface

Highlights

- High performance 2-port switch with VLAN, QoS packet prioritization, rate limiting, IGMP monitoring and management functions
- Interfaces to most 8/16-bit embedded controllers and 32-bit embedded controllers with an 8/16-bit bus
- Integrated Ethernet PHYs with HP Auto-MDIX
- Compliant with Energy Efficient Ethernet 802.3az
- Wake on LAN (WoL) support
- Integrated IEEE 1588v2 hardware time stamp unit
- Cable diagnostic support
- 1.8V to 3.3V variable voltage I/O
- Integrated 1.2V regulator for single 3.3V operation

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions & video recorders
- VoIP/Video phone systems, home gateways
- Test/Measurement equipment, industrial automation

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM, 512 entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1D spanning tree protocol support
  - 4 separate transmit queues available per port
  - Fixed or weighted egress priority servicing
  - QoS/CoS Packet prioritization
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable Traffic Class map based on input priority on per port basis
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress with coloring and random early discard, per port / priority
    - Programmable rate limiting at the egress with leaky bucket algorithm, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable broadcast storm protection with global % control and enable per port
  - Programmable buffer usage limits
  - Dynamic queues on internal memory
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any port or port pair
  - Fully compliant statistics (MIB) gathering counters
- Ports
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - 100BASE-FX support via external fiber transceiver
  - Full and half duplex support, full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - Programmable interframe gap, flow control pause value
  - Auto-negotiation, polarity correction & MDI/MDI-X
- Host Bus Interface
  - Indexed register or multiplexed bus
  - SPI / Quad SPI support
- IEEE 1588v2 hardware time stamp unit
  - Global 64-bit tunable clock
  - Boundary clock: master / slave, one-step / two-step, end-to-end / peer-to-peer delay
  - Transparent Clock with Ordinary Clock: master / slave, one-step / two-step, end-to-end / peer-to-peer delay
  - Fully programmable timestamp on TX or RX, timestamp on GPIO
  - 64-bit timer comparator event generation (GPIO or IRQ)
- Comprehensive power management features
  - 3 power-down levels
  - Wake on link status change (energy detect)
  - Magic packet wakeup, Wake on LAN (WoL), wake on broadcast, wake on perfect DA
  - Wakeup indicator event signal
- Power and I/O
  - Integrated power-on reset circuit
  - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
  - JEDEC Class 3A ESD performance
  - Single 3.3V power supply (integrated 1.2V regulator)
- Additional Features
  - Multifunction GPIOs
  - Ability to use low cost 25MHz crystal for reduced BOM
- Packaging
  - RoHS compliant 72-pin QFN or 80-pin XVTQFP
- Available in extended commercial, industrial, and extended industrial temp. ranges

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GENERAL DESCRIPTION

The LAN9352 is a full featured, 2 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9352 combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers, and host bus interface. IEEE 1588v2 is supported via the integrated IEEE 1588v2 hardware time stamp unit, which supports end-to-end and peer-to-peer transparent clocks. The LAN9352 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) (100Mbps only), and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications. 100BASE-FX is supported via an external fiber transceiver.

At the core of the device is the high performance, high efficiency 3 port Ethernet Switch Fabric. The Switch Fabric contains a 3 port VLAN layer 2 Switch Engine that supports untagged, VLAN tagged, and priority tagged frames. The Switch Fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 512 entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block within the Switch Fabric. All aspects of the Switch Fabric are managed via the Switch Fabric configuration and status registers, which are indirectly accessible via the system control and status registers.

The LAN9352 provides 2 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9352 provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the Host MAC are used to connect the LAN9352 switch fabric to the host bus interface. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. Automatic 32-bit CRC generation/checking and automatic payload padding are supported to further reduce CPU overhead. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while decreasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the device.

Two user selectable host bus interface options are available:

- ***Indexed register access***
  This implementation provides three index/data register banks, each with independent Byte/WORD to DWORD conversion. Internal registers are accessed by first writing one of the three index registers, followed by reading or writing the corresponding data register. Three index/data register banks support up to 3 independent driver threads without access conflicts. Each thread can write its assigned index register without the issue of another thread overwriting it. Two 16-bit cycles or four 8-bit cycles are required within the same 32-bit index/data register - however, these access can be interleaved. Direct (non-indexed) read and write accesses are supported to the packet data FIFOs. The direct FIFO access provides independent Byte/WORD to DWORD conversion, supporting interleaved accesses with the index/data registers. Direct FIFO access also supports burst reading of the data FIFO.
- ***Multiplexed address/data bus***
  This implementation provides a multiplexed address and data bus with both single phase and dual phase address support. The address is loaded with an address strobe followed by data access using a read or write strobe. Two back to back 16-bit data cycles or 4 back to back 8-bit data cycles are required within the same 32-bit DWORD. These accesses must be sequential without any interleaved accesses to other registers. Burst read and write accesses are supported to the packet data and status FIFOs by performing one address cycle followed by multiple read or write data cycles.

The HBI supports 8/16-bit operation with big, little, and mixed endian operations. Four separate FIFO mechanisms (TX/RX Data FIFO's, TX/RX Status FIFO's) interface the HBI to the Host MAC and facilitate the transferring of packet data and status information between the host CPU and the switch fabric. A configurable host interrupt pin allows the device to inform the host CPU of any internal interrupts.

An SPI / Quad SPI slave controller provides a low pin count synchronous slave interface that facilitates communication between the device and a host system. The SPI / Quad SPI slave allows access to the System CSRs, internal FIFOs and memories. It supports single and multiple register read and write commands with incrementing, decrementing and static addressing. Single, Dual and Quad bit lanes are supported with a clock rate of up to 80 MHz.

The LAN9352 supports numerous power management and wakeup features. The LAN9352 can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including “Magic Packet”, “Wake on LAN”, wake on broadcast, wake on perfect DA, and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command or one of the wake events.

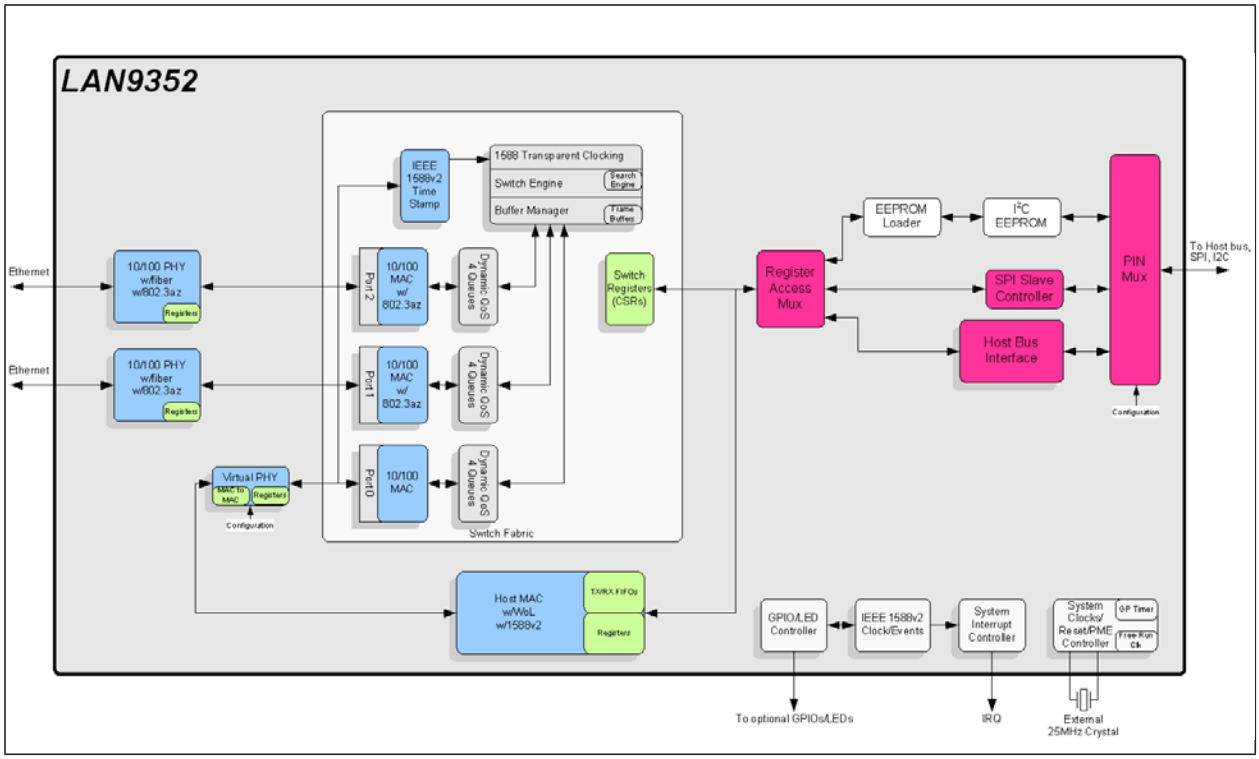
The LAN9352 contains an I^2C master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the device at reset.

In addition to the primary functionality described above, the LAN9352 provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, a configurable GPIO/LED interface, and IEEE 1588 time stamping on all ports and all GPIOs. The IEEE time stamp unit provides a 64-bit tunable clock for accurate PTP timing and a timer comparator to allow time based interrupt generation.

The LAN9352 can be configured to operate via a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN9352 is available in extended commercial, industrial, and extended industrial temperature ranges. Figure 1 provides an internal block diagram of the LAN9352.

FIGURE 1: INTERNAL BLOCK DIAGRAM



PACKAGE OUTLINES

72-QFN

FIGURE 2: 72-QFN PACKAGE

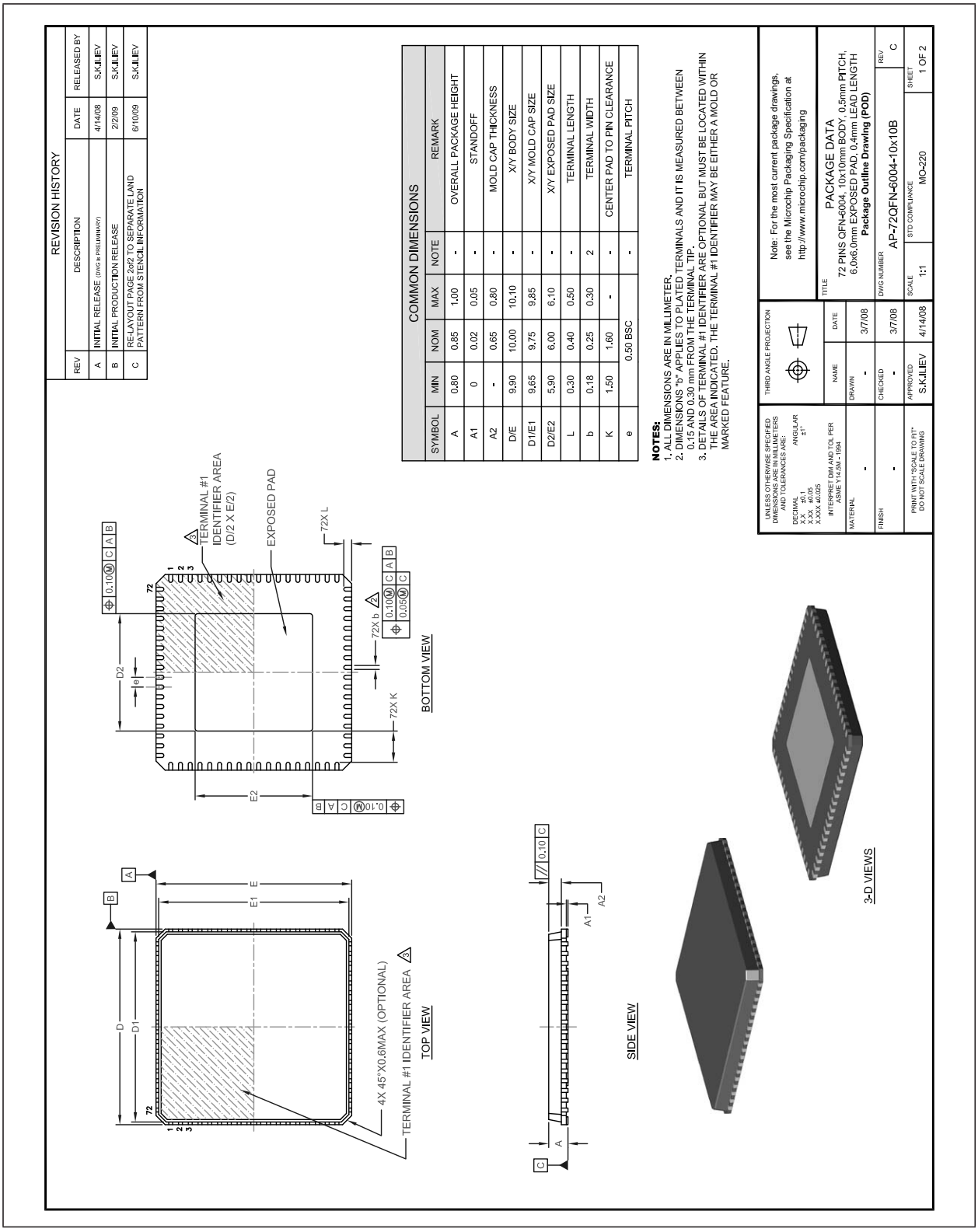
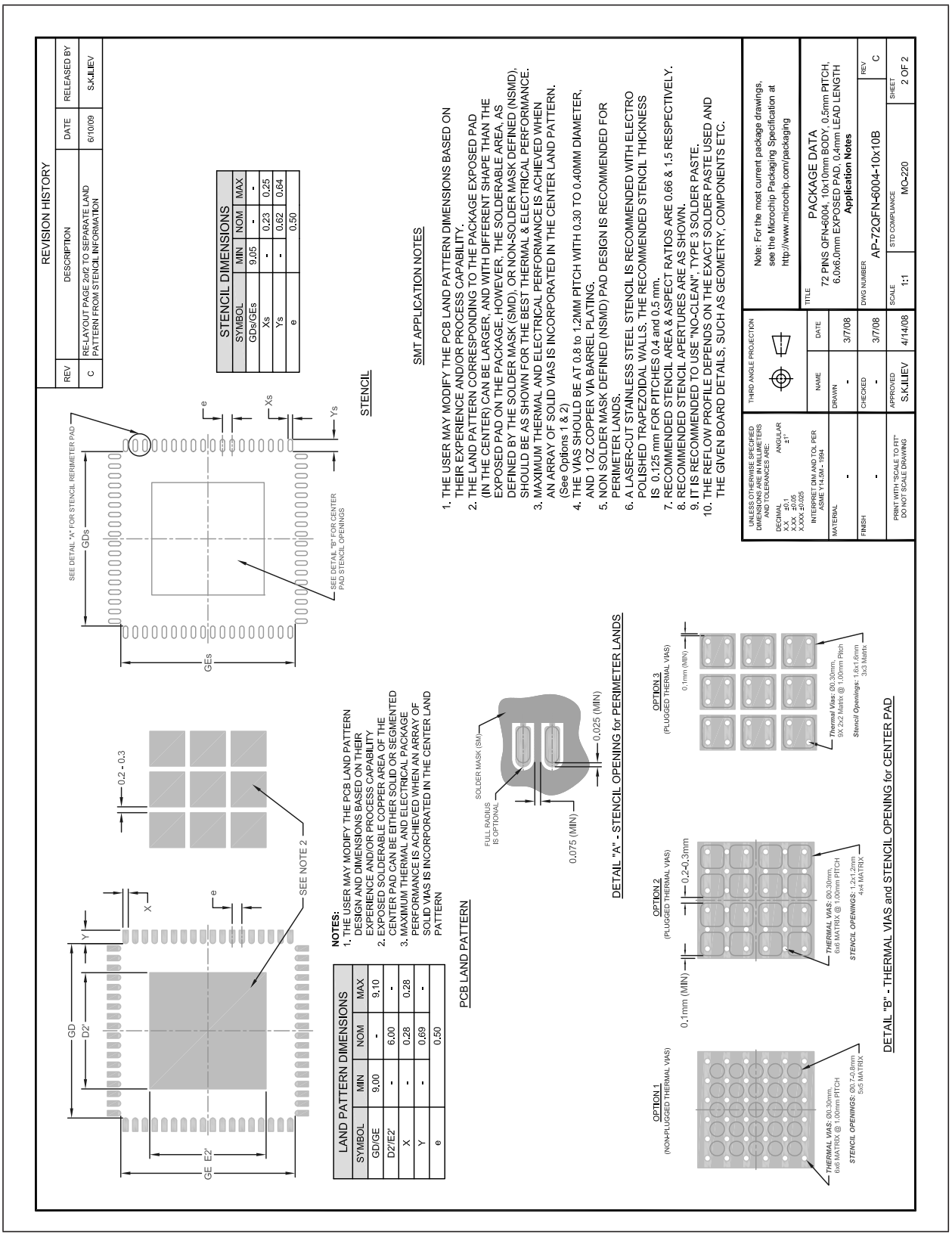


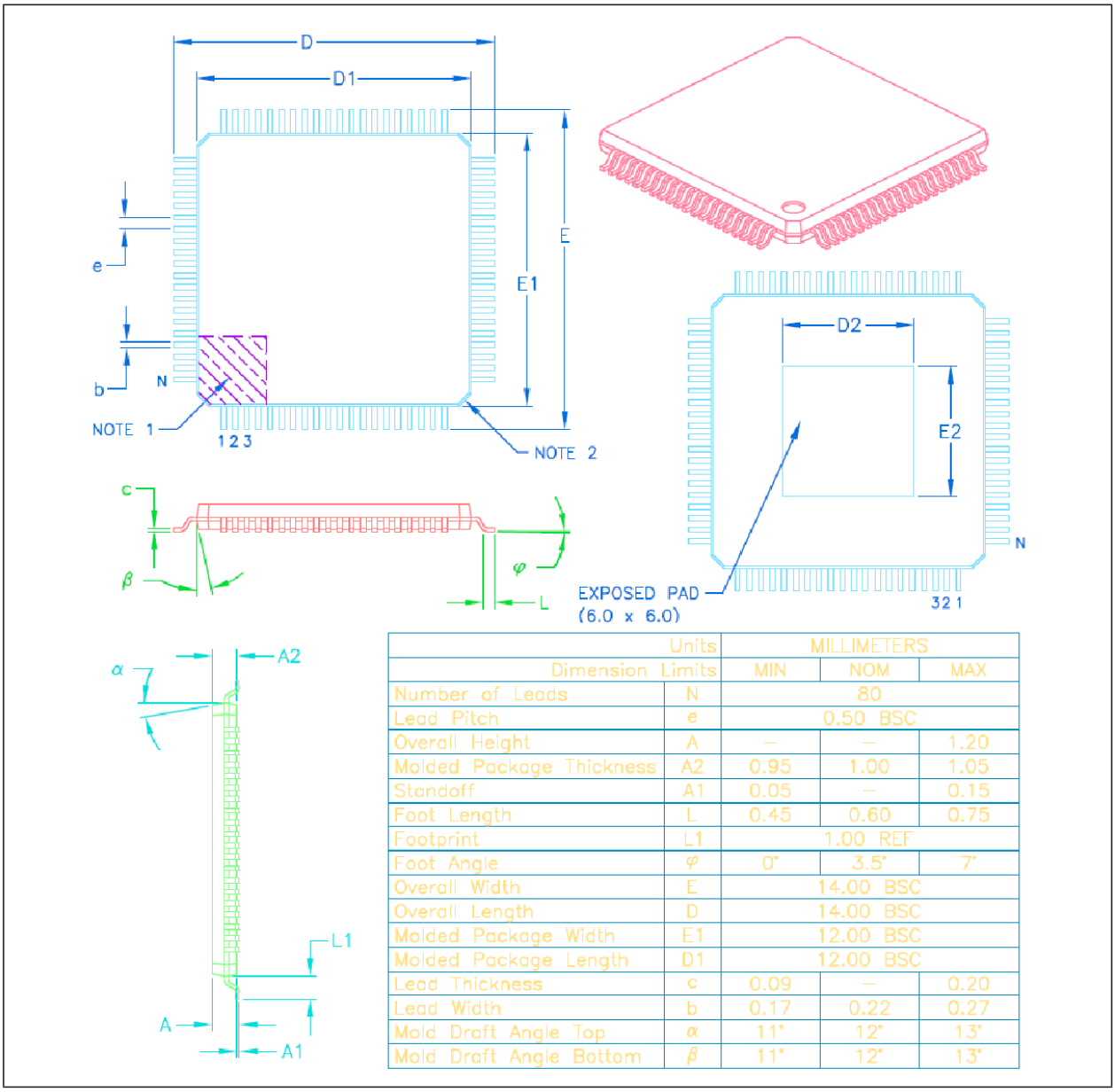
FIGURE 2: 72-QFN PACKAGE (CONTINUED)



Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

80-XVTQFP

FIGURE 3: 80-XVTQFP PACKAGE



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Note 1: Pin 1 visual index feature may vary, but will be located within the hatched area.

2: Chamfers at corners are optional; size may vary.

3: Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

4: Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
REV A (04-01-14)	Document Release	

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PART NO.	[X]	[X]	/	XX
Device	Tape and Reel Option	Temperature Range		Package

Device:	LAN9352	
Tape and Reel Option:	Blank = Standard packaging (tray) T = Tape and Reel (Note 1)	
Temperature Range:	Blank = 0°C to +85°C I = -40°C to +85°C V = -40°C to +105°C	(Extended Commercial) (Industrial) (Extended Industrial) (Note 2)
Package:	ML = 72-pin QFN PT = 80-pin XVTQFP	

Examples:

a) LAN9352/ML
Standard Packaging (Tray),
Extended Commercial Temperature,
72-pin QFN

b) LAN9352TI/PT
Tape and Reel
Industrial Temperature,
80-pin XVTQFP

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Extended industrial temp. support (105°C) in the 72-QFN only

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