1-Kbit I²C Serial EEPROM with Unique 128-Bit Serial Number, Automotive Grade

AT24CS01

Features

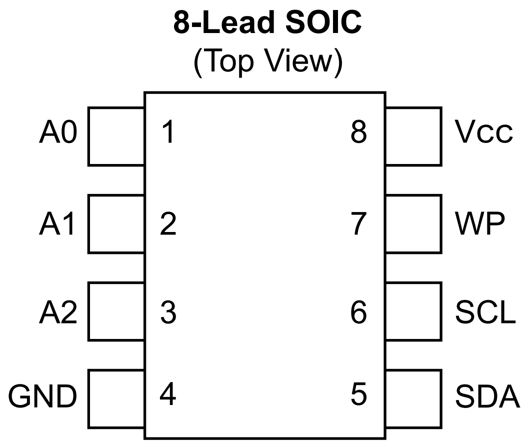
- Medium-Voltage Operation:
  - Grade 1, V_{CC} = 2.5V to 5.5V
- Internally Organized as 128 x 8 (1K)
- 128-Bit Unique Factory-Programmed Serial Number
  - Permanent read-only value
  - Unique across entire CS Series of Serial EEPROMs
- Extended Temperature Range:
  - Grade 1 temperature range: -40°C to +125°C
- I^2C-Compatible (Two-Wire) Serial Interface:
  - 100 kHz Standard Mode, 2.5V to 5.5V
  - 400 kHz Fast Mode, 2.5V to 5.5V
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Write-Protect Pin for Full Array Hardware Data Protection
- Ultra-Low Active Current (3 mA maximum) and Standby Current (6 µA maximum)
- 8-Byte Page Write Mode:
  - Partial page writes allowed
- Random and Sequential Read Modes
- Self-Timed Write Cycle within 5 ms Maximum
- ESD Protection > 4,000V
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- RoHS compliant
- AEC-Q100 Automotive Qualified

Package

- 8-Lead SOIC

Table of Contents

1. Package Types (not to scale)



2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	8-Lead SOIC	Function
A0[(1)]	1	Device Address Input
A1[(1)]	2	Device Address Input
A2[(1)]	3	Device Address Input
GND	4	Ground
SDA	5	Serial Data
SCL	6	Serial Clock
WP[(1)]	7	Write-Protect
V_{CC}	8	Device Power Supply

Note:

1. If the A0, A1, A2 or WP pins are not driven, they are internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Microchip recommends connecting these pins to a known state whenever possible.

2.1 Device Address Inputs (A0, A1, A2)

The A0, A1 and A2 pins are device address inputs that are hardwired (directly to GND or to V_{CC}) for compatibility with other two-wire Serial EEPROM devices. When the pins are hardwired, as many as eight devices may be addressed on a single bus system. A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A0, A1 and A2 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, Microchip recommends always connecting the address pins to a known state. When using a pull-up resistor, Microchip recommends using 10 kΩ or less.

2.2 Ground

The ground reference for the power supply. GND should be connected to the system ground.

2.3 Serial Data (SDA)

The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled high using an external pull-up resistor (not to exceed 10 kΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

2.4 Serial Clock (SCL)

The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin are always latched in on the rising edge of SCL, while output data on the SDA pin are clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled high using an external pull-up resistor.

2.5 Write-Protect (WP)

The write-protect input, when connected to GND, allows normal write operations. When the WP pin is connected directly to V_{CC}, all write operations to the protected memory are inhibited.

If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, connecting the WP pin to a known state is recommended. When using a pull-up resistor, using 10 kΩ or less is recommended.

Table 2-2. Write-Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Full Array
At GND	Normal Write Operations

2.6 Device Power Supply (V_{CC})

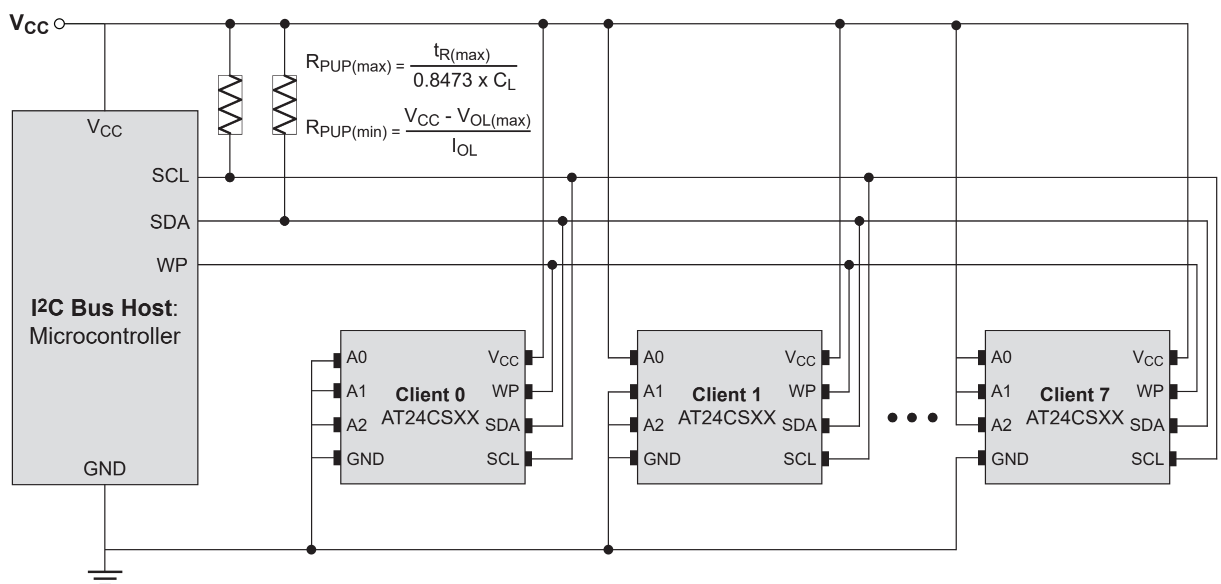
The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

3. Description

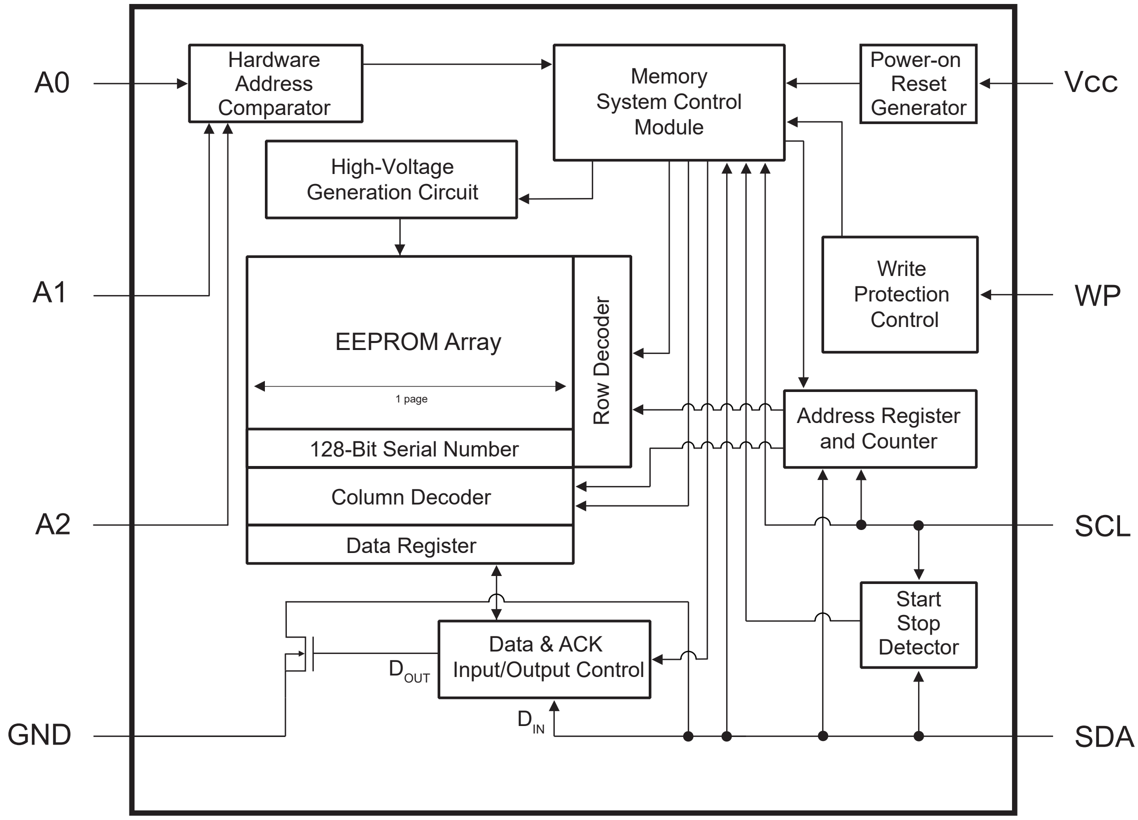
The AT24CS01 provides 1,024 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 128 words of 8 bits each. The device's cascading feature allows up to eight devices to share a common two-wire bus. This device is optimized for use in many automotive applications where low-power and low-voltage operations are essential. The device is available in the space-saving 8-lead SOIC package, which will operate from 2.5V to 5.5V.

The AT24CS01 provides the additional feature of a factory-programmed, ensured unique 128-bit serial number while maintaining all of the traditional features available in the 1-Kbit Serial EEPROM. The time-consuming step of performing and ensuring true serialization of product on a manufacturing line can be removed from the production flow by employing the CS Series Serial EEPROM. The 128-bit serial number is programmed and permanently locked from future writing during the Microchip production process. Further, this 128-bit location does not consume any of the user read/write area of the 1-Kbit Serial EEPROM. The uniqueness of the serial number is ensured across the entire CS Series of Serial EEPROMs, regardless of the size of the memory array or the type of interface protocol. This means that as an application's needs for memory size or interface protocol evolve in future generations, any previously deployed serial number from any Microchip CS Series Serial EEPROM part will remain valid.

3.1 System Configuration Using Two-Wire Serial EEPROMs



3.2 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
V_{CC}	6.25V
Voltage on any pin with respect to ground	-1.0V to +7.0V
DC output current	5.0 mA
ESD protection	>4 kV

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT24CS01	Automotive Grade 1
Operating Temperature (Case)	-40°C to +125°C
V_{CC} Power Supply	2.5V to 5.5V

4.3 DC Characteristics

Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Maximum	Units	Test Conditions
Supply Voltage	V_{CC}	2.5	5.5	V	
Supply Current	I_{CC1}	—	1.0	mA	V_{CC} = 5.0V, Read at 400 kHz
Supply Current	I_{CC2}	—	3.0	mA	V_{CC} = 5.0V, Write at 400 kHz
Standby Current	I_{SB}	—	6.0	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND
Input Leakage Current	I_{LI}	—	3.0	µA	V_{IN} = V_{CC} or GND
Output Leakage Current	I_{LO}	—	3.0	µA	V_{OUT} = V_{CC} or GND
Input Low Level	V_{IL}	-0.6	V_{CC} x 0.3	V	Note 1
Input High Level	V_{IH}	V_{CC} x 0.7	V_{CC} + 0.5	V	Note 1
Output Low Level	V_{OL}	—	0.4	V	V_{CC} = 3.0V, I_{OL} = 2.1 mA

Note:

1. This parameter is characterized but is not 100% tested in production.

4.4 AC Characteristics

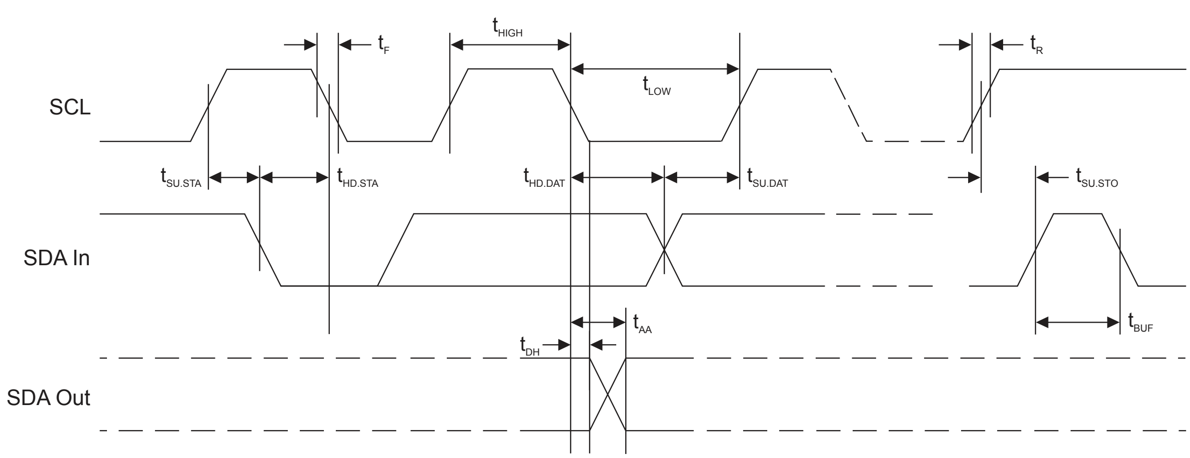
Table 4-3. AC Characteristics[1]

Parameter	Symbol	Min.	Max.	Units
Clock Frequency, SCL	f_{SCL}	—	400	kHz
Clock Pulse Width Low	t_{LOW}	1,200	—	ns
Clock Pulse Width High	t_{HIGH}	600	—	ns
Input Filter Spike Suppression	t_I	—	50	ns
Clock Low to Data Out Valid	t_{AA}	100	900	ns
Bus Free Time between Stop and Start	t_{BUF}	1,200	—	ns
Start Hold Time	$t_{HD.STA}$	600	—	ns
Start Set-Up Time	$t_{SU.STA}$	600	—	ns
Data In Hold Time	$t_{HD.DAT}$	0	—	ns
Data In Set-up Time	$t_{SU.DAT}$	100	—	ns
Inputs Rise Time[2]	t_R	—	300	ns
Inputs Fall Time[2]	t_F	—	300	ns
Stop Set-Up Time	$t_{SU.STO}$	600	—	ns
Data Out Hold Time	t_{DH}	50	—	ns
Write Cycle Time	t_{WR}	—	5	ms

Notes:

1. AC measurement conditions:
   - C_L: 100 pF
   - R_{PUP} (SDA bus line pull-up resistor to V_{CC}): 1.3 kΩ (400 kHz)
   - Input pulse voltages: 0.3 x V_{CC} to 0.7 x V_{CC}
   - Input rise and fall times: ≤50 ns
   - Input and output timing reference voltages: 0.5 x V_{CC}
2. These parameters are determined through product characterization and are not 100% tested in production.

Figure 4-1. Bus Timing



4.5 Electrical Specifications

4.5.1 Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT24CS01 should monotonically rise from GND to the minimum V_{CC} level, as specified in Table 4-1, with a slew rate no faster than 0.1 V/µs.

4.5.1.1 Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT24CS01 includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus host must wait at least t_{PUP} before sending the first command to the device. See Table 4-4 for the values associated with these power-up parameters.

Table 4-4. Power-up Conditions[1]

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands	100	—	μs
V_{POR}	Power-on Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	500	—	ms

Note:

1. These parameters are characterized but are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT24CS01 drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed. First, drive the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time, and then perform a new power-up sequence in compliance with the requirements defined in this section.

4.5.2 Pin Capacitance

Table 4-5. Pin Capacitance[1]

Symbol	Test Condition	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A0, A1, A2 and SCL)	6	pF	V_{IN} = 0V

Note:

1. This parameter is characterized but is not 100% tested in production.

4.5.3 EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance[1]	T_A = +25°C, V_{CC} = 5.0V, Page Write mode	1,000,000	—	Write Cycles
Data Retention[1]	T_A = +55°C	100	—	Years

Note:

1. Performance is determined through characterization and the qualification process.

5. Device Operation and Communication

The AT24CS01 operates as a client device and utilizes a simple I^2C-compatible Two-Wire digital serial interface to communicate with a host controller, commonly referred to as the bus host. The host initiates and controls all read and write operations to the client devices on the serial bus, and both the host and the client devices can transmit and receive data on the bus.

The serial interface consists of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the host, while the bidirectional SDA pin is used to receive command and data information from the host as well as to send data back to the host. Data are always latched into the AT24CS01 on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pins incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant bit (MSb) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an Acknowledge (ACK) or a No-Acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the host. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation; thus, there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must change only while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and terminate all serial bus communication between the host and the client devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the host. For the serial bus to be idle, both the SCL and SDA pins must be in the logic high state simultaneously.

5.1 Clock and Data Transition Requirements

The SDA pin is an open-drain terminal and therefore must be pulled high with an external pull-up resistor. SCL is an input pin that can either be driven high or pulled high using an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below. The relationship of the AC timing parameters with respect to SCL and SDA for the AT24CS01 is shown in the timing waveform in Figure 4-1. The AC timing characteristics and specifications are outlined in AC Characteristics.

5.2 Start and Stop Conditions

5.2.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable logic '1' state and will bring the device out of Standby mode. The host uses a Start condition to initiate any data transfer sequence; therefore, every command must begin with a Start condition. The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Refer to Figure 5-1 for more details.

5.2.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic '1' state.

The host can use the Stop condition to end a data transfer sequence with the AT24CS01, which will subsequently return to Standby mode. The host can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the host will perform another operation. Refer to Figure 5-1 for more details.

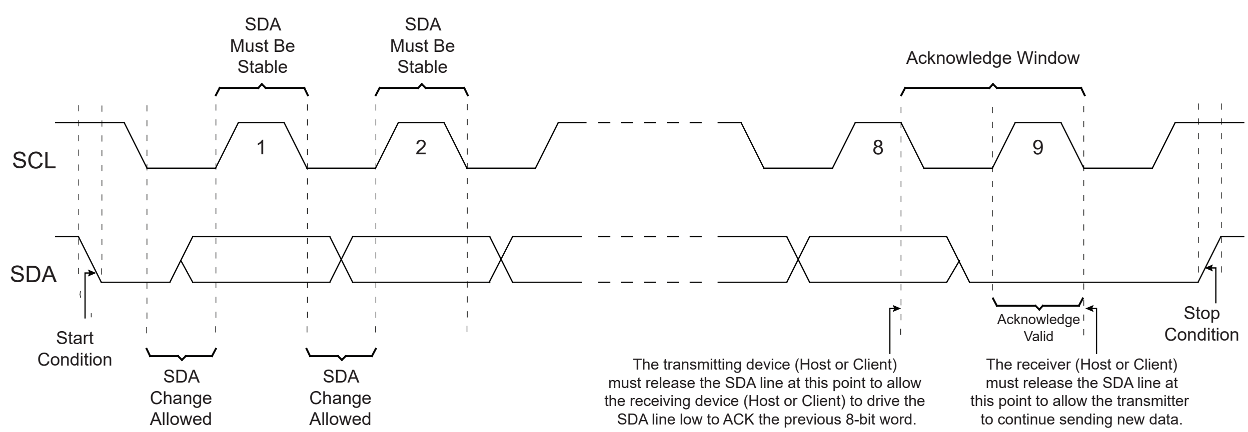
5.3 Acknowledge and No-Acknowledge

After each byte of data is received, the receiving device must confirm with the transmitting device that it has successfully received the data byte by responding with what is known as an Acknowledge (ACK). An ACK occurs when the transmitting device first releases the SDA line at the falling edge of the eighth clock cycle, followed by the receiving device responding with a logic '0' throughout the ninth clock cycle's high period.

When the AT24CS01 is transmitting data to the host, the host can indicate that it has finished receiving data and wants to end the operation by sending a logic '1' response to the AT24CS01 instead of an ACK response during the ninth clock cycle. This is known as a No-Acknowledge (NACK) and is accomplished when the host sends a logic '1' during the ninth clock cycle, at which point the AT24CS01 will release the SDA line so the host can then generate a Stop condition.

The transmitting device, which can be either the bus host or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a logic '0' to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram is provided in Figure 5-1 to better illustrate these requirements.

Figure 5-1. Start Condition, Data Transitions, Stop Condition and Acknowledge



5.4 Standby Mode

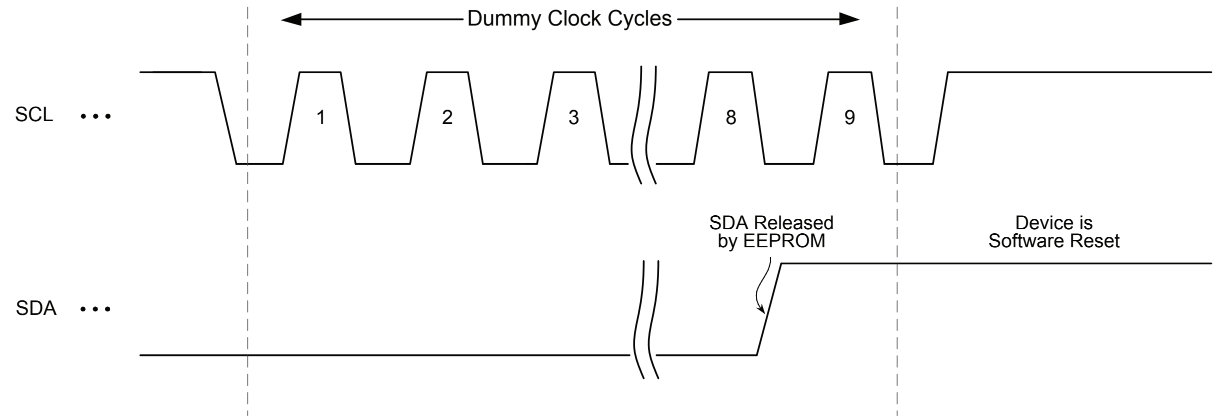
The AT24CS01 features a low-power Standby mode that is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see Power-Up Requirements and Reset Behavior).
- A Stop condition is received by the device unless it initiates an internal write cycle (see Write Operations).
- At the completion of an internal write cycle (see Write Operations).

5.5 Software Reset

After an interruption in protocol, power loss or system Reset, any two-wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The software Reset sequence should not take more than nine dummy clock cycles. Once the software Reset sequence is complete, new protocol can be sent to the device by sending a Start condition followed by the protocol. Refer to Figure 5-2 for an illustration.

Figure 5-2. Software Reset



In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see Power-Up Requirements and Reset Behavior).

6. Memory Organization

The AT24CS01 is internally organized as 16 pages of 8 bytes each.

6.1 Device Addressing

Accessing the device requires an 8-bit device address byte following a Start condition to enable the device for a read or write operation. Since multiple client devices can reside on the serial bus, each client device must have its own unique address so the host can access each device independently.

The Most Significant four bits of the device address byte are referred to as the device type identifier. The device type identifier '1010' (Ah) is required in bits 7 through 4 of the device address byte (see Table 6-1).

The AT24CS01 utilizes a separate memory block containing a factory-programmed 128-bit serial number. Access to this memory location is similar to the EERPOM region with the exception that the device type identifier is set to '1011' (Bh) in bits 7 through 4 of the device address byte (see Table 6-1).

Following the 4-bit device type identifier are the hardware client address bits, A2, A1 and A0. These bits can be used to expand the address space by allowing up to eight Serial EEPROM devices on the same bus. These hardware client address bits must correlate with the voltage level on the corresponding hardwired device address input pins A0, A1 and A2. The A0, A1 and A2 pins use an internal proprietary circuit that automatically biases the pin to a logic '0' state if the pin is allowed to float. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once the pin is biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Microchip recommends connecting the A0, A1 and A2 pins to a known state whenever possible.

When using the SOT23 package, the A2, A1 and A0 pins are not accessible and are left floating. The previously mentioned automatic pull-down circuit will set these pins to a logic '0' state. As a result, to properly communicate with the device in the SOT23 package, the A2, A1 and A0 software bits must always be set to logic '0' for any operation. Refer to Table 6-1 to review these bit positions.

The eighth bit (bit 0) of the device address byte is the Read/Write Select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon the successful comparison of the device address byte, the AT24CS01 will return an ACK. If a valid comparison is not made, the device will NACK.

Table 6-1. Device Address Byte

Access Area	Device Type Identifier				Hardware Client Address Bits			R/$\overline{W}$ Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Serial Number	1	0	1	1	A2	A1	A0	R/$\overline{W}$

For all operations except the current address read, a word address byte must be transmitted to the device immediately following the device address byte. The word address byte contains a 7-bit memory array word address and is used to specify which byte location in the EEPROM to start reading or writing. Refer to Table 6-2 to review these bit positions.

Table 6-2. Word Address Byte

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	X	A6	A5	A4	A3	A2	A1	A0
Serial Number	1	0	x	x	x	x	x	x

7. Write Operations

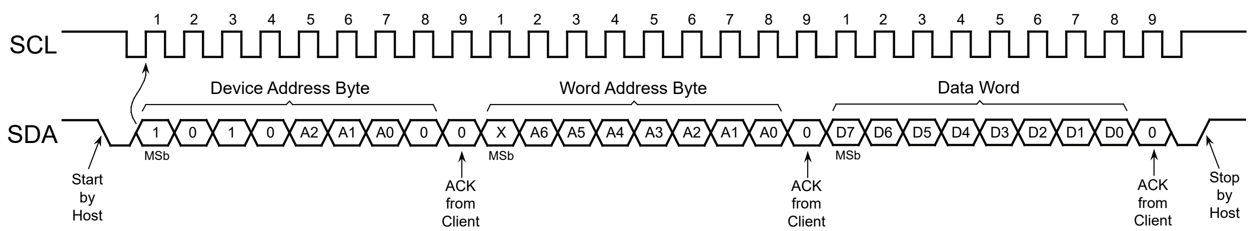
All write operations for the AT24CS01 begin with the host sending a Start condition, followed by a device address byte with the R/$\overline{W}$ bit set to logic '0', and then by the word address byte. The data value(s) to be written to the device immediately follow the word address byte.

7.1 Byte Write

The AT24CS01 supports the writing of a single 8-bit byte. Selecting a data word in the AT24CS01 requires a 7-bit word address.

Upon receipt of the proper device address and the word address bytes, the EEPROM will send an Acknowledge. The device will then be ready to receive the 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will respond with an ACK. The addressing device, such as a bus host, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle, which will be completed within t_{WR}, while the data word is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete.

Figure 7-1. Byte Write



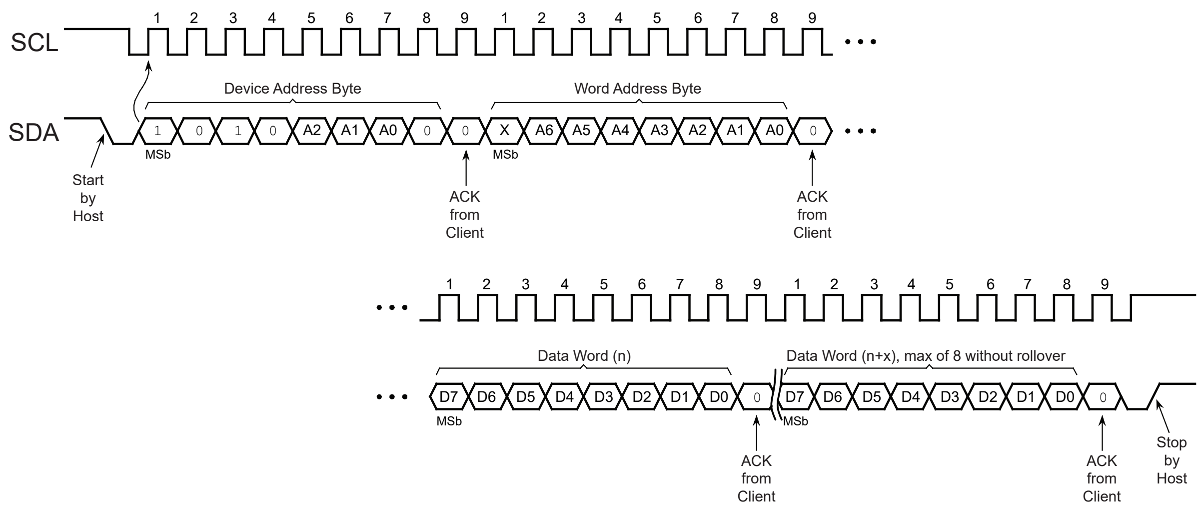
7.2 Page Write

A page write operation allows up to 8 bytes to be written in the same write cycle, provided that all bytes are in the same row of the memory array (where address bits A6 to A3 are the same). Partial page writes of fewer than 8 bytes are also allowed.

A page write is initiated the same way as a byte write, but the bus host does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the bus host can transmit up to seven additional data words. The EEPROM will respond with an ACK after each data word is received. Once all data to be written have been sent to the device, the bus host must issue a Stop condition (see Figure 7-2), at which time the internally self-timed write cycle will begin.

The lower three bits of the word address are internally incremented following the receipt of each data word. The higher-order address bits are not incremented and retain the memory page row location. Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. When the incremented word address reaches the page boundary, the address counter will roll over to the beginning of the same page. Nevertheless, creating a rollover event should be avoided as previously loaded data in the page could become unintentionally altered.

Figure 7-2. Page Write

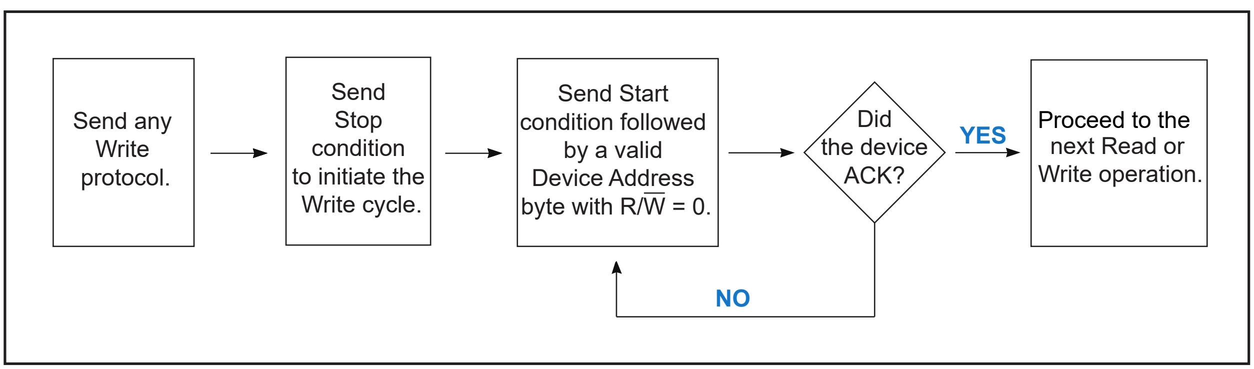


7.3 Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time-sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}). This method allows the application to immediately know when the Serial EEPROM write cycle has completed so a subsequent operation can be started.

Once the internally self-timed write cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '0'. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write cycle has completed, the EEPROM will respond with an ACK, allowing a new read or write operation to be immediately initiated. A flowchart has been included in Figure 7-3 to better illustrate this technique.

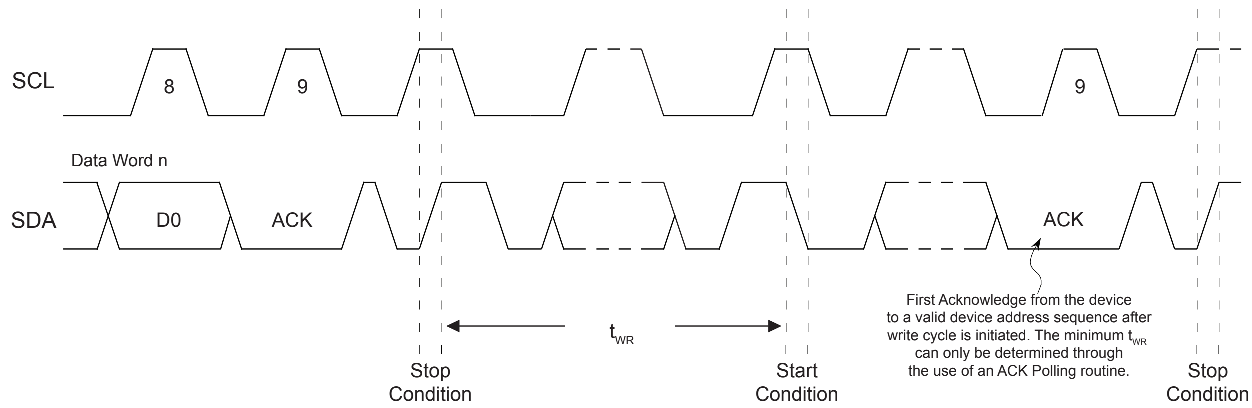
Figure 7-3. Acknowledge Polling Flowchart



7.4 Write Cycle Timing

The length of the self-timed write cycle (t_{WR}) is defined as the amount of time from the Stop condition, which begins the internal write cycle, to the Start condition of the first device address byte sent to the AT24CS01, to which it subsequently responds with an ACK. Figure 7-4 shows this measurement. During the internally self-timed write cycle, any attempts to read from or write to the memory array will not be processed.

Figure 7-4. Write Cycle Timing



7.5 Write Protection

The AT24CS01 utilizes a hardware data protection scheme that allows the user to write-protect the entire memory contents when the WP pin is at V_{CC} (or a valid V_{IH}). No write protection will be set if the WP pin is at GND or left floating.

Table 7-1. AT24CS01 Write-Protect Behavior

WP Pin Voltage	Part of the Array Protected
V_{CC}	Full Array
GND	None — Write Protection Not Enabled

The status of the WP pin is sampled at the Stop condition for every byte write or page write operation prior to the start of an internally self-timed write cycle. Changing the WP pin state after the Stop condition has been sent will not alter or interrupt the execution of the write cycle.

If an attempt is made to write to the device while the WP pin has been asserted, the device will acknowledge the device address, word address and data bytes. However, no write cycle will occur when the Stop condition is issued. The device will immediately be ready to accept a new read or write command.

8. Read Operations

Read operations are initiated the same way as write operations, with the exception that the Read/Write Select bit in the device address byte must be a logic '1'. There are four read operations:

- Current Address Read
- Random Read
- Sequential Read
- Serial Number Read

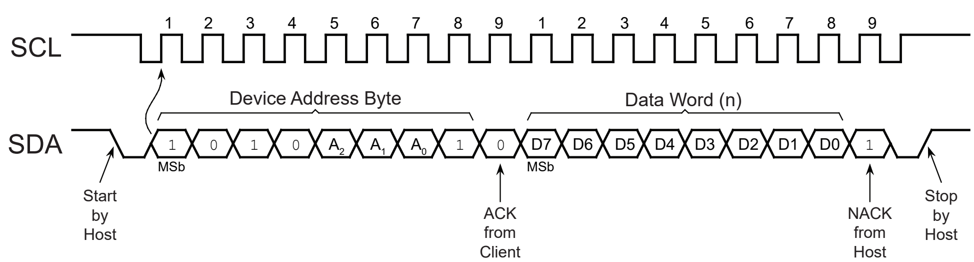
Note: The AT24CS01 contains a single Address Pointer register, which is shared by both the EEPROM and the serial number. As such, when changing from one region to the other, the first read operation in the new region should begin with a dummy write sequence (i.e., a random read operation with the new region's device address and word address bytes) in order to ensure the Address Pointer is set to a known value. See Serial Number Read for additional requirements on the serial number read.

8.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the V_{CC} is maintained to the part. The address rollover during a read is from the last byte of the last page to the first byte of the first page of the memory.

A current address read operation will output data according to the location of the internal data word address counter. This is initiated with a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The device will ACK this sequence and the current address data word is serially clocked out on the SDA line. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

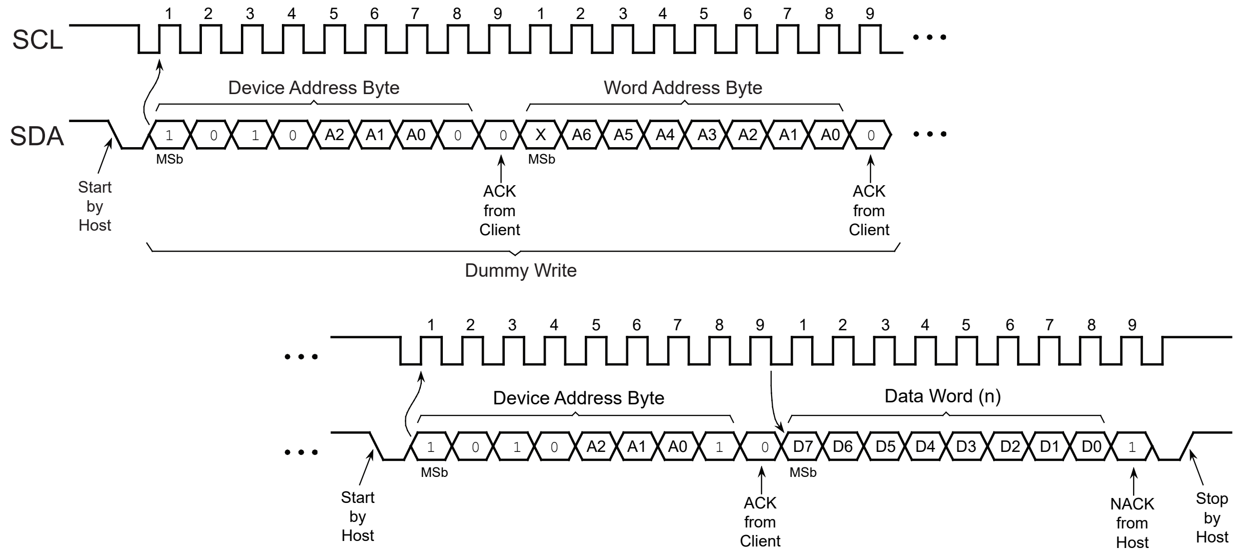
Figure 8-1. Current Address Read



8.2 Random Read

A random read begins in the same way as a byte write operation does to load in a new data word address. This is known as a "dummy write" sequence; however, the data byte and the Stop condition of the byte write must be omitted to prevent the part from entering an internal write cycle. Once the device address and word address are clocked in and acknowledged by the EEPROM, the bus host must generate another Start condition. The bus host now initiates a current address read by sending a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The EEPROM will ACK the device address and serially clock out the data word on the SDA line. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

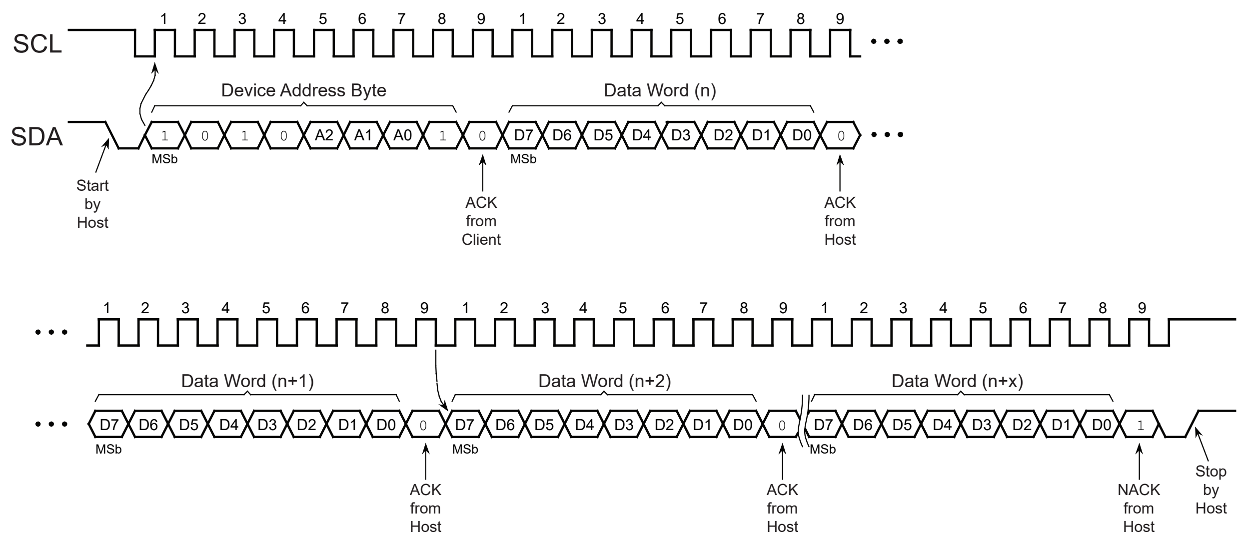
Figure 8-2. Random Read



8.3 Sequential Read

Sequential reads are initiated by either a current address read or a random read. After the bus host receives a data word, it responds with an Acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the word address and serially clock out sequential data words. When the maximum memory address is reached, the data word address will roll over and the sequential read will continue from the beginning of the memory array. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

Figure 8-3. Sequential Read



8.4 Serial Number Read

Reading the serial number is similar to the sequential read sequence but requires use of the specific device Address and word address bytes as specified in Table 6-1 and Table 6-2.

Note: The entire 128-bit value must be read from the starting address of the serial number block to ensure a unique number.

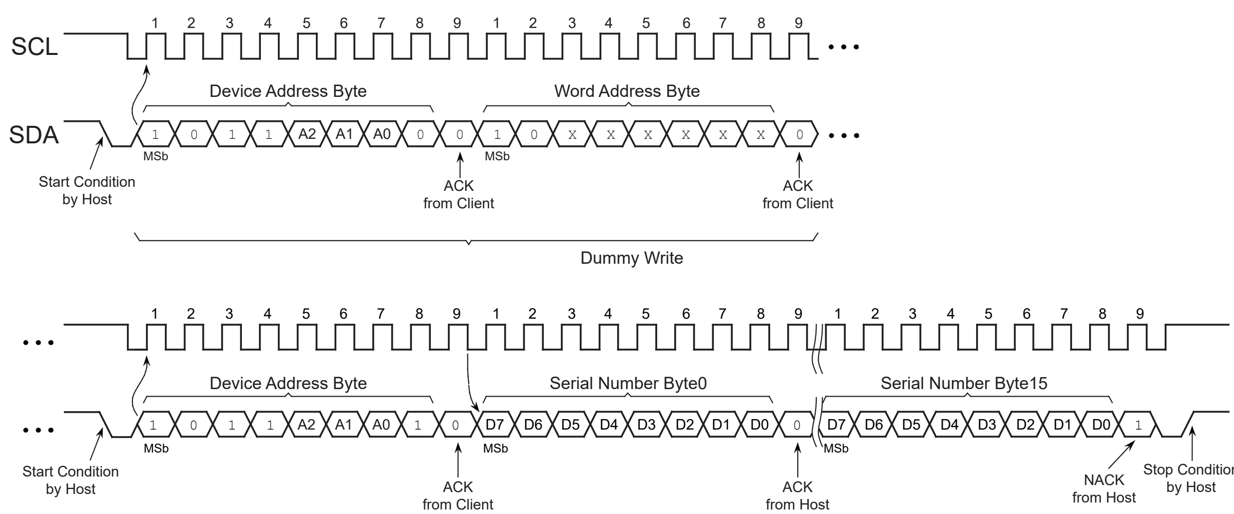
Since the Address Pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a random read or sequential read protocol, should be performed to ensure the Address Pointer is set to a known value. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a '`10`' sequence in bits A7 and A6 of the word address, regardless of the intended address as depicted in Table 6-2. If a word address other than '`10`' is used, then the device will output undefined data.

Note: If the application desires to read the first byte of the serial number, the word address input would need to be 80h.

When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will roll over back to the beginning of the 128-bit serial number. The serial number read operation is terminated when the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence (see Figure 8-4).

Figure 8-4. Serial Number Read



9. Device Default Condition from Microchip

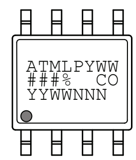
The AT24CS01 is delivered with the EEPROM array set to logic '1', resulting in FFh data in all locations.

10. Packaging Information

10.1 Package Marking Information

AT24CS01: Package Marking Information

8-Lead SOIC



Note 1: ● designates pin 1.
Note 2: Package drawings are not to scale.

Catalog Number Truncation	
AT24CS01	Truncation Code ###: N1

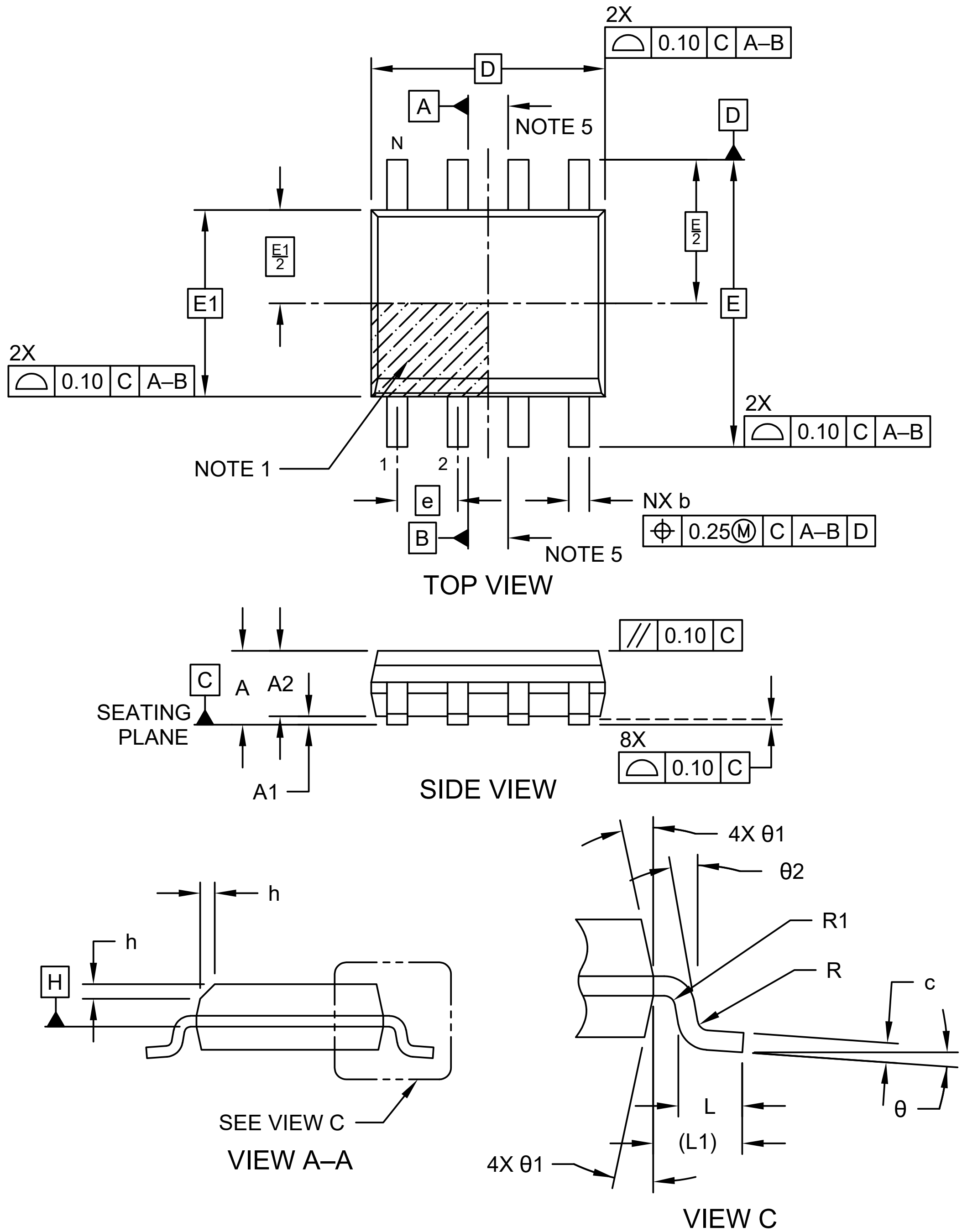
Date Codes	Voltages
Y = Year Code (last digit of calendar year) YY = Year Code (last 2 digits of calendar year) WW = Week code (week of January 1 is week '01')	% = Minimum Voltage D: = 2.5V min

Country of Origin	Device Grade	Atmel Truncation
CO = Country of Origin	P: Automotive Grade 1	AT:Atmel ATM:Atmel ATML:Atmel

Trace Code
NNN = Alphanumeric Trace Code (2 Characters for Small Packages)

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

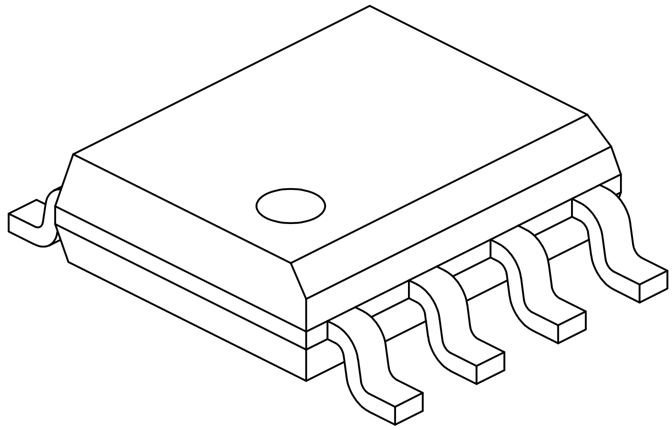
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

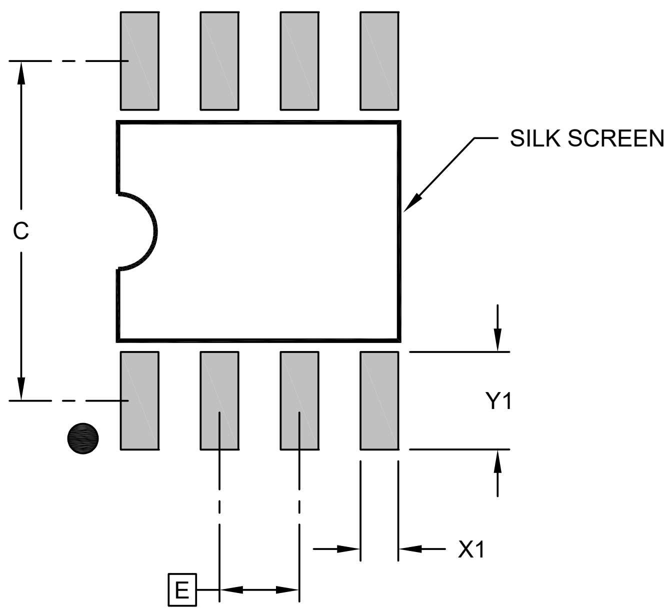
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev K

11. Revision History

Revision A (June 2024)

Initial version of this document.

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

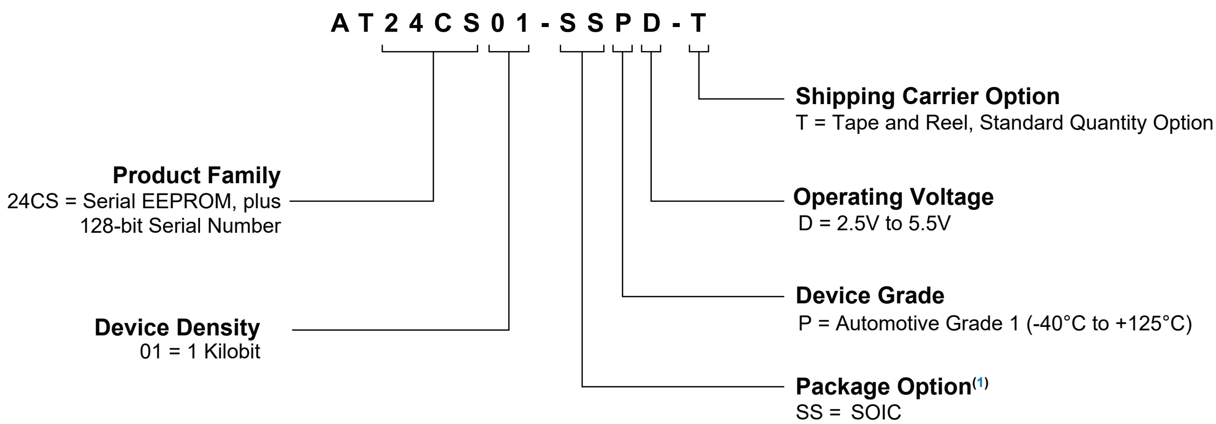
- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Note 1: Contact Microchip for other package options.

Examples

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Automotive Grade
AT24CS01-SSPD-T	SOIC	SN	SS	Tape and Reel	Grade 1 (-40°C to +125°C)

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED

Trademarks

ISBN: 978-1-6683-4507-8

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Hod Hasharon** Tel: 972-9-775-5100 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820