REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		8-21-07
B	Various Pin Name Changes		1-7-08
C	Added EEPROM_SIZE_x Pull-up/Pull-down Details		6-27-08
D	Added MDIO Pull-up Resistor Details		10-22-08

DOCUMENT DESCRIPTION

Schematic Checklist for the LAN9313, 128-pin (X)VTQFP Package

SMSC® SUCCESS BY DESIGN

LANCheck

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Document Number	Revision
SC471209	D

Schematic Checklist for LAN9313

Information Particular for the 128-pin (X)VTQFP Package

LAN9313 (X)VTQFP Phy No. 1 Interface:

1. TXP1 (pin 111); This pin is the transmit twisted pair output positive connection from the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.
2. TXN1 (pin 110); This pin is the transmit twisted pair output negative connection from the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.
3. For Transmit Channel connection and termination details, refer to Figure 1.
4. RXP1 (pin 116); This pin is the receive twisted pair input positive connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.
5. RXN1 (pin 115); This pin is the receive twisted pair input negative connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.
6. For Receive Channel connection and termination details, refer to Figure 2.

LAN9313 (X)VTQFP Phy No. 2 Interface:

1. TXP2 (pin 126); This pin is the transmit twisted pair output positive connection from the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.
2. TXN2 (pin 127); This pin is the transmit twisted pair output negative connection from the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.
3. For Transmit Channel connection and termination details, refer to Figure 1.
4. RXP2 (pin 123); This pin is the receive twisted pair input positive connection to the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.
5. RXN2 (pin 124); This pin is the receive twisted pair input negative connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.
6. For Receive Channel connection and termination details, refer to Figure 2.

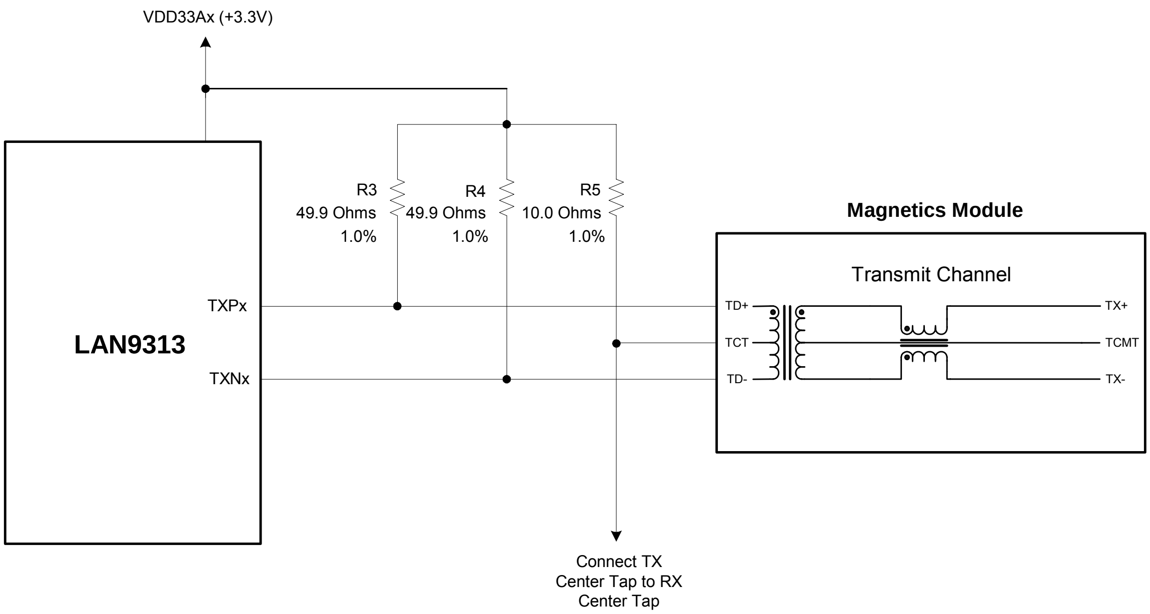

Figure 1 – Transmit Channel Connections and Terminations

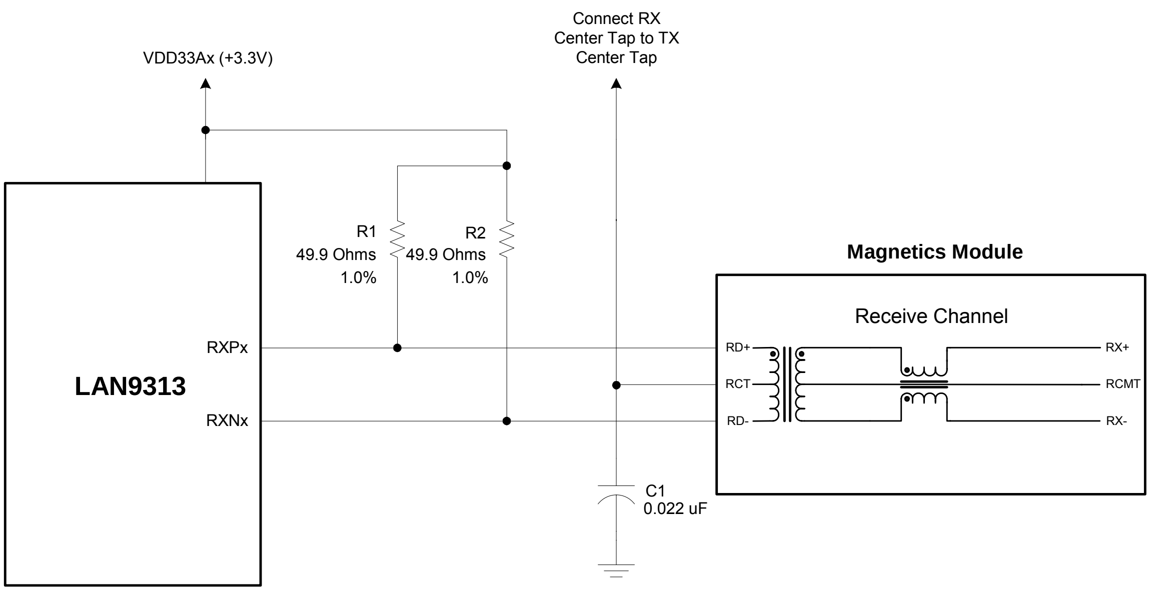

Figure 2 - Receive Channel Connections and Terminations

LAN9313 (X)VTQFP Magnetic No. 1:

1. The center tap connection on the LAN9313 side for the transmit channel must be connected to VDD33A1 (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the primary magnetics also connects to the receive channel center tap of the primary magnetics.

2. The center tap connection on the LAN9313 side for the receive channel is connected to the transmit channel center tap on the primary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the primary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the primary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the primary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP1 (pin 111) of the LAN9313 (X)VTQFP.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN1 (pin 110) of the LAN9313 (X)VTQFP.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP1 (pin 116) of the LAN9313 (X)VTQFP.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN1 (pin 115) of the LAN9313 (X)VTQFP.

10. When using the SMSC LAN931x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 "Suggested Magnetics" for proper magnetics.

LAN9313 (X)VTQFP Magnetic No. 2:

1. The center tap connection on the LAN9313 side for the transmit channel must be connected to VDD33A2 (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the secondary magnetics also connects to the receive channel center tap of the secondary magnetics.

2. The center tap connection on the LAN9313 side for the receive channel is connected to the transmit channel center tap on the secondary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the secondary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the secondary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the secondary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP2 (pin 126) of the LAN9313 (X)VTQFP.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN2 (pin 127) of the LAN9313 (X)VTQFP.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP2 (pin 123) of the LAN9313 (X)VTQFP.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN2 (pin 124) of the LAN9313 (X)VTQFP.

10. When using the SMSC LAN931x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 “Suggested Magnetics” for proper magnetics.

RJ45 Connector No. 1 & No. 2:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

+3.3V Power Supply Connections:

1. The digital supply (VDD33IO) pins on the LAN9313 (X)VTQFP are 7, 13, 21, 27, 33, 39, 46, 54, 64, 66, 72, 73, 81, 87, 93 & 100. They require a connection to +3.3V.

2. Each VDD33IO power pin should have one .01 μF (or smaller) capacitor to decouple the LAN9313. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD33A1) pins for Phy No. 1 on the LAN9313 (X)VTQFP are pins 114 & 117. They require a connection to +3.3V through one ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDD33A1 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9313. The capacitor size should be SMD_0603 or smaller.

5. The analog supply (VDD33A2) pins for Phy No. 2 on the LAN9313 (X)VTQFP are pins 122 & 125. They require a connection to +3.3V through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

6. Each VDD33A2 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9313. The capacitor size should be SMD_0603 or smaller.

7. VDD33BIAS (pin 120), this pin serves as the master bias voltage supply for the LAN9313. This pin requires a connection to +3.3V through a third ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

8. The VDD33BIAS pin should have one .01 μF (or smaller) capacitor to decouple the LAN9313. The capacitor size should be SMD_0603 or smaller.

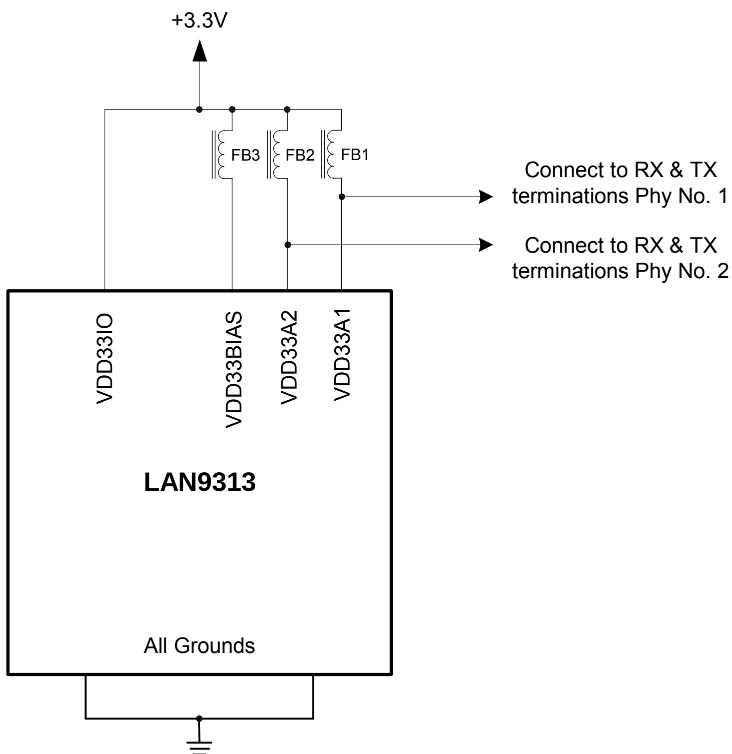

Figure 3 – LAN9313 +3.3V Power Connections

VDD18CORE:

1. VDD18CORE (pins 3, 14, 40, 65, 74, 88 & 104), these seven pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 μF bypass capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 74 requires a bulk capacitor placed as close as possible to pin 74. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 0.1 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only and LAN9313 use only. **Do Not** power other circuits or devices with this supply.

2. VDD18PLL (pin 107), this pin supplies power for the core PLL. This pin must be connected to VDD18CORE through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

3. The VDD18PLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN9313. The capacitor size should be SMD_0603 or smaller.

4. **Do Not**, under any circumstances, connect VDD18CORE to VDD18TX2. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9313.

5. **Do Not**, under any circumstances, use either VDD18CORE or VDD18TX2 to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9313 only.

VDD18TX2:

1. VDD18TX2 (pin 121), this pin is used to provide bypassing for the +1.8V PHY regulator. This pin requires a 0.01 μF bypass capacitor. This capacitor should be located as close as possible to its pin without using vias. In addition, pin 121 requires a bulk capacitor placed as close as possible to pin 121. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 0.1 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only and LAN9313 use only. **Do Not** power other circuits or devices with this supply.

2. VDD18TX1 (pin 118), this pin supplies power to both PHY transmitters. This pin must be connected directly to the VDD18TX2 (pin 121) pin.

3. The VDD18TX1 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9313. The capacitor size should be SMD_0603 or smaller.

4. **Do Not**, under any circumstances, connect VDD18TX2 to VDD18CORE. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9313.

5. **Do Not**, under any circumstances, use either VDD18TX2 or VDD18CORE to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9313 only.

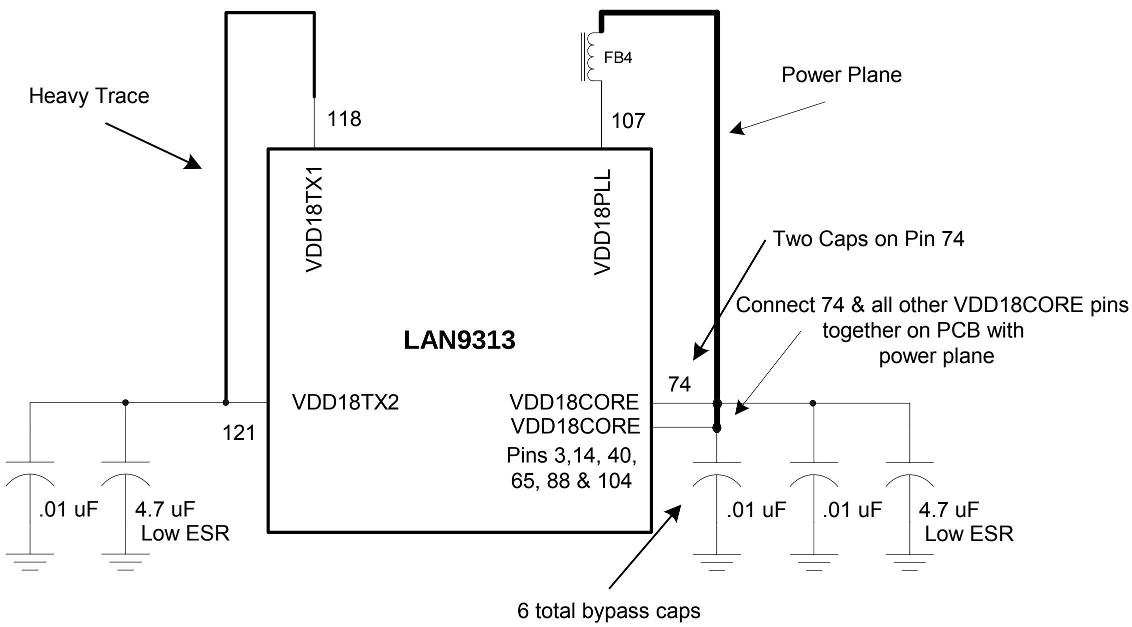

Figure 4 LAN9313 +1.8V Power Connections

Ground Connections:

1. The digital ground pins (VSS) on the LAN9313 (X)VTQFP are 18, 48, 80, 97, 112, 113 & 128. They need to be connected directly to a solid, contiguous ground plane.

2. Both the digital ground pins (VSS) and the GND_CORE pins on the LAN9313 XVTQFP are all connected internally to the exposed die paddle ground. The EDP Ground pad on the underside of the LAN9313 must be connected directly to a solid, contiguous digital ground plane.

3. We recommend that the Digital Ground pins and the EDP pin be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

4. The LAN9313 VTQFP device does not have an exposed die paddle ground. Simply connect all ground pins (VSS) directly to a solid, contiguous ground plane.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9313 (X)VTQFP. For exact specifications and tolerances refer to the latest revision LAN9313 data sheet.

2. XI (pin 105) on the LAN9313 (X)VTQFP is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 106) on the LAN9313 (X)VTQFP is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, an additional 1.0M Ω resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

EEPROM Interfaces:

The LAN9313 supports two different types of EEPROM interfaces. Three pins configure the EEPROM interface on the LAN9313 (X)VTQFP:

1. EEPROM_TYPE (pin 98), functions as a configuration input and is used to select the EEPROM type. Upon the deassertion of reset, this pin selects the EEPROM type depending upon what state it is in.

   When this pin is high, the Philips I^2C EEPROM mode of operation is selected. For this mode, this pin must be pulled high with an external 10.0K Ω pull-up resistor.

   When this pin is low, the National Semiconductor Microwire™ EEPROM mode of operation is selected. For this mode, this pin must be pulled low with an external 10.0K Ω pull-down resistor.

2. EEPROM_SIZE_1 (pin 99), functions as a configuration input and is used to configure the high bit of the EEPROM size range. This bit is not used for I^2C EEPROMs. For Microwire EEPROMS, upon the deassertion of reset, the combination of this pin & the EEPROM_SIZE_0 (pin 101) pin, determines the EEPROM size. For example, configurations range from 128 x 8 for 00h to 2048 x 8 for 10h. 11h is currently reserved. See the LAN9313 Data Sheet for additional details.

3. EEPROM_SIZE_0 (pin 101), functions as a configuration input and is used to configure the low bit of the EEPROM size range. For I^2C EEPROMs, this bit is used solely. For Microwire EEPROMs, both size bits are utilized. For both types of EEPROMs, upon the deassertion of reset, this pin determines the EEPROM size. For example, for I^2C EEPROMs, configurations range from 16 x 8 when this pin is low through 65536 x 8 when this pin is latched high. See the LAN9313 Data Sheet for additional details.

4. The EEPROM_SIZE_1 & EEPROM_SIZE_2 pins do not have internal terminations (internal pull-ups or pull-downs). In order to select the proper configuration, external 10.0K Ω resistors must be used to terminate each pin either high or low. They should not be left as No Connects.

Microwire™ (3-wire) EEPROM Interface:

1. EECS (pin 101) on the LAN9313 (X)VTQFP connects to the external EEPROM's CS pin.

2. EECLK (pin 99) on the LAN9313 (X)VTQFP connects to the external EEPROM's serial clock pin.

3. EEDI (pin 96) on the LAN9313 (X)VTQFP connects to the external EEPROM's Data Out pin.

4. EEDO (pin 98) on the LAN9313 (X)VTQFP connects to the external EEPROM's Data In pin.

5. Be sure to select a 3-wire style EEPROM that matches the organization and size as determined by the configuration pins.

I^2C (2-wire) EEPROM Interface:

1. EE_SCL (pin 99) on the LAN9313 (X)VTQFP connects to the external I^2C EEPROM's serial clock pin.

2. EE_SDA (pin 96) on the LAN9313 (X)VTQFP connects to the external I^2C EEPROM's Data In/Out pin.

3. Be sure to select a 2-wire style EEPROM that matches the organization and size as determined by the configuration pins.

EXRES Resistor:

1. EXRES (pin 119) on the LAN9313 (X)VTQFP should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

Required External Pull-ups/Pull-downs:

1. IRQ (pin 63) may require an external pull-up resistor if this output is programmed as an Open Drain type.

2. EE_SDA (pin 96) requires a 10.0K ohm pull-up resistor in order to guarantee proper operation in the I^2C mode.

3. EE_SCL (pin 99) requires a 10.0K ohm pull-up resistor in order to guarantee proper operation in the I^2C mode.

4. MDIO (pin 12) requires a 1.5K ohm pull-up resistor to +3.3V in order to guarantee proper operation on the SMI.

5. nP1LED0/GPIO0 (pin 92) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

6. nP1LED1/GPIO1 (pin 91) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

7. nP1LED2/GPIO2 (pin 90) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

8. nP1LED3/GPIO3 (pin 89) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

9. nP2LED0/GPIO4 (pin 86) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

10. nP2LED1/GPIO5 (pin 85) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

11. nP2LED2/GPIO6 (pin 84) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

12. nP2LED3/GPIO7 (pin 83) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

MII Interface:

The table below lists each of the pins on the MII Interface of the LAN9313 device. Depending upon which mode of operation (MAC or PHY mode) is selected, each signal is either an input or output. The design engineer should always double check his connections and make sure that outputs from the LAN9313 device are driving inputs on the target device. Also, check that inputs on the LAN9313 are being driven from outputs on the target device.

MII Interface Signal I/O Definitions

Signal Name	Pin Number	MAC Mode	PHY Mode
RXD0	61	Input from Ext Phy	Output to Ext MAC
RXD1	5	Input from Ext Phy	Output to Ext MAC
RXD2	6	Input from Ext Phy	Output to Ext MAC
RXD3	8	Input from Ext Phy	Output to Ext MAC
RXDV	11	Input from Ext Phy	Output to Ext MAC
RXER	9	Input from Ext Phy	Output to Ext MAC
RXCLK	10	Input from Ext Phy	Output to Ext MAC
TXER	62	Output to Ext PHY	Input from Ext MAC
TXD0	23	Output to Ext PHY	Input from Ext MAC
TXD1	22	Output to Ext PHY	Input from Ext MAC
TXD2	20	Output to Ext PHY	Input from Ext MAC
TXD3	19	Output to Ext PHY	Input from Ext MAC
TXEN	4	Output to Ext PHY	Input from Ext MAC
TXCLK	24	Input from Ext Phy	Output to Ext MAC
CRS	16	Input from Ext Phy	Output to Ext MAC
COL	17	Input from Ext Phy	Output to Ext MAC
		SMI/MII Slave	**MII Master**
MDIO	12	I/O to Ext Master	I/O to Ext Phy
MDC	15	Input from Ext Master	Output to Ext Phy

1. MII_DUPLEX (pin 60), this strap pin sets the Duplex operation of the MII Port. The value can be changed at any time (live value) and can be overridden by disabling the Auto Negotiation (VPHY_AN) bit in the Virtual PHY Basic Control register. In MAC mode, this pin is typically tied to the duplex indication from the external Phy. In PHY mode, this signal is typically held high or low as required. The polarity of this signal depends upon the duplex_pol_strap_mii strap. If duplex_pol_strap_mii is zero, a MII_DUPLEX value of zero indicates Full Duplex and a one indicates Half Duplex operation. If duplex_pol_strap_mii is one, a MII_DUPLEX value of one indicates Full Duplex and a zero indicates Half Duplex operation. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Serial Management Modes:

1. MNGT_MODE0 (pin 28) & MNGT_MODE1 (pin 26), these two pins configure the serial management mode of the LAN9313. The modes are as follows:

   00 = Unmanaged Mode
   01 = SMI Managed Mode
   10 = I^2C Managed Mode
   11 = SPI Managed Mode

   See the latest version of the LAN9313 data sheet for complete details. These pins have weak internal pull-ups and can be driven low with an external 1.0K Ω resistor to digital ground.

Management SPI Slave Mode:

1. SI (pin 67), SPI Slave Serial Data Input pin. This pin has an internal pull-up in SPI Mode.

2. SO (pin 68), SPI Slave Serial Data Output pin. This pin is only operational in SPI Mode. It is driven low in all other modes of operation.

3. nSCS (pin 69), SPI Slave Chip Select pin. When low, the SPI Slave is selected for SPI transfers. When high, the SPI serial data output (SO) is tri-stated. This pin is only operational in SPI Mode. This pin has an internal pull-up enabled at all times.

4. SCK (pin 70), SPI Slave Serial input Clock pin. This pin has an internal pull-up in SPI Mode.

Management I^2C Slave Mode:

1. SDA (pin 67), I^2C Slave Serial Data Input/Output pin. This pin is an open-drain output in I^2C mode and requires an external 10K Ω pull-up resistor. The internal pull-up termination is disabled in I^2C mode.

2. SCL (pin 70), I^2C Slave Serial Clock pin. This pin is an input in I^2C mode and requires an external 10K Ω pull-up resistor. The internal pull-up termination is disabled in I^2C mode.

Dedicated Configuration Strap Pins:

1. All configuration strap values are latched in on power-on reset or nRST de-assertion. For more detailed information of each bit and functionality, consult the latest version of LAN9313 data sheet.

2. LED_FUN0 (pin 47) & LED_FUN1 (pin 45), these two strap pins configure the default value for the LED_FUN bits in the LED configuration Register (LED_CFG). LED pins nP1LED[3:0] & nP2LED[3:0] can be programmed to display one of four combinations of various Ethernet activity such as Speed, Link, RX & TX Activity, and more. See the latest version of the LAN9313 data sheet for complete details. These pins have weak internal pull-ups and can be driven low with an external 1.0K Ω resistor to digital ground.

3. MII_MODE (pin 25), this pin configures the operating mode of the external MII port. The modes are as follows:

   0 = MAC Mode
   1 = PHY Mode

   This pin is LAN9313 centric. With the LAN9313 in MAC mode, typical applications will connect an external Phy to the MII Interface. With the LAN9313 in Phy mode, typical applications will connect an external MAC to the MII Interface. See the latest version of the LAN9313 data sheet for complete details. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

4. PHY_ADDR_SEL (pin 95), functions as a configuration input and is used to establish the default MII Management address values for the three internal PHYs. See the LAN9313 data sheet for further details on PHY addressing. Upon the deassertion of reset, this pin selects the functionality depending upon what state it is in.

   With this pin low, the PHY addressing will start with 00h. This mode can be achieved with a 1.0K Ω pull-down resistor added to this pin.

   0 = Virtual PHY Address = 00
   Port 1 PHY Address = 01
   Port 2 PHY Address = 02

   If this pin is high, the PHY addressing will start with 01h. This mode can be achieved by leaving this pin as a no-connect as this pin has an internal pull-up.

   1 = Virtual PHY Address = 01
   Port 1 PHY Address = 02
   Port 2 PHY Address = 03

   See the latest version of the LAN9313 data sheet for complete details.

Port 0 Configuration Straps:

1. SPEED_MII (pin 34), together with the DUPLEX_POL_MII and MMI_DUPLEX pins, this strap configures the base ability values in the Virtual Phy Auto Negotiation Link Partner Base Page Ability Register. This pin also configures the speed for Port 0 when the Virtual Auto Negotiation fails. When latched low, 10BASE-T operation is enabled. When latched high, 100BASE-TX operation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

2. DUPLEX_POL_MII (pin 32), this strap pin configures the polarity of the MII_DUPLEX pin for Port 0. If MII_DUPLEX = DUPLEX_POL_MII, Full Duplex operation is enabled. If MII_DUPLEX ! = DUPLEX_POL_MII, Half Duplex operation is selected. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

3. BP_EN_MII (pin 31), this strap pin configures the default value for the Port 0 Back Pressure Enable bit in the Port 0 Manual Flow Control register. When latched low, Back Pressure is disabled. When latched high, Back Pressure is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

4. FD_FC_MII (pin 30), this strap pin configures the default value for the Port 0 Full Duplex Transmit Flow Control Enable and the Port 0 Full Duplex Receive Flow Control Enable bits in the Port 0 Manual Flow Control register. When latched low, Full Duplex Pause Packet Detection and Generation is disabled. When latched high, Full Duplex Pause Packet Detection and Generation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

5. MANUAL_FC_MII (pin 29), this strap pin configures the default value for the Port 0 Full Duplex Manual Flow Control Select bit in the Port 0 Manual Flow Control register. When latched low, Flow Control is determined by Virtual Auto Negotiation. When latched high, Flow Control is determined by the Port 0 Full Duplex Transmit Flow Control Enable and Port 0 Full Duplex Receive Flow Control Enable bits. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Port 1 Configuration Straps:

1. AUTO_MDIX_1 (pin 56), this strap pin configures the default value for the Auto MDIX functionality on Port 1. When latched low, Auto MDIX is disabled. When latched high, Auto MDIX is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

2. AUTO_NEG_1 (pin 55), this strap pin configures the default value for the Auto Negotiation enable bit in the PHY_BASIC_CTRL_1 register. When latched low, Auto Negotiation is disabled. When latched high, Auto Negotiation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

3. SPEED_1 (pin 53), this strap pin configures the default value for the Speed Select LSB in the PHY_BASIC_CTRL_1 register. When latched low, 10BASE-T operation is enabled. When latched high, 100BASE-TX operation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

4. DUPLEX_1 (pin 52), this strap pin configures the default value for the Duplex Mode in the PHY_BASIC_CTRL_1 register. When latched low, Half Duplex operation is enabled. When latched high, Full Duplex operation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

5. BP_EN_1 (pin 51), this strap pin configures the default value for the Port 1 Back Pressure Enable bit in the Port 1 Manual Flow Control register. When latched low, Back Pressure is disabled. When latched high, Back Pressure is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

6. FD_FC_1 (pin 50), this strap pin configures the default value for the Port 1 Full Duplex Transmit Flow Control Enable and the Port 1 Full Duplex Receive Flow Control Enable bits in the Port 1 Manual Flow Control register. When latched low, Full Duplex Pause Packet Detection and Generation is disabled. When latched high, Full Duplex Pause Packet Detection and Generation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

7. MANUAL_FC_1 (pin 49), this strap pin configures the default value for the Port 1 Full Duplex Manual Flow Control Select bit in the Port 1 Manual Flow Control register. When latched low, Flow Control is determined by Auto Negotiation. When latched high, Flow Control is determined by the Port 1 Full Duplex Transmit Flow Control Enable and Port 1 Full Duplex Receive Flow Control Enable bits. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Port 2 Configuration Straps:

1. AUTO_MDIX_2 (pin 43), this strap pin configures the default value for the Auto MDIX functionality on Port 2. When latched low, Auto MDIX is disabled. When latched high, Auto MDIX is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

2. AUTO_NEG_2 (pin 42), this strap pin configures the default value for the Auto Negotiation enable bit in the PHY_BASIC_CTRL_2 register. When latched low, Auto Negotiation is disabled. When latched high, Auto Negotiation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

3. SPEED_2 (pin 41), this strap pin configures the default value for the Speed Select LSB in the PHY_BASIC_CTRL_2 register. When latched low, 10BASE-T operation is enabled. When latched high, 100BASE-TX operation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

4. DUPLEX_2 (pin 38), this strap pin configures the default value for the Duplex Mode in the PHY_BASIC_CTRL_2 register. When latched low, Half Duplex operation is enabled. When latched high, Full Duplex operation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

5. BP_EN_2 (pin 37), this strap pin configures the default value for the Port 2 Back Pressure Enable bit in the Port 2 Manual Flow Control register. When latched low, Back Pressure is disabled. When latched high, Back Pressure is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

6. FD_FC_2 (pin 36), this strap pin configures the default value for the Port 2 Full Duplex Transmit Flow Control Enable and the Port 2 Full Duplex Receive Flow Control Enable bits in the Port 2 Manual Flow Control register. When latched low, Full Duplex Pause Packet Detection and Generation is disabled. When latched high, Full Duplex Pause Packet Detection and Generation is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

7. MANUAL_FC_2 (pin 35), this strap pin configures the default value for the Port 2 Full Duplex Manual Flow Control Select bit in the Port 2 Manual Flow Control register. When latched low, Flow Control is determined by Auto Negotiation. When latched high, Flow Control is determined by the Port 2 Full Duplex Transmit Flow Control Enable and Port 2 Full Duplex Receive Flow Control Enable bits. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Miscellaneous:

1. There are 10 No-Connect pins on the LAN9313. It is very important that these pins remain as no-connects. These pins are 1, 2, 57, 58, 59, 76, 94, 102, 103 & 109.

   Caution: To ensure normal device operation, pin 102 must be low at all times. Pin 102 has an internal pull-down. Do not add any type of external pull-up or other circuit connection to this pin as this will result in configuring the device disabled. This pin must be left as a No-Connect.

2. LED_EN (pin 44), functions as a configuration input and is used to establish the functionality of the nPxLEDx/GPIOx pins. Upon the deassertion of reset, this pin selects the functionality depending upon what state it is in.

   With this pin low, the LAN9313 will configure all eight LED/GPIO pins as GPIOs. This mode can be achieved with a 1.0K Ω pull-down resistor added to this pin.

   If this pin is high, the LAN9313 will configure all eight LED/GPIO pins as LEDs. This mode can be achieved by leaving this pin as a no-connect as this pin has an internal pull-up.

3. nRST (pin 71), this pin is an active-low reset input. This signal resets all logic and registers within the LAN9313. This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected the LAN9313 will rely on its internal power-on reset circuitry.

4. TEST1 (pin 75), this pin must be connected to +3.3V.

5. TEST2 (pin 108), this pin must be connected to +3.3V.

6. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

7. Be sure to incorporate enough bulk capacitors (4.7 - 22µF caps) for each power plane.

LAN9313 (X)VTQFP QuickCheck Pinout Table:

Use the following table to check the LAN9313 (X)VTQFP shape in your schematic.

LAN9313 (X)VTQFP							
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC1	33	VDD33IO	65	VDD18CORE	97	VSS
2	NC2	34	SPEED_MII	66	VDD33IO	98	EEDO
3	VDD18CORE	35	MAN_FC_2	67	SI/SDA	99	EECLK
4	TXEN	36	FD_FC_2	68	SO	100	VDD33IO
5	RXD1	37	BP_EN_2	69	nSCS	101	EECS
6	RXD2	38	DUPLEX_2	70	SCK/SCL	102	NC8
7	VDD33IO	39	VDD33IO	71	nRST	103	NC9
8	RXD3	40	VDD18CORE	72	VDD33IO	104	VDD18CORE
9	RXER	41	SPEED_2	73	VDD33IO	105	XI
10	RXCLK	42	AUTO_NEG_2	74	VDD18CORE	106	XO
11	RXDV	43	AUTO_MDIX_2	75	TEST1	107	VDD18PLL
12	MDIO	44	LED_EN	76	NC6	108	TEST2
13	VDD33IO	45	LED_FUN1	77	GPIO11	109	NC10
14	VDD18CORE	46	VDD33IO	78	GPIO10	110	TXN1
15	MDC	47	LED_FUN0	79	GPIO9	111	TXP1
16	CRS	48	VSS	80	VSS	112	VSS
17	COL	49	MAN_FC_1	81	VDD33IO	113	VSS
18	VSS	50	FD_FC_1	82	GPIO8	114	VDD33A1
19	TXD3	51	BP_EN_1	83	nP2LED3	115	RXN1
20	TXD2	52	DUPLEX_1	84	nP2LED2	116	RXP1
21	VDD33IO	53	SPEED_1	85	nP2LED1	117	VDD33A1
22	TXD1	54	VDD33IO	86	nP2LED0	118	VDD18TX1
23	TXD0	55	AUTO_NEG_1	87	VDD33IO	119	EXRES
24	TXCLK	56	AUTO_MDIX_1	88	VDD18CORE	120	VDD33BIAS
25	MII MODE	57	NC3	89	nP1LED3	121	VDD18TX2
26	MNGT_MODE1	58	NC4	90	nP1LED2	122	VDD33A2
27	VDD33IO	59	NC5	91	nP1LED1	123	RXP2
28	MNGT_MODE0	60	MII_DUPLEX	92	nP1LED0	124	RXN2
29	MAN_FC_MII	61	RXD0	93	VDD33IO	125	VDD33A2
30	FD_FC_MII	62	TXER	94	NC7	126	TXP2
31	BP_EN_MII	63	IRQ	95	PHY_ADDR_SEL	127	TXN2
32	DUP_POL_MII	64	VDD33IO	96	EEDI	128	VSS
129 Note 1				EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package			

Notes:

1. Pin 129 (EDP) is not present on the VTQFP Package

Reference Material:

1. SMSC LAN9313 Data Sheet; check web site for latest revision.
2. SMSC LAN9313 EVB Schematic, Assembly No. 6471; check web site for latest revision.
3. SMSC LAN9313 EVB PCB, Assembly No. 6471; order PCB from web site.
4. SMSC LAN9313 EVB PCB Bill of Materials, Assembly No. 6471; check web site for latest revision.
5. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.