

LAN8841 Silicon Errata & Data Sheet Clarification

This document describes known silicon errata for the Microchip LAN8841 device, which include the following variants:

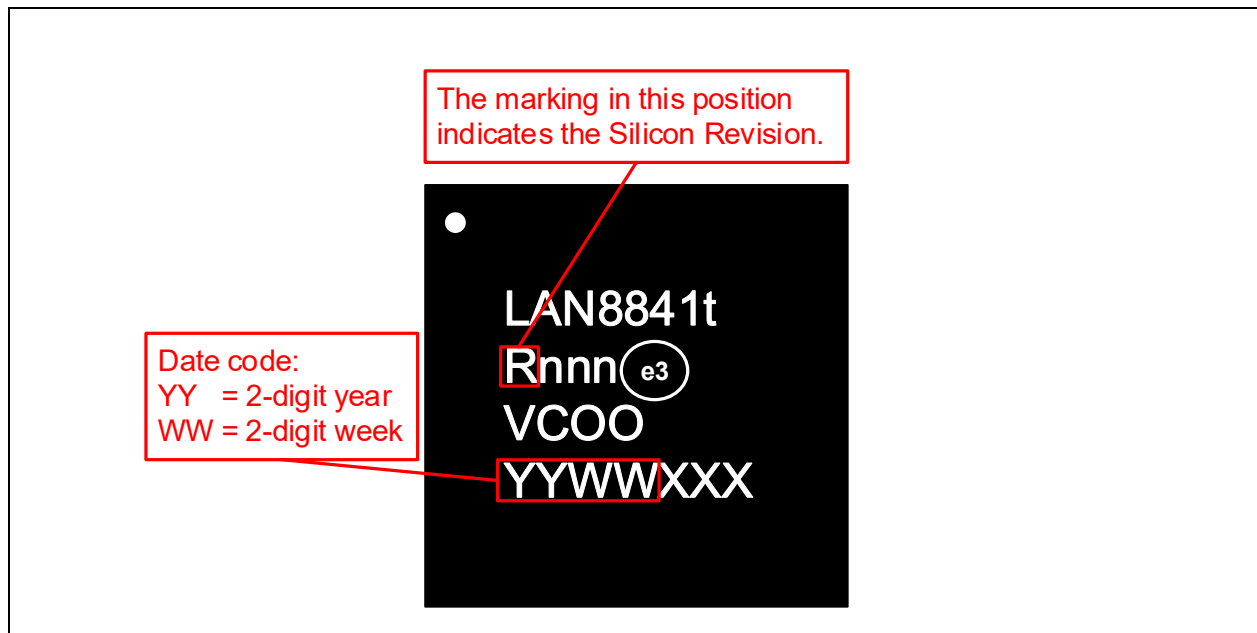
- LAN8841/Q2A
- LAN8841V/Q2A

The silicon errata discussed in this document are for silicon revisions as listed in [Table 1](#). The silicon revision can be determined by the device's top marking as indicated in [Figure 1](#). A summary of LAN8841 silicon errata is provided in [Table 2](#).

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
LAN8841/Q2A LAN8841V/Q2A	B

FIGURE 1: TOP MARKING DATE CODE INDICATION



Note: The purpose of [Figure 1](#) is to detail the top markings of an example part and highlight the location of the silicon revision code. Other top marking values may differ (lot codes, location of manufacture, etc.).

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification	B0
2.	Analog front-end not optimized for PHY-side shorted center taps	B0
3.	Register read may be needed after soft reset with 10/100 Link Partner	B0
4.	IEEE Clause 40 PMA compliance tests may fail	B0
5.	LDO tuning adjustment to supply proper VDD/VDDAL range to device	B0
6.	RGMI1 100Mbps latency adjustment for PTP timing	B0

Silicon Errata Issues

Module 1: 1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification

DESCRIPTION

The device's 1000BASE-T Transmitter Distortion exceeds the <10mV limit indicated in the IEEE specification.

END USER IMPLICATIONS

It is unlikely this specification failure will impact system performance. The following Application Note provides more details regarding the Gigabit Transmit Distortion test:

<https://www.microchip.com/en-us/application-notes/an3455>

Work Around

None

PLAN

This erratum will not be corrected in a future revision.

Module 2: Analog front-end not optimized for PHY-side shorted center taps

DESCRIPTION

When connecting the PHY to magnetics which short center-tap connections on the PHY-facing winding, the default register settings of the device need to be optimized for better electrical performance.

END USER IMPLICATIONS

When magnetics with shorted center-tap connections are used, register settings should be applied for optimized operation at 10Mbps and 100Mbps speeds. It is expected that the device is configuration strapped for use with shorted center-tap magnetics in such a design. If separate center-tap magnetics are used, then these settings are not needed.

Work Around

Check MMD Address 2, Register 2 bit 14 = 1 (Device is strapped for shorted center-tap magnetics). If this bit is set, the following two registers need configuration to the following values:

MMD Address 1C, Register 45 (MMD 28.69) = 0xBFFC

MMD Address 1C, Register 46 (MMD 28.70) = 0x00AF

PLAN

This erratum will not be corrected in a future revision.

Module 3: Register read may be needed after soft reset with 10/100 Link Partner

DESCRIPTION

After a soft reset, the device can have an issue if the link partner is in 10Mbps or 100Mbps speed. In such a situation, a read of any register will resolve the issue.

END USER IMPLICATIONS

The device will not link after soft reset as the duplex of the link is not resolved. A register read restarts the algorithm to establish the correct duplex mode for a 10/100Mbps link partner. The issue is not seen when the link partner is in auto-negotiation and 1000Mbps capable.

Work Around

A read of any device register after soft reset will resolve the issue.

PLAN

This erratum will not be corrected in a future revision.

Module 4: IEEE Clause 40 PMA compliance tests may fail

DESCRIPTION

The default register settings of the device's 1000BASE-T PMA are sub-optimal, and may result in UNH compliance failures for Clause 40 PMA Transmitter tests. The default register settings of the device require optimization.

END USER IMPLICATIONS

It is recommended to apply the settings unconditionally, for better PHY interoperability performance.

Work Around

The following registers settings will optimize PHY interoperability performance:

MMD Address 1C, Register 1 (MMD 28.1) = 0x0040

MMD Address 1C, Register D (MMD 28.13) = 0x0001

PLAN

This erratum will not be corrected in a future revision.

Module 5: LDO tuning adjustment to supply proper VDD/VDDAL range to device

DESCRIPTION

The device LDO provides VDD/VDDAL voltage slightly out of range using default settings. An LDO adjustment is necessary to provide adequate VDD/VDDAL operating voltage range to the device.

END USER IMPLICATIONS

It is recommended to apply the adjusted settings for designs using the LDO for proper VDD/VDDAL supply to the device. For non-LDO designs, these settings are optional, however these settings will not degrade performance in either LDO designs or non-LDO designs.

Work Around

The following register setting will optimize the LDO for VDD/VDDAL supply:

MMD Address 1C, Register E (MMD 28.14) = 0x1000

PLAN

This erratum will not be corrected in a future revision.

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Module 6: RGMII 100Mbps latency adjustment for PTP timing

DESCRIPTION

At 100Mbps speed, the device may have link-to-link RGMII PTP latency variation between 0 ns and 40 ns. This PTP latency variation can be adjusted to between 0 ns and 8 ns. The RGMII PTP latency for 10Mbps or 1000Mbps is under 10 ns without any adjustments necessary.

END USER IMPLICATIONS

For applications which can handle PTP latency variation of up to 40 ns, no additional register setting is necessary. However, for applications which require tighter timing, register settings can improve the variation to a tighter 0 ns to 8 ns range. This improves the 100Mbps RGMII PTP accuracy for such applications.

Work Around

The RGMII 100Mbps PTP timing latency variation can be reduced with the following register writes:

MMD Address 1, Register C6 (MMD 1.198) = 0x0000

MMD Address 0, Register 11 (MMD 0.17) = 0x000A

PLAN

This erratum will not be corrected in a future revision.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80001056A (10-06-22)	All	Initial release

LAN8841

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