LAN9255

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip LAN9255 2/3-Port EtherCAT® Device Controller and SAM 32-bit MCU. The LAN9255 consists of a LAN9253 EtherCAT Device Controller and a SAM E53J 32-bit ARM Cortex-M4F MCU in a single 128-pin TQFP package. All signals from both devices are brought out to pins, and there are no internal connections between the two devices. The EtherCAT device controller should be connected to the MCU via the QSPI interface. A summary of these items is provided in Section 15.0, "Hardware Checklist Summary". Detailed information for verifying the correct design can be found in the following sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Ethernet/EtherCAT® Signals"
- Section 5.0, "Clock Circuit"
- Section 6.0, "Configuration for System Applications"
- Section 7.0, "Microcontroller Mode Via SPI/SQI Interface"
- Section 8.0, "Expansion Mode with MII Interface for Extra Port"
- Section 9.0, "EEPROM Interface"
- Section 10.0, "Digital I/O Pins"
- Section 11.0, "Ethernet/EtherCAT® LED Indicators"
- Section 12.0, "SAM E53J Ethernet MAC Interface"
- Section 13.0, "SAM E53J Programming and Debug Ports"
- Section 14.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The LAN9255 implementor should have the following documents on hand:

- *SAM D5x/E5x Family Data Sheet*
- *LAN9255 2/3-Port EtherCAT® Device Controller with Integrated PHYs & SAM E53J 32-bit ARM® Cortex®-M4F MCU Data Sheet*
- *LAN9253 2/3-Port EtherCAT® Device Controller with Integrated Ethernet PHYs Data Sheet*

2.2 Pin Check

- Check the pinout of the schematic symbol against the data sheet. Ensure that all symbol pins match the data sheet and are correctly configured as inputs, outputs, or bidirectional for error checking.
- Refer to Table 2-1 to check the LAN9255 pinout.

TABLE 2-1: LAN9255 PINOUT

Pin Number	Pin Name	Device
1	OSCO	LAN9253
2	PB03	SAM E53J
3	PA00	SAM E53J
4	OSCVDD12	LAN9253
5	PA01	SAM E53J
6	OSCVSS	LAN9253
7	VDD33	LAN9253
8	PA02	SAM E53J
9	PA03	SAM E53J
10	PB04	SAM E53J
11	PB05	SAM E53J
12	VDDCR	LAN9253
13	REG_EN	LAN9253
14	CLK_25/CLK_25_EN/XTAL_MODE	LAN9253
15	GNDANA	SAM E53J
16	VDDANA	SAM E53J
17	ERRLED/PME/100FD_B/LEDPOL4	LAN9253
18	WAIT_ACK/PME/LATCH0/EE_EMUL_SPI3	LAN9253
19	PB06	SAM E53J
20	PB07	SAM E53J
21	RST#	LAN9253
22	PB08	SAM E53J
23	PB09	SAM E53J
24	D2/AD2/SOF/SIO2/EE_EMUL_SPI0	LAN9253
25	PA04	SAM E53J
26	D1/AD1/EOF/SO/SIO1	LAN9253
27	PA05	SAM E53J
28	PA06	SAM E53J
29	VDDIO_J	LAN9253
30	PA07	SAM E53J
31	D14/AD14/DIGIO8/GPI8/GPO8/MII_TXD3/TX_SHIFT1	LAN9253
32	D13/AD13/DIGIO7/GPI7/GPO7/MII_TXD2/TX_SHIFT0	LAN9253
33	PA08	SAM E53J
34	PA09	SAM E53J
35	PA10	SAM E53J
36	PA11	SAM E53J
37	VDDIOB	SAM E53J
38	D0/AD0/WD_STATE/SI/SIO0	LAN9253
39	SYNC1/LATCH1/PME	LAN9253
40	PB10	SAM E53J
41	D9/AD9/LATCH_IN/SCK	LAN9253
42	PB11	SAM E53J
43	PB12	SAM E53J

TABLE 2-1: LAN9255 PINOUT (CONTINUED)

Pin Number	Pin Name	Device
44	PB13	SAM E53J
45	VDDIO_J	LAN9253
46	PB14	SAM E53J
47	PB15	SAM E53J
48	NC	N/A
49	D12/AD12/DIGIO6/GPI6/GPO6/MII_TXD1/100FD_B	LAN9253
50	D11/AD11/DIGIO5/GPI5/GPO5/MII_TXD0/100FD_A	LAN9253
51	D10/AD10/DIGIO4/GPI4/GPO4/MII_TXEN	LAN9253
52	VDDCR	LAN9253
53	A1/ALELO/OE_EXT/MII_CLK25/EE_EMUL_SPI2	LAN9253
54	A3/BE0/DIGIO11/GPI11/GPO11/MII_RXDV	LAN9253
55	A4/BE1/DIGIO12/GPI12/GPO12/MII_RXD0	LAN9253
56	CS/DIGIO13/GPI13/GPO13/MII_RXD1	LAN9253
57	A2/ALEHI/DIGIO10/GPI10/GPO10/LINKACTLED2/ EE_EMUL_ALELO_POL/MII_LINKPOL/LEDPOL2	LAN9253
58	WR/ENB/DIGIO14/GPI14/GPO14/MII_RXD2	LAN9253
59	RD/RD_WR/DIGIO15/GPI15/GPO15/MII_RXD3	LAN9253
60	VDDIO_J	LAN9253
61	PA12	SAM E53J
62	PA13	SAM E53J
63	PA14	SAM E53J
64	PA15	SAM E53J
65	VDDIO_S	SAM E53J
66	A0/D15/AD15/DIGIO9/GPI9/GPO9/MII_RXER	LAN9253
67	PA16	SAM E53J
68	PA17	SAM E53J
69	PA18	SAM E53J
70	SYNC0/LATCH0/PME	LAN9253
71	D3/AD3/WD_TRIG/SIO3/EE_EMUL_SPI1	LAN9253
72	D6/AD6/DIGIO0/GPI0/GPO0/MII_RXCLK	LAN9253
73	PA19	SAM E53J
74	VDDIO_J	LAN9253
75	NC	N/A
76	VDDCR	LAN9253
77	PB16	SAM E53J
78	D7/AD7/DIGIO1/GPI1/GPO1/MII_MDC	LAN9253
79	PB17	SAM E53J
80	D8/AD8/DIGIO2/GPI2/GPO2/MII_MDIO	LAN9253
81	TESTMODE	LAN9253
82	EESDA/TMS/EE_EMUL1	LAN9253
83	EESCL/TCK/EE_EMUL2	LAN9253
84	PA20	SAM E53J
85	NC	N/A
86	NC	N/A

TABLE 2-1: LAN9255 PINOUT (CONTINUED)

Pin Number	Pin Name	Device
87	PA21	SAM E53J
88	IRQ/LATCH1	LAN9253
89	RUNLED/STATE_RUNLED/E2PSIZE/EE_EMUL0/LEDPOL3	LAN9253
90	LINKACTLED1/TDI/CHIP_MODE1/LEDPOL1	LAN9253
91	PA22	SAM E53J
92	PA23	SAM E53J
93	PA24	SAM E53J
94	VDDIO_J	LAN9253
95	LINKACTLED0/TDO/CHIP_MODE0/100FD_A/LEDPOL0	LAN9253
96	PA25	SAM E53J
97	VDDIO_S	SAM E53J
98	PB22	SAM E53J
99	PB23	SAM E53J
100	D4/AD4/DIGIO3/GPI3/GPO3/MII_LINK	LAN9253
101	D5/AD5/OUTVALID/SCS#	LAN9253
102	VDD33TXRX1	LAN9253
103	TXNA	LAN9253
104	TXPA	LAN9253
105	RXNA	LAN9253
106	RXPA	LAN9253
107	PA27	SAM E53J
108	RESETN_E53	SAM E53J
109	VDDCORE	SAM E53J
110	VDD12TX1	LAN9253
111	RBIAS	LAN9253
112	VDD33BIAS	LAN9253
113	VDD12TX2	LAN9253
114	VSW	SAM E53J
115	RXPB	LAN9253
116	RXNB	LAN9253
117	VDDIO_S	SAM E53J
118	TXPB	LAN9253
119	TXNB	LAN9253
120	PA30	SAM E53J
121	PA31	SAM E53J
122	PB30	SAM E53J
123	PB31	SAM E53J
124	VDD33TXRX2	LAN9253
125	PB00	SAM E53J
126	PB01	SAM E53J
127	PB02	SAM E53J
128	OSCI	LAN9253
129	EDP Ground, Exposed Die Paddle Ground, Pad on Bottom of Package	Both

3.0 POWER

3.1 +3.3V Power Supply Connections

- The supply for the two internal regulators on the LAN9253 is pin 7 (**VDD33**). This pin requires a connection to +3.3V. The **VDD33** power pin should have one 1 µF capacitor and one 0.1 µF capacitor for decoupling. The capacitor size should be SMD_0603 or smaller.

Note: +3.3V must be supplied to this pin even if the internal regulators are disabled.

- The analog supply (**VDD33TXRX1**) pin on the LAN9253 is pin 102. It requires a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. The **VDD33TXRX1** pin should have one 0.1 µF to 0.01 µF capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.
- The analog supply (**VDD33TXRX2**) pin on the LAN9253 is pin 124. It requires a connection to +3.3V through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. The **VDD33TXRX2** pin should have one 0.1 µF to 0.01 µF capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.
- The **VDD33BIAS** (pin 112) pin serves as the central bias voltage supply for the LAN9253. This pin requires a connection to +3.3V through a third ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. The **VDD33BIAS** pin should have one 0.1 µF to 0.01 µF capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.

3.2 +1.8V to +3.3V Variable I/O Power Supply Connections

- The succeeding power pins require 1.8V to 3.3V. Except where noted, they are all independent and can be supplied at different voltages if necessary. In addition, they may all be powered from a single supply.
- Each unique supply voltage should be decoupled with at least 10 µF of bulk capacitance.
- **VDDIO_J** powers the LAN9253 I/O pins. Place a 0.1 µF to 0.01 µF decoupling capacitor near each of the five **VDDIO_J** pins.
- **VDDIOB** powers the SAM E53J I/O pins PB8, PB9, PB10, and PB11. Place a 0.1 µF to 0.01 µF decoupling capacitor near the **VDDIOB** pin.
- **VDDIO_S** and **VDDANA** must share the same supply. **VDDIO_S** and **VDDANA** power the SAM E53J I/O pins that are not powered by **VDDIOB**.
- **VDDANA** should be filtered with a ferrite bead (33Ω to 220Ω @ 100 MHz, <1.0Ω DC) with a 10 µF bulk capacitor on each side of the bead. **VDDIO_S** does not require a ferrite bead. Place a 0.1 µF to 0.01 µF decoupling capacitor close to the chip, between **VDDANA** (pin 16) and **GNDANA** (pin 15).
- **VDDIO_S** does not require a ferrite bead. Place a 0.1 µF to 0.01 µF decoupling capacitor near each of the three **VDDIO_S** pins.

3.3 VDDCORE and VSW

- The **VDDCORE** (pin 109) pin is used to provide bypassing for the SAM E53J +1.2V regulator output. Connect one 4.7 µF and one 100 nF capacitor from this pin to ground. These capacitors should be located as close as practical to this pin.

Caution: This +1.2V supply is for internal logic only. Do not power other external circuits or devices with this supply.

- The **VSW** (pin 114) pin is used only if the SAM E53J regulator is operated in Switching mode. When the regulator will be operated in Switching mode, connect a 10 µH inductor between VSW and VDDCORE. If the regulator will only be operated in Linear mode, leave **VSW** open.

3.4 VDDCR

3.4.1 INTERNAL REGULATOR ENABLE MODE (REG_EN PIN PULL-UP)

- The **VDDCR** pins (pins 12, 52, and 76) are used to provide bypassing for the +1.2V core regulator. Both pin 52 and pin 76 require a 0.1 µF to 0.01 µF decoupling capacitor. Each capacitor should be located as close as possible to each pin without using vias. Pin 12 requires a 1.0 µF (or greater) bulk capacitor and a 470 pF bypass capacitor. Place both of them as close as possible to pin 12, particularly the 470 pF capacitor. The bulk capacitor must have an equivalent series resistance (ESR) of no more than 2.0Ω. Microchip recommends a very low 0.1Ω ESR ceramic capacitor for design stability. Other values, tolerances, and characteristics are not recommended.

Caution: This +1.2V supply is for internal logic only. Do not power other external circuits or devices with this supply.

- **OSCVDD12** (pin 4) can be left floating in internal regulator Enable mode.
- The **VDD12TX1** (pin 110) and **VDD12TX2** (pin 113) pins derive power from **VDDCR** pin through a ferrite bead for the two Ethernet blocks. These two pins must be tied together. Be sure to place bulk capacitance on each side of the ferrite bead.
- The **VDD12TX1** and **VDD12TX2** pins should each have one 0.1 µF to 0.01 µF decoupling capacitor. The capacitor size should be SMD_0603 or smaller.

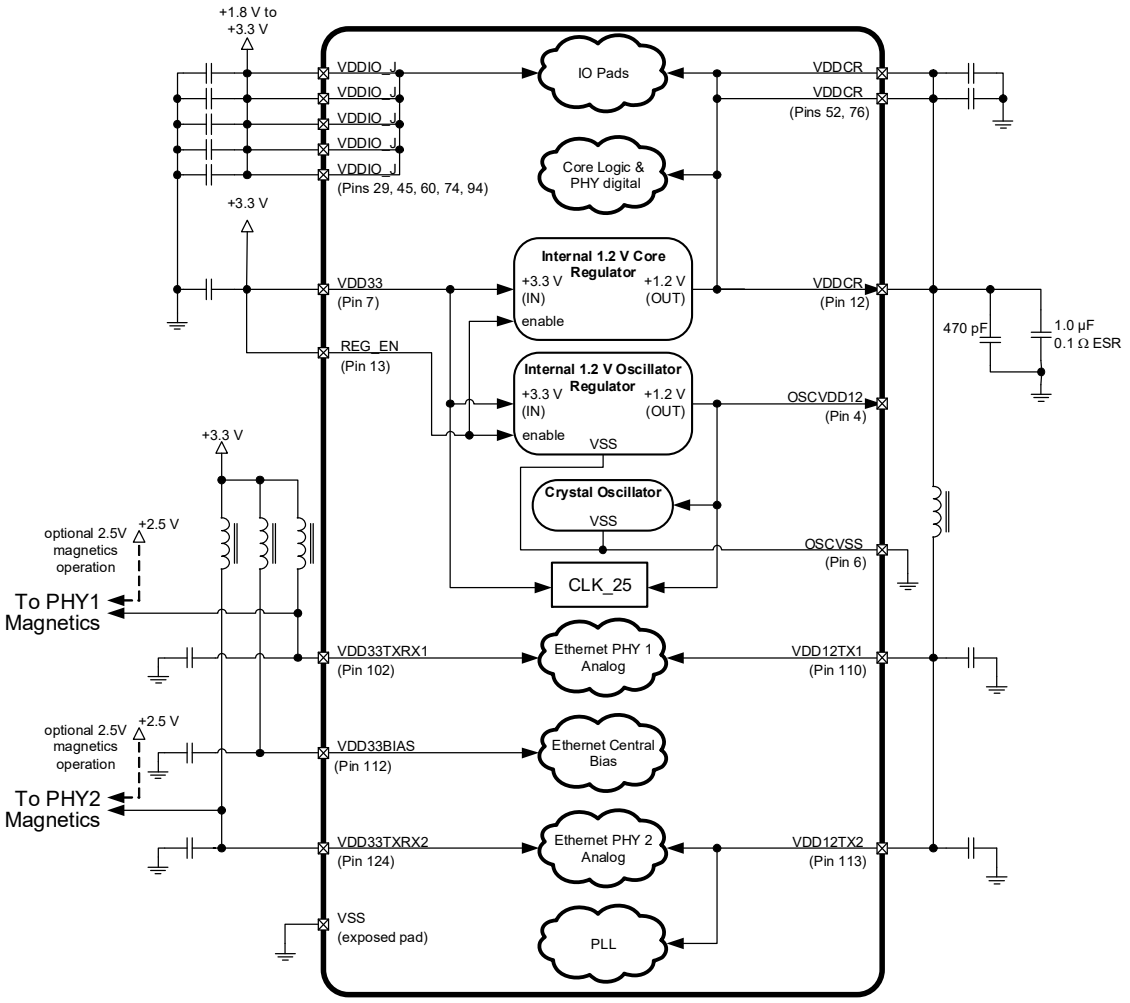
3.4.2 INTERNAL REGULATOR DISABLE MODE (REG_EN PIN PULL-DOWN)

- Connect an external 1.2V supply directly to OSCVDD12 (pin 4) and VDDCR (pins 12, 52, and 76).
- OSCVDD12 and each VDDCR pin requires a 0.1 µF to 0.01 µF decoupling capacitor. Each capacitor should be located as close as possible to its pin without using vias.
- The **VDD12TX1** (pin 110) and **VDD12TX2** (pin 113) pins derive power from the +1.2V supply through a ferrite bead for the two Ethernet blocks. These two pins must be tied together. Be sure to place bulk capacitance on each side of the ferrite bead.
- The **VDD12TX1** and **VDD12TX2** pins should each have one 0.1 µF to 0.01 µF decoupling capacitor. The capacitor size should be SMD_0603 or smaller.

3.5 Ground and Power Connections

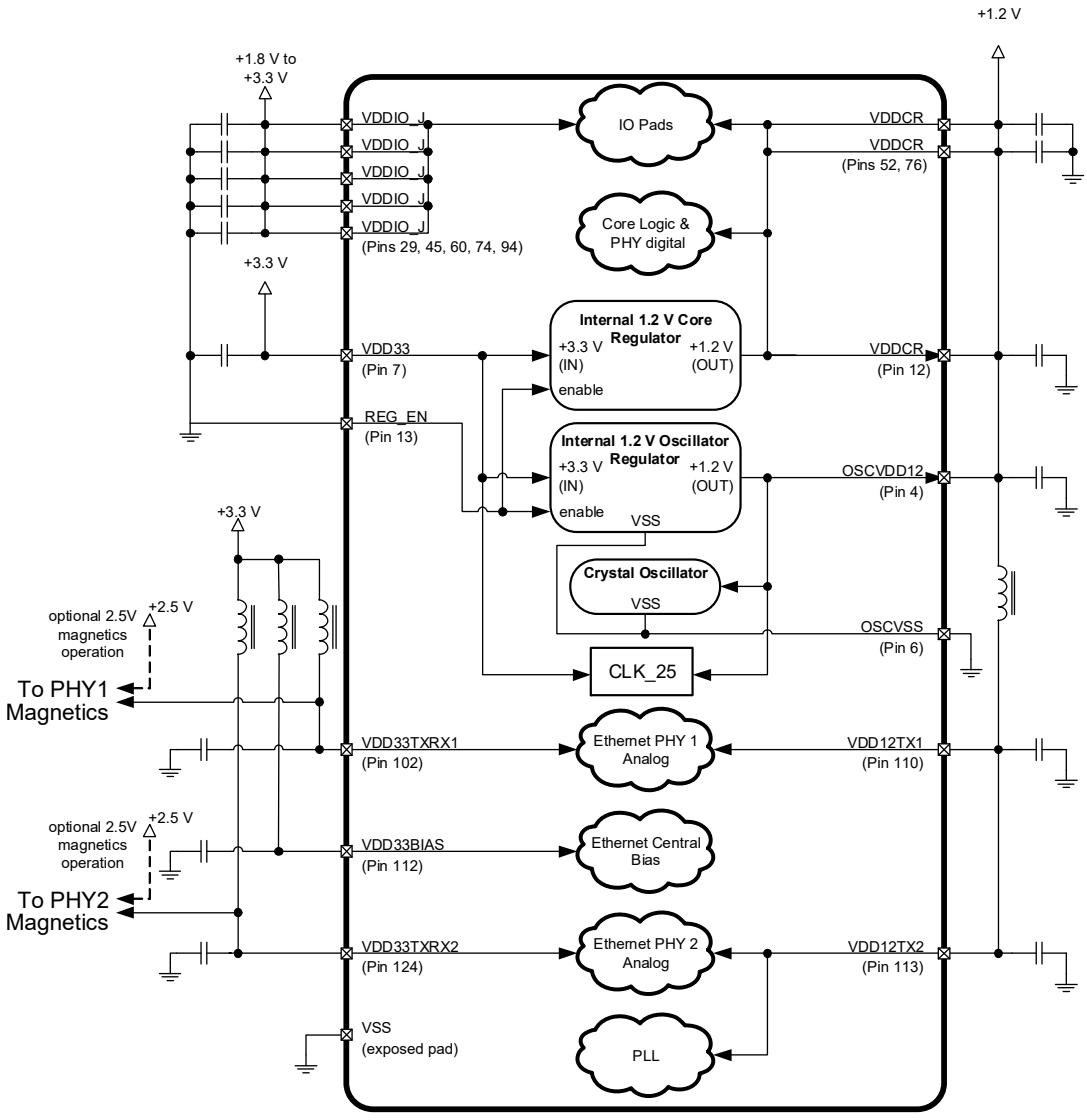
- All grounds, the digital ground pins (**GND**), the core ground pins (**GND_CORE**), and the analog ground pins (**VSS_A**) on the LAN9253 and SAM E53J are all connected internally to the exposed die paddle ground (**VSS**) as system ground. The EDP ground pad on the underside of the LAN9255 must be connected directly to a solid, contiguous ground plane.
- The **GNDANA** (pin 15) must also be connected directly to the contiguous ground plane.
- On the PCB, one system ground is recommended. Running separate digital ground and analog ground planes for any of Microchip's LAN products is not recommended.
- For the power connections of the LAN9253 with its regulators enabled and the regulator disabled, see Figure 3-1 and Figure 3-2.
- For the power connections of the SAM E53J with its regulator in Switching/Linear mode and Linear-Only mode, see Figure 3-3 and Figure 3-4.

FIGURE 3-1: LAN9253 POWER CONNECTION WITH REGULATORS ENABLED (REG_EN PIN PULL-UP)



Note: Bypass and bulk caps as needed for PCB

FIGURE 3-2: LAN9253 POWER CONNECTION WITH REGULATORS DISABLED (REG_EN PIN PULL-DOWN)



Note: Bypass and bulk caps as needed for PCB

- The **OSCVDD12** (pin 4) pin is supplied by one of the internal +1.2V regulators of the LAN9255 and can be left as a no-connection in this mode (REGEN = high). When REGEN = low, this pin must be supplied by an external +1.2V power supply.
- The **OSCVSS** (pin 6) pin should be connected directly to system ground for all applications.
- In addition to having decoupling capacitors, be sure to incorporate enough bulk capacitors (4.7 µF to 22 µF) for each power plane.

FIGURE 3-3: SAM E53J POWER SUPPLY CONNECTION FOR SWITCHING/LINEAR MODE

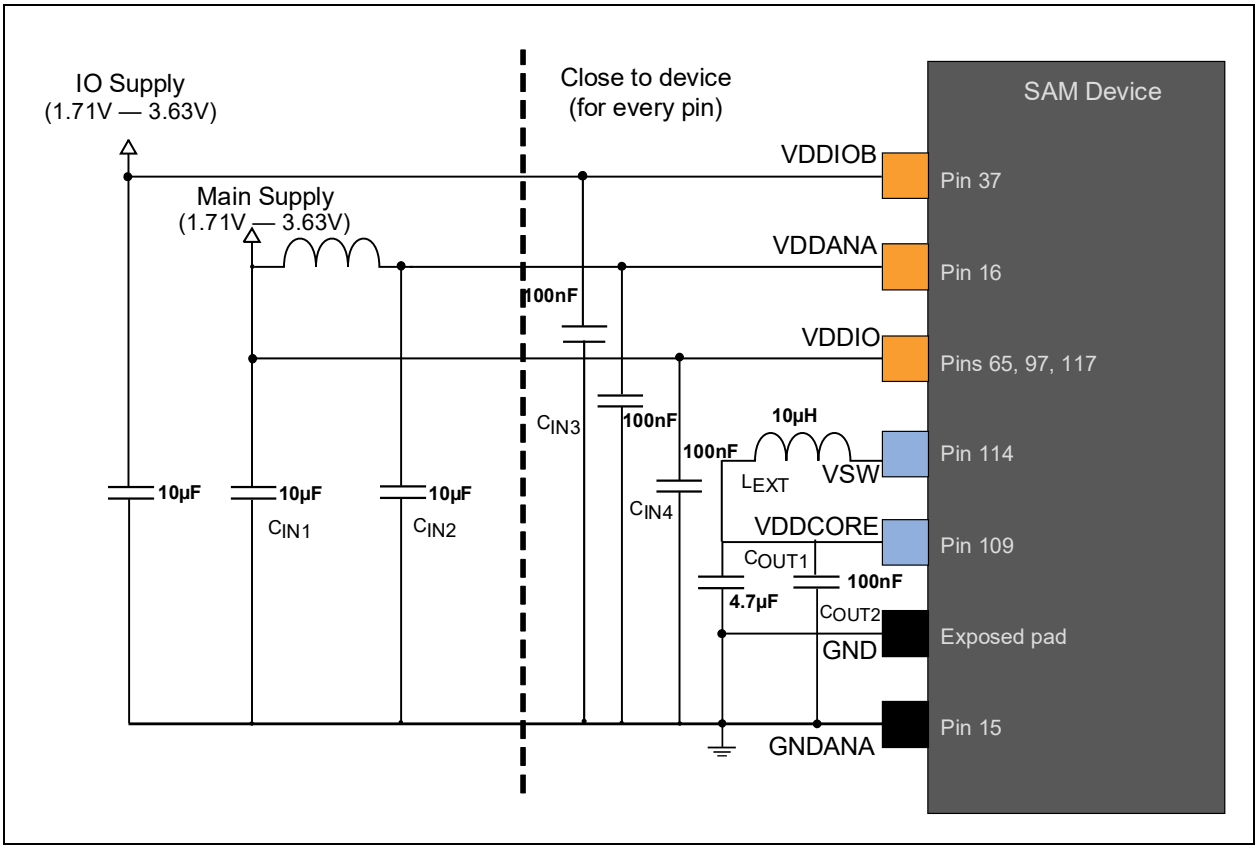
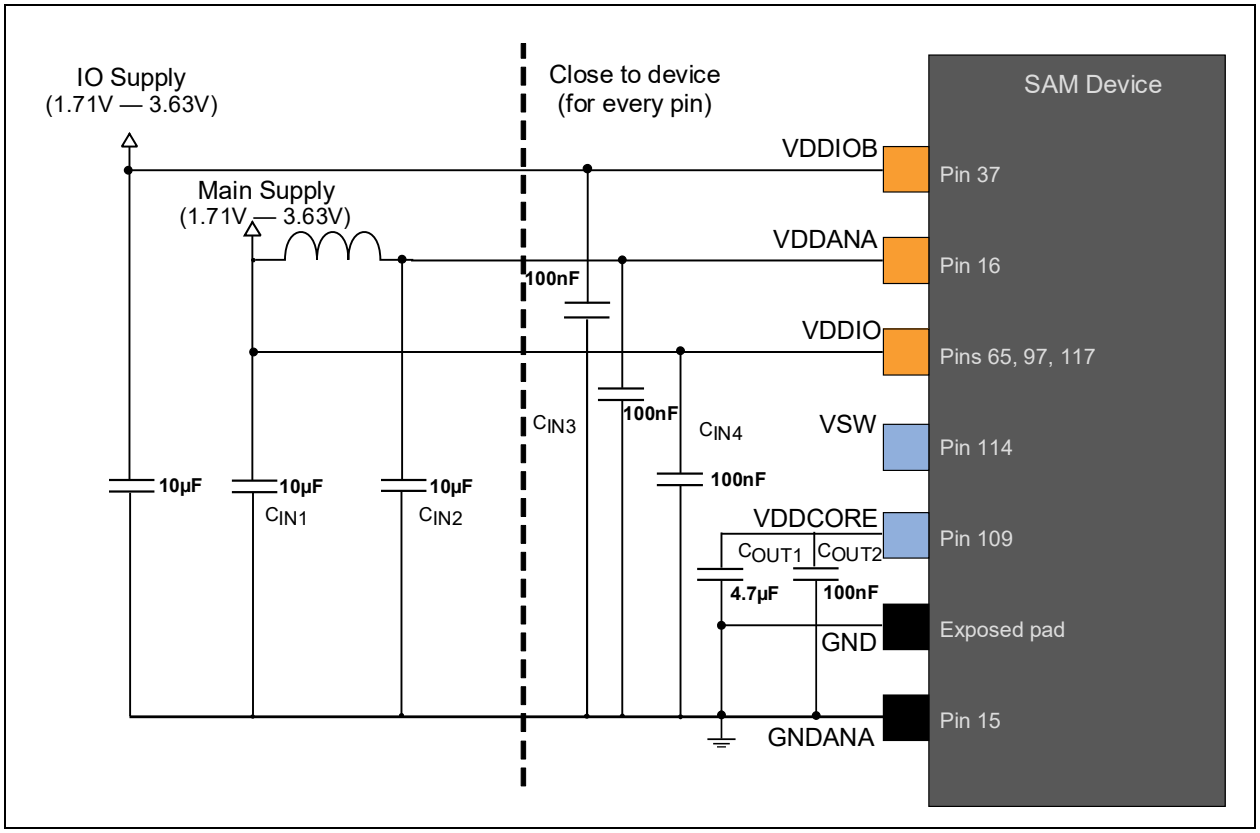


FIGURE 3-4: SAM E53J POWER SUPPLY CONNECTION FOR LINEAR MODE ONLY



3.6 Placing Power Pins in PCB Layout

3.6.1 GROUND CONNECTIONS

- If using the magnetics and RJ45 connector, a chassis ground should be used for the line side of the magnetics and the metal case of the RJ45 connector. The system ground and the chassis ground should be tied together by a component (ferrite bead, resistor, or capacitor). Leave the component out, and the two grounds are separate. Short them together with a zero ohm resistor or short them together with a ferrite bead or a capacitor for best performance. An SMD_0805 or 1210 footprint can be used for the component (ferrite bead, resistor, or capacitor).

3.7 Routing Power Pins in PCB Layout

3.7.1 +3.3V POWER SUPPLY CONNECTIONS

- Route the **VDD33** pin of the LAN9255 directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short and wide as possible.
- Route the VDD33 decoupling capacitor for the LAN9255 power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V and system ground plane) for the capacitor.
- Route the **VDD33TXRX1** pin of the LAN9255 directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short and wide as possible.
- Route the VDD33TXRX1 decoupling capacitor for the LAN9255 power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V and system ground plane) for the capacitor.
- Route directly the VDD33TXRX1 bulk capacitor for the LAN9255 power pins as short as possible to the VDD33TXRX1 power plane.

- Route the **VDD33TXRX2** pin of the LAN9255 directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short and wide as possible.
- Route the VDD33TXRX2 decoupling capacitor for the LAN9255 power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V and system ground plane) for the capacitor.
- Route directly the VDD33TXRX2 bulk capacitor for the LAN9255 power pin as short as possible to the VDD33TX-RX2 power plane.
- Route the **VDD33BIAS** pin (pin 112) of the LAN9255 directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short and wide as possible.
- Route the VDD33BIAS decoupling capacitor for the LAN9255 power pin extremely close to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V and system ground plane) for the capacitor.
- Route the VDD33BIAS bulk capacitor for the LAN9255 power pin extremely close to the VDD33BIAS power plane.
- Place one VDD33TXRX2 decoupling capacitor for the LAN9255 as close to the power pin as possible. Using an SMD_0603 package makes this task easier.

3.7.2 +1.8V TO +3.3V VARIABLE I/O POWER SUPPLY CONNECTIONS

- Route the five **VDDIO** pins of the LAN9255 directly into a solid, +1.8V to +3.3V power plane. The pin-to-plane trace should be as short and wide as possible.
- Route the five VDDIO decoupling capacitors for the LAN9255 power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (VDDIO power plane and system ground plane) for each capacitor.

3.7.3 VDDCR

- The **VDDCR** pins (pins 12, 52, and 76) must be routed with a heavy, wide trace with multiple vias to the three decoupling capacitors and the single bulk capacitor associated with it. All three pins and the capacitors should be routed directly into a solid, +1.2V power plane. The pin-to-plane trace should be as short and wide as possible.
- The **VDD12TX1** (pin 110) and **VDD12TX2** (pin 113) pins must be routed with a heavy, wide trace with multiple vias to the two decoupling capacitors and the single bulk capacitor associated with them. Pins 110 and 113 as well as the capacitors should be routed through the associated ferrite bead directly into a solid, +1.2V power plane (VDDCR).

3.7.4 GROUND CONNECTIONS

- The exposed die paddle (EDP) on the LAN9255 should be connected directly into a solid and contiguous system ground plane. The EDP pad on the component side of the PCB should be connected to the internal system ground plane with 36 power vias in a 6 x 6 grid.
- It is recommended that all ground pins be tied together to the same ground plane. Separate ground planes for **GNDANA** or **OSCVSS** are not recommended.

4.0 ETHERNET/ETHERCAT® SIGNALS

The LAN9255 has two integrated 100 Mbps Ethernet transceivers that are compliant with the IEEE 802.3/802.3u standard and compatible with EtherCAT P.

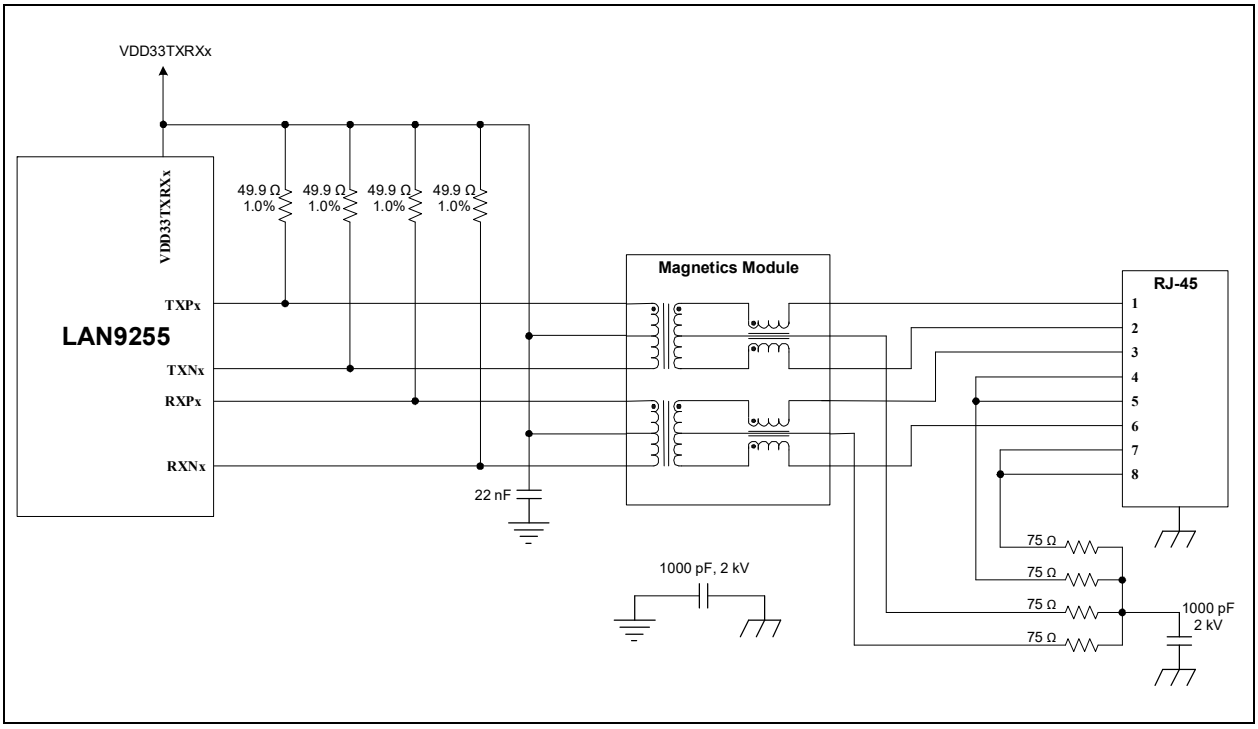
4.1 Copper Port Differential Pair PHY Interface

- Each PHY port has two differential signal pairs. Port A uses pins **TXNA**, **TXPA**, **RXNA**, and **RXPA**, while Port B uses pins **RXPB**, **RXNB**, **TXPB**, and **TXNB**. Configure both ports in the same manner.
- A 100BASE-TX Ethernet magnetics module is required for each port. It may be a discreet device or it may be integrated into the RJ45 jack. The **RX** and **TX** paths must be identical, and the transformer windings must be 1:1. Common-mode chokes should be included on the cable-facing side of the transformer.
- Connect each differential pair of the LAN9255 directly to chip-facing transformer windings of the magnetics module.
- Each of the pins must be individually pulled up to **VDD33TXRX1** (for Port A) or **VDD33TXRX2** (for Port B) with its own 49.9Ω, 1.0% resistor.
- The **TX** and **RX** center tap connections on the LAN9255 side of the magnetics must be connected directly to **VDD33TXRX1** (created from +3.3V). In addition, a 22 nF capacitor is required from the center taps to system ground.
- For added EMC flexibility in an LAN9255 design, the designer may include the option for four low-valued capacitors on the **TXP**, **TXN**, **RXP**, and **RXN** pins. Low-valued capacitors (less than 22 pF) can be added to each line and terminated to system ground. These components can be added to the schematic and should be designated as Do Not Populate (DNP).

4.2 Copper Port Magnetics to RJ45 Connections

- The center tap connections on the cable side of the magnetics should be individually terminated with 75Ω resistors to a common termination point. A 1000 pF, 2 kV capacitor ($C_{magterm}$) connects the common termination point to chassis ground. This is done separately for ports A and B.
- Connect the following RJ45 signals directly to the cable-facing side of the magnetics. Below are the standard connections to the RJ45 jack, but the **TX** and **RX** signals may be swapped if desired.
  - Pin 1 of the RJ45 is **TX**+ and should trace through the magnetics to **TXP** of the LAN9255.
  - Pin 2 of the RJ45 is **TX**– and should trace through the magnetics to **TXN** of the LAN9255.
  - Pin 3 of the RJ45 is **RX**+ and should trace through the magnetics to **RXP** of the LAN9255.
  - Pin 6 of the RJ45 is **RX**– and should trace through the magnetics to **RXN** of the LAN9255.
- Pins 4, 5, 7, and 8 of the RJ45 jack connect to unused wires in CAT-5 type cables. They should be terminated to chassis ground through a 1000 pF, 2 kV capacitor (C_{rjterm}). There are two methods of accomplishing this:
  1. Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor (C_{rjterm}). Repeat for pins 7 and 8 to the same capacitor.
  2. For a lower component count, short RJ45 pins 4 and 5 together and terminate them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor (C_{rjterm}) to chassis ground. Repeat for pins 7 and 8 to the same capacitor.
- If desired, the two 1000 pF capacitors, $C_{magterm}$ and C_{rjterm}, may be combined into a single capacitor. This is commonly done.
- The RJ45 shield should be attached directly to chassis ground.
- For PHY **TX** and **RX** channel connections and termination details, refer to Figure 4-1.

FIGURE 4-1: PHY PORT CONNECTIONS AND TERMINATIONS



4.3 Using RJ45 with Integrated LED

- The user can utilize the RJ45 connector with integrated LED components if the product working environment is not very noisy.
- If the designed product operates in an electrically noisy outside environment, using RJ45 with integrated LED components is not recommended. This is because the outside interference signal or voltage could be coupled to the LED circuit through the line side of RJ45 due to the LED circuit that is directly connected to chip and system power or ground. It is better to use independent LED components.
- If the user needs to utilize the RJ45 with an integrated LED circuit in a noisy environment, consider adding TVS diodes to protect the chip.

4.4 Placing Copper Ports in PCB Layout

4.4.1 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS INTERFACE

- If the Auto-MDIX functionality is enabled, place the 49.9Ω TX termination pull-up (**TXPA** and **TXPB** pins) as close as possible to the LAN9255. If the Auto-MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
- If the Auto-MDIX functionality is enabled, place the 49.9Ω TX termination pull-up (**TXNA** and **TXNB** pins) as close as possible to the LAN9255. If the Auto-MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
- Place the 49.9Ω RX termination pull-up (**RXPA** and **RXPB** pins) as close as possible to the LAN9255.
- Place the 49.9Ω RX termination pull-up (**RXNA** and **RXNB** pins) as close as possible to the LAN9255.
- Place the four optional, low-valued, Common-mode capacitors for each differential signal as close as possible to the magnetics. They should be placed to create the smallest possible stub.

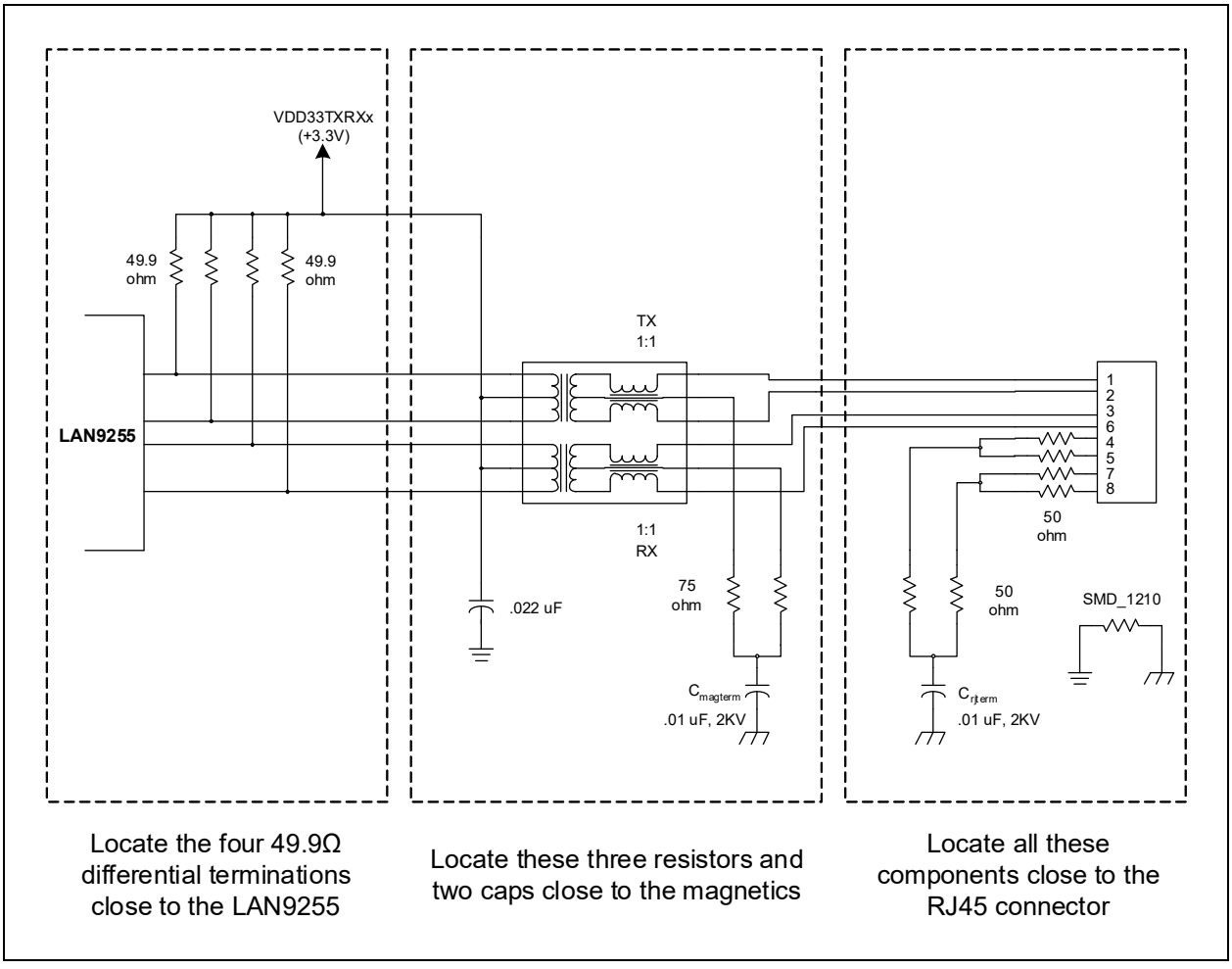
4.4.2 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS THROUGH MAGNETICS

- Place the 0.022 µF TX/RX channel center tap termination capacitor as close as possible to the magnetics.
- Place the 75Ω cable side center tap termination resistors and the 1000 pF, 2 kV capacitor ($C_{magterm}$) cap as close as possible to the magnetics.

4.4.3 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS THROUGH MAGNETICS TO RJ45 CONNECTORS

- Place the RJ45 connector, the magnetics, and the LAN9255 next to each other. If this is not possible, keep the RJ45 connector and the magnetics as close as possible.
- Strategically select and place the magnetics to set up the best routing scheme from the LAN9255 to the magnetics and to the RJ45 connector. There are many styles and sizes of magnetics with different pinouts to facilitate this operation. Investigate Tab-Up and Tab-Down RJ45 connectors in order to facilitate layout.
- Place the unused wire pair termination resistors and the 1000 pF, 2 kV capacitor (C_{rjterm}) extremely close to the RJ45 connector.
- Make sure not to place any other components in or near the TX channel and RX channel lanes of the PCB. These lanes should be clear of any other signals and components.
- For the placement of copper ports from LAN9255 to the magnetics and RJ45 connector, refer to Figure 4-2.

FIGURE 4-2: COMPONENTS PLACEMENT FOR COPPER PORTS



4.5 Routing Copper Ports in PCB Layout

4.5.1 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS INTERFACE

- The traces connecting the TX outputs (**TXPA** and **TXNA** pins, or **TXPB** and **TXNB** pins) to the magnetics must be run as differential pairs. The differential impedance should be 100Ω.
- The traces connecting the RX inputs (**RXPA** and **RXNA** pins, or **RXPB** and **RXNB** pins) from the magnetics must be run as differential pairs. The differential impedance should be 100Ω.
- For differential traces running from the LAN PHY to the magnetics, Microchip recommends routing these traces on the component side of the PCB with a contiguous system ground plane on the next layer. This minimizes the use of vias and avoids impedance mismatches by switching PCB layers.
- The **VDD33TXRX1** of Port A and the **VDD33TXRX2** of Port B power supply should be routed as a mini-plane. They can be routed on an internal power plane layer.

4.5.2 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS THROUGH MAGNETICS

- The traces connecting the TX outputs from the magnetics to pins 1 and 2 on the RJ45 connector must be run as differential pairs. The differential impedance should be 100Ω.
- The traces connecting the RX inputs on the magnetics from pins 3 and 6 on the RJ45 connector must be run as differential pairs. The differential impedance should be 100Ω.
- For differential traces running from the magnetics to the RJ45 connector, Microchip recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This minimizes the use of vias and unwanted noise from coupling into the differential pairs. The plane clear-out boundary is usually halfway through the magnetics.

4.5.3 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS THROUGH MAGNETICS TO RJ45 CONNECTORS

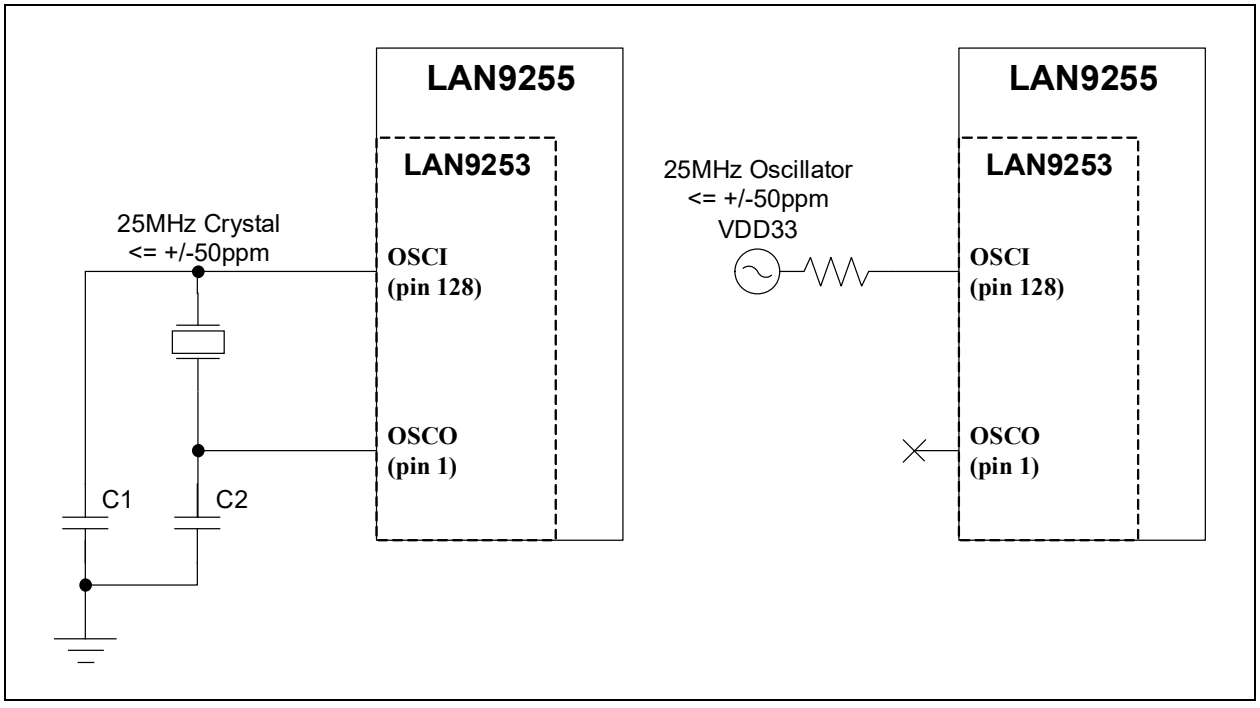
- Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and may cause EMC problems.
- The construction of a separate chassis ground that can be easily connected to system ground at one point is also recommended. This plane provides the lowest impedance path to earth ground.

5.0 CLOCK CIRCUIT

5.1 LAN9253 Crystal or Oscillator Clock Connections

- The LAN9253 requires a 25.000 MHz reference clock. This is most commonly generated from a crystal, but a single-ended 25.000 MHz clock from an oscillator or other source may be substituted.
- If a crystal is used, connect it between **OSCI** (pin 128) and **OSCO** (pin 1). Additional shunt and series resistors are not required. See Figure 5-1.
- Full crystal specifications may be found in the *LAN9253 Data Sheet*. The minimum crystal drive level specification is 300 µw.
- Load capacitors should be installed from **OSCI** to ground, and from **OSCO** to ground. The capacitor value is determined from the C_L specification of the crystal. The equation is: $C_1 = C_2 = 2 * (C_L – C_{stray})$. C_{stray} is the stray board capacitance plus the OSCI/OSCO pin capacitance. It varies based on board layout, but a typical value is between 5 pF and 6 pF.
- As an alternative to a crystal, a 25.000 MHz oscillator may be used to provide the clock source for the LAN9253. Connect a single-ended clock source to **OSCI** (pin 128), and leave **OSCO** (pin 1) floating as No Connect (NC). The clock source supply voltage should be between 1.5V and 3.3V. See Figure 5-1.
- **Design Verification Tip:** Microchip recommends taking advantage of the Clock Output Test mode in the LAN9253. In order to facilitate system-level validation and debugging, the crystal clock can be enabled onto the **IRQ** pin by setting the IRQ Clock Select (IRQ_CLK_SELECT) bit of the Interrupt Configuration Register (IRQ_CFG). The **IRQ** pin should be set to a push-pull driver by using the IRQ Buffer Type (IRQ_TYPE) bit for best results. Be sure to include a test pin on the **IRQ** (pin 88) pin and a ground pin close to the test pin. Note that depending on how the LAN9253 is configured, 25 MHz output clocks may also be accessed on the **CLK_25** or **MII_CLK25** pins. Using a high-quality and precise frequency counter with 8-digits or more will accurately determine the frequency of the 25.000 MHz in the design. Adjusting the crystal circuit load caps slightly will fine tune the frequency of the circuit.

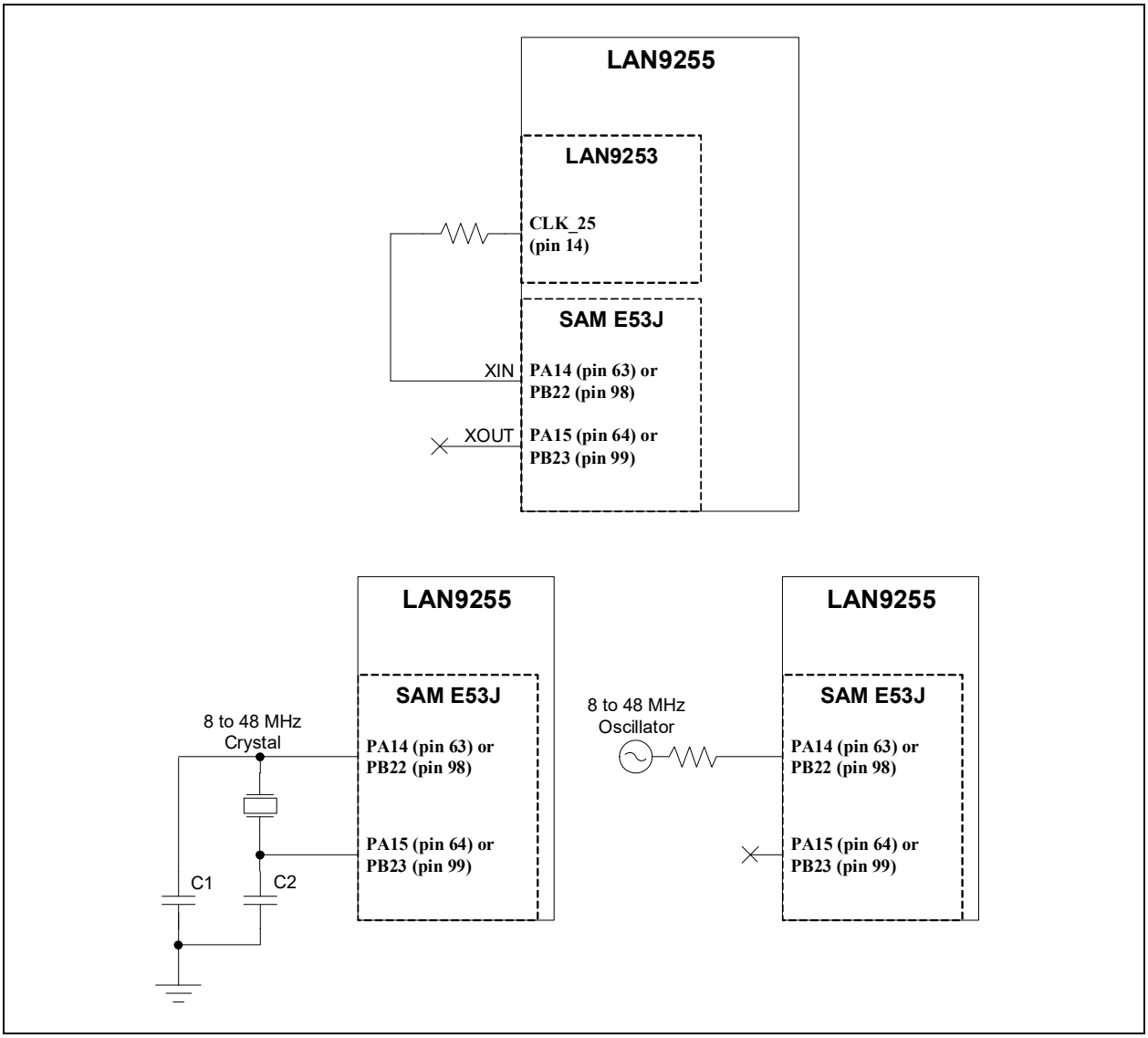
FIGURE 5-1: LAN9253 CRYSTAL OR OSCILLATOR CONNECTIONS



5.2 SAM E53J Crystal or Oscillator Clock Connections

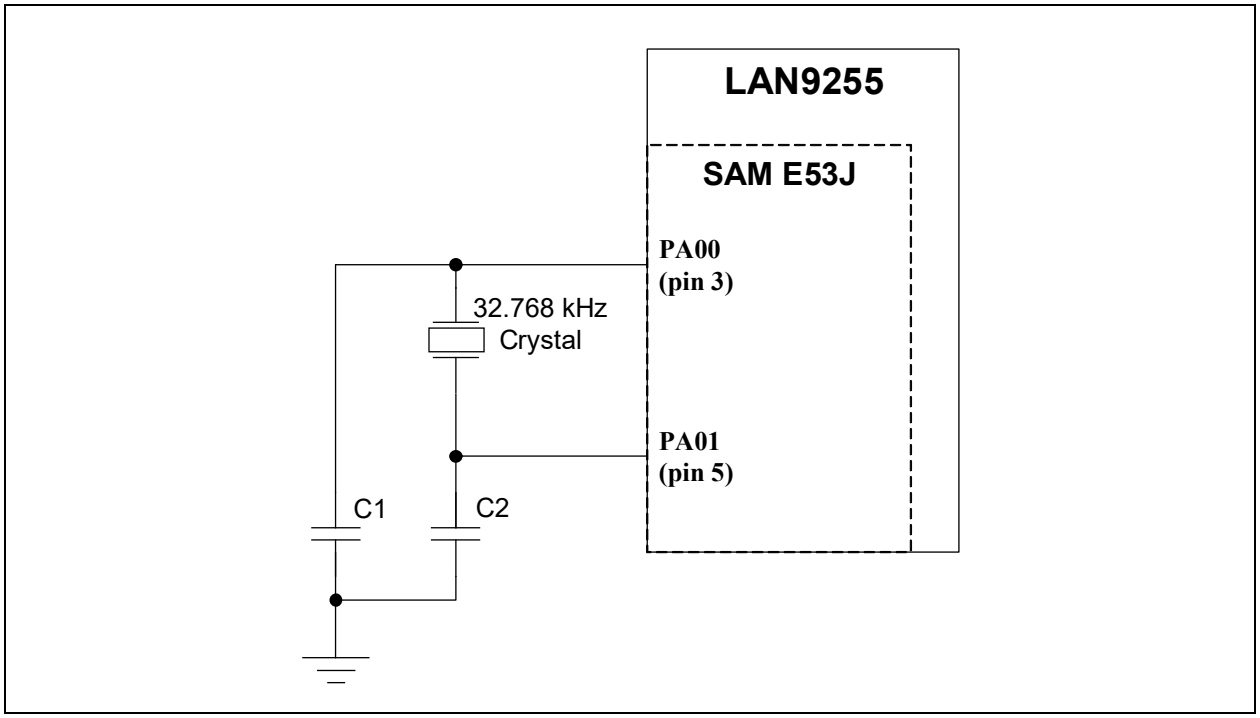
- The SAM E53J requires an 8 MHz to 48 MHz crystal or single-ended clock as its primary reference clock. The **XIN/XOUT** pair may be either **PA14** (pin 63) and **PA15** (pin 64), or **PB22** (pin 98) and **PB23** (pin 99). See Figure 5-2.
- The simplest way to clock the SAM E53J is from the **CLK_25** output of the LAN9253. Connect **CLK_25** (pin 14) to either **PA14** or **PB22**. Use a series resistor (approximately 22Ω) for impedance matching and EMI control.
- Alternatively, connect an 8 MHz to 48 MHz crystal between the **XIN** and **XOUT** pins. Connect load capacitors to each pin. Refer to the discussion in Section 5.1, "LAN9253 Crystal or Oscillator Clock Connections" about calculating the capacitor values. See the *SAM D5x/E5x Family Data Sheet* for crystal specifications.
- Alternatively, connect an external single-ended clock source, such as an oscillator, to the **XIN** pin (**PA14** or **PB22**). Leave the corresponding **XOUT** pin (**PA15** or **PB23**) unused. The clock source supply voltage should be the same as **VDDIO_S.**
- The **XIN/XOUT** pair that is not used for the reference clock may be used for other purposes.

FIGURE 5-2: SAM E53J MHZ CRYSTAL OR OSCILLATOR CONNECTION OPTIONS



- The SAM E53J may optionally use a 32.768 kHz crystal as clock source for the Real-Time counter.
- **PA00** (pin 3) is the **XIN32** pin, and **PA01** (pin 5) is the **XOUT32** pin. Connect a 32.768 kHz crystal between these pins, and connect load capacitors to each pin. Refer to the discussion in Section 5.1, "LAN9253 Crystal or Oscillator Clock Connections" about calculating the capacitor values. This is shown in Figure 5-3.
- Refer to the *SAM D5x/E5x Family Data Sheet* for crystal specifications.

FIGURE 5-3: SAM E53J 32KHZ CRYSTAL CONNECTIONS



5.3 Other Clock Pins

- **CLK_25/CLK_25_EN/XTAL_MODE** (pin 14) is an additional 25 MHz clock output of the LAN9253 intended to provide 25 MHz crystal clock for an external device. It is suggested to use this output to clock the SAM E53J as described in Section 5.2, "SAM E53J Crystal or Oscillator Clock Connections". Alternatively, it may be used as a reference clock to a PHY connected to the LAN9253 MII bus or to the SAM E53J RMII bus. If it is needed to drive more than one load, a clock buffer chip should be used.
- This pin is also used for configuration strapping. It determines the mode of the LAN9253 **OSCI** pin and whether the **CLK_25** output is enabled. The following are three possible configuration strapping cases:
  - If the 25 MHz clock output is not needed, connect pin 14 to ground directly to disable the 25 MHz clock output on pin 8 **CLK_25**.
  - If **CLK_25** is to be used, a resistor voltage divider of two equal resistors can be used to set a 1.5V voltage level on **CLK_25_EN** to enable 25 MHz output from pin 14 **CLK_25**. Typical resistor values are 1 kΩ to 10 kΩ. If a clock input to **OSCI** is used instead of a crystal, see the next case.
  - If two LAN9255 with 25 MHz clock are used in the clock daisy chaining configuration with the **CLK_25** of the previous devices as the input clock source, or if any other external clock is driving **OSCI**, then **OSCI** should be set to Schmitt Trigger Input mode via the pin 14 **XTAL_MODE** strap-in by a pull-up resistor to **VDD33**. Use 1 kΩ to 10 kΩ.

5.4 Placing and Routing Crystal in PCB Layout

- Place the 25.000 MHz crystal and the associated load capacitors extremely close to each other and to the LAN9255 (**OSCI** and **OSCO** pins). They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, and so on.)
- Place all the crystal components on the component side of the PCB with a system ground plane layer on the next layer. This minimizes vias in the circuit connections and assures that all the crystal components are referenced to the same reference plane.
- The routing for the crystal or clock circuitry should be kept as small and short as possible.
- A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the system ground plane directly below it.

6.0 CONFIGURATION FOR SYSTEM APPLICATIONS

The LAN9255 applications can be divided into the following modes. Refer to Figure 6-11 for details.

- Microcontroller mode with SPI/SQI interface
- Expansion mode with MII to External PHY

6.1 Microcontroller Mode with SPI/SQI Interface

- The device can be accessed via SPI/SQI with MCU while also providing up to 16 inputs or outputs for general purpose usage. An SPI/SQI (Quad SPI) client controller provides a low pin count synchronous interface that facilitates communication between the device and a host system.
- The SPI/SQI connection between the MCU and the EtherCAT device facilitates the transferring of the data information between the host MCU and the EtherCAT device.

6.2 Expansion Mode with MII to External PHY

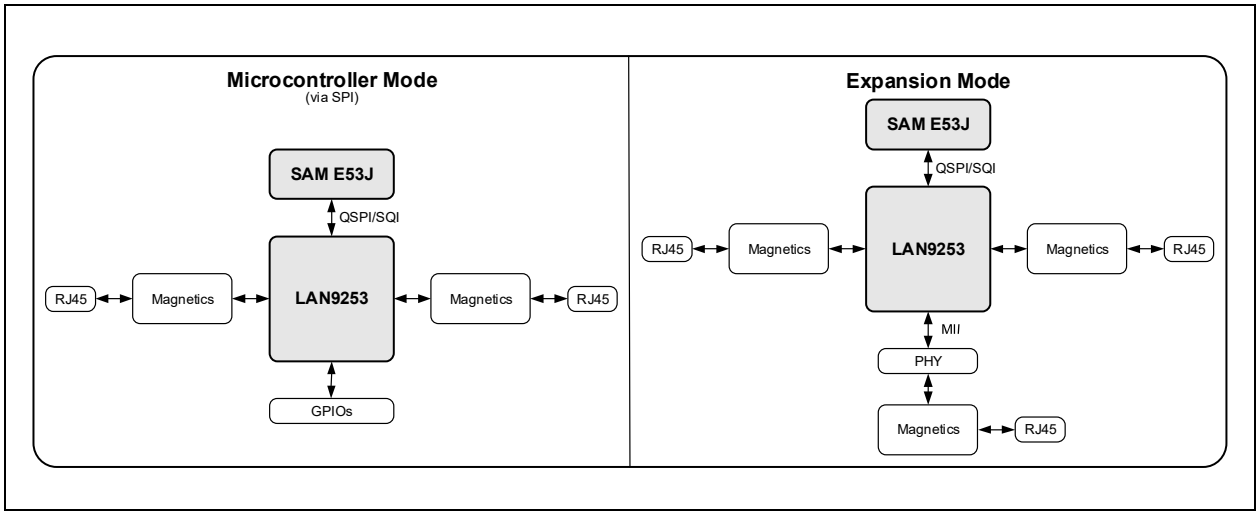
- While the device is in SPI/SQI mode, a third networking port can be enabled to provide an additional MII port. This port can be connected to an external PHY to enable star or tree network topologies, or to another LAN9255 to create a four-port solution. This port can be configured for upstream or downstream direction.

6.3 Unused Application Modes

The LAN9253 has additional modes that do not make sense in the context of LAN9255, which includes a SAM E53J MCU with SPI/SQI capability. The two unused modes are the following:

- **Microcontroller mode with Host Bus Interface (HBI)**. The integrated Host Bus Interface supports 8/16-bit operation with big, little, and mixed endian operations. The HBI connection between the MCU and EtherCAT device facilitates the transferring of data information between the host MCU and the EtherCAT device.
- **Digital I/O mode**. For simple digital modules without MCU, the LAN9253 can operate in Digital I/O mode where 16 digital signals can be controlled or monitored by the EtherCAT host. Up to seven control signals are also provided.

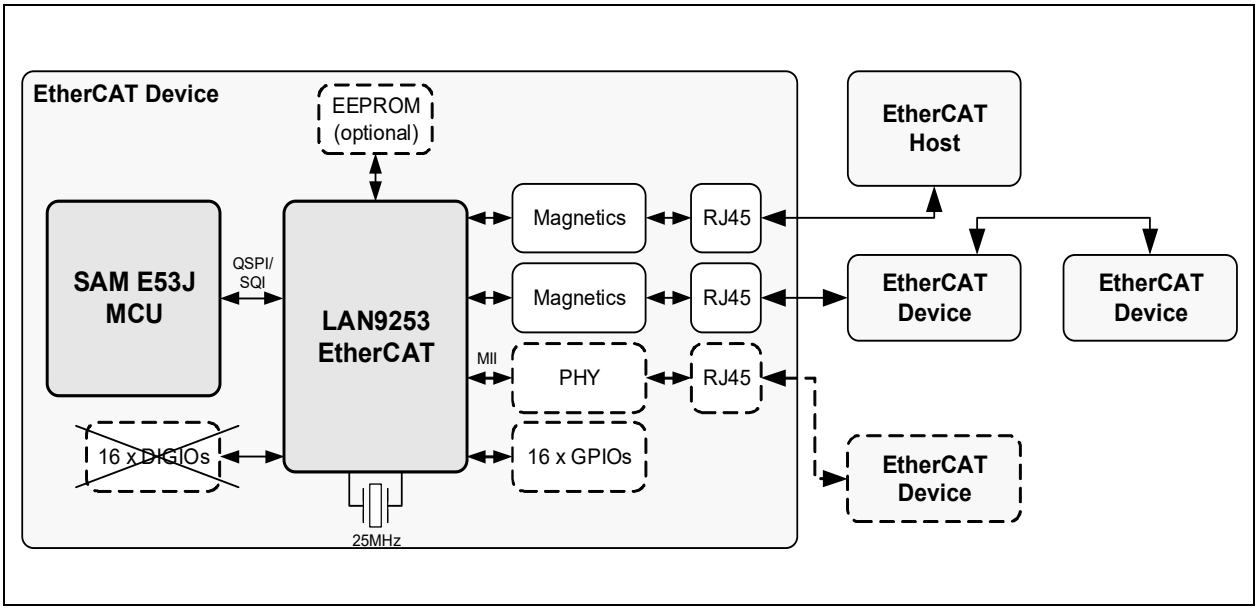
FIGURE 6-1: LAN9253 MODES OF OPERATION



6.4 System Block Diagram

- The complete system application block diagram is illustrated in Figure 6-2.
- The SAM E53J should be connected via the QSPI/SQI bus to the LAN9253.
- An EEPROM is optional.
- Port 0 (Port A) connects to EtherCAT host in 3-port Downstream mode.
- Port 1 (Port B) connects to EtherCAT device in 3-port Downstream mode.
- Port 2 MAC MII optionally connects an external PHY to another EtherCAT device.

FIGURE 6-2: SYSTEM BLOCK DIAGRAM

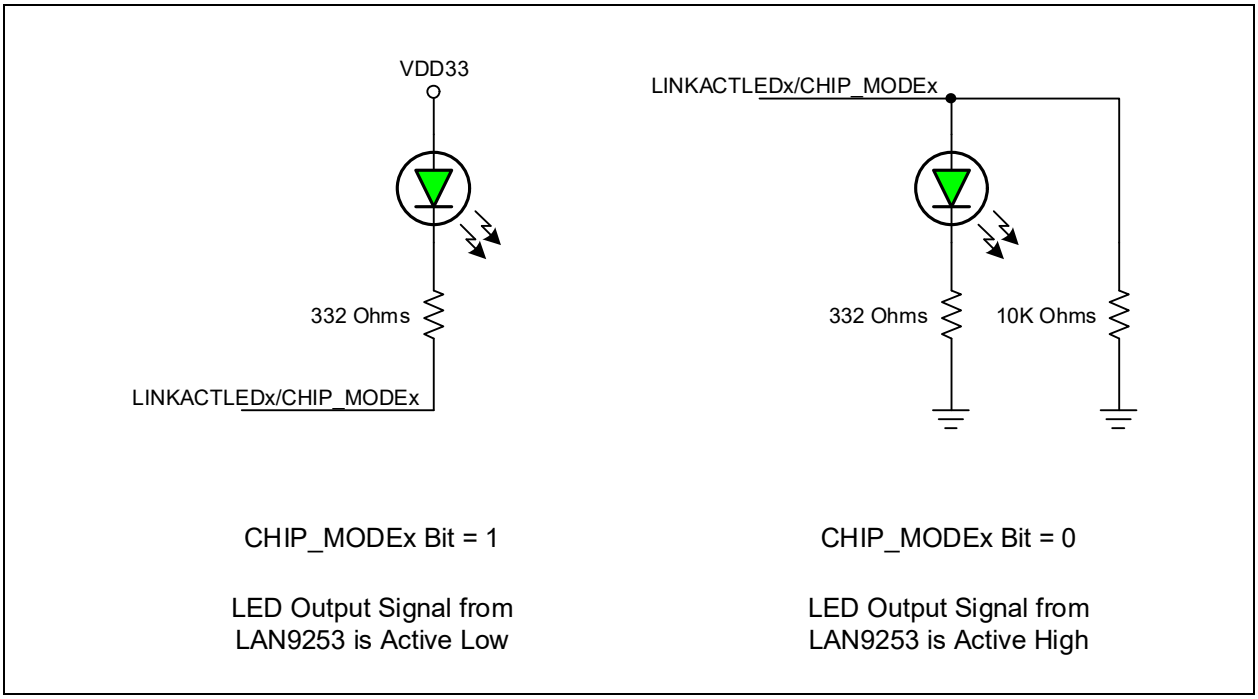


- **CHIP_MODE1** (pin 90) and **CHIP_MODE0** (pin 95) pins configure the number of active ports and port types of the LAN9253. The configuration modes are shown in Table 6-1, and the strapping is shown in Figure 6-3.

TABLE 6-1: LAN9253 MODE SELECTION

CHIP_MODE [1:0]	Mode	Description
0x	2-Port mode	Port 0 = PHY A, Port 1 = PHY B Ports 0 and 1 are connected to internal PHYs A and B.
10	3-Port Down-stream mode	Port 0 = PHY A, Port 1 = PHY B, Port 2 = MII Ports 0 and 1 are connected to internal PHYs A and B. Port 2 is connected to the external MII pins.
11	3-Port Upstream mode	Port 0 = MII, Port 1 = PHY B, Port 2 = PHY A Ports 2 and 1 are connected to internal PHYs A and B. Port 0 is connected to the external MII pins.

FIGURE 6-3: STRAPPING FOR LED/CHIP_MODEX

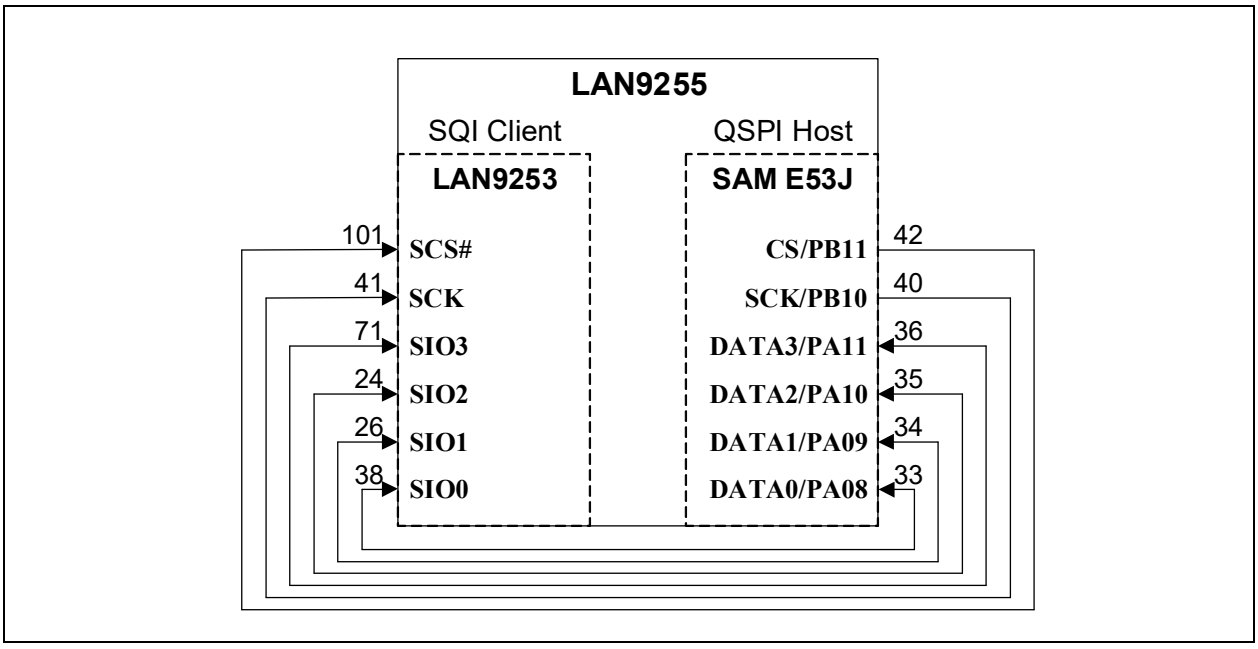


7.0 MICROCONTROLLER MODE VIA SPI/SQI INTERFACE

7.1 QSPI/SQI Host-to-Client Connection

- The connection between SAM E53J QSPI/SQI Host mode and LAN9253 SQI Client mode is the primary interface between these two devices. These connections must be made at the board level via the pins of the LAN9255 since there are no chip-to-chip connections within the LAN9255 package.
- Since the connections between the pins are very short, series resistors are not needed for signal integrity purposes. However, a series resistor may be desired on the clock signal for reducing radiated emissions. Details are shown in Figure 7-1.

FIGURE 7-1: QSPI/SQI CONNECTION BETWEEN SAM E53J AND LAN9253



8.0 EXPANSION MODE WITH MII INTERFACE FOR EXTRA PORT

8.1 MII Signals and Connections

When connecting an external MII PHY to the LAN9253, refer to the proper connections for the 14 signals in Table 8-1.

TABLE 8-1: LAN9255 MII SIGNALS TO EXTERNAL PHY

From	Connects to	Location of Series Resistors
LAN9255	**MII PHY Device**	
MII_RXD0 (pin 55)	RXD<0>	Near PHY
MII_RXD1 (pin 56)	RXD<1>	Near PHY
MII_RXD2 (pin 58)	RXD<2>	Near PHY
MII_RXD3 (pin 59)	RXD<3>	Near PHY
MII_RX_DV (pin 54)	RX_DV	Near PHY
MII_RX_ER (pin 66)	RX_ER	Near PHY
MII_RXCLK (pin 72)	RX_CLK	Near PHY
MII_TXD0 (pin 50)	TXD<0>	Near LAN9255
MII_TXD1 (pin 49)	TXD<1>	Near LAN9255
MII_TXD2 (pin 32)	TXD<2>	Near LAN9255
MII_TXD3 (pin 31)	TXD<3>	Near LAN9255
MII_TX_EN (pin 51)	TX_EN	Near LAN9255
MII_MDIO (pin 80)	MDIO	Pull-up resistor
MII_MDC (pin 78)	MDC	Near LAN9255

8.2 MII Interface for EtherCAT® Device

- **TX_CLK** from the external PHY is not connected since the EtherCAT device does not incorporate a TX FIFO. The TX signals from the EtherCAT device may be delayed with respect to the **CLK25** output by using TX shift compensation so that they align properly as if they were driven by the **TX_CLK** of the PHY.
- The **COL** and **CRS** outputs from the PHY are not connected since EtherCAT operates in Full-Duplex mode.
- The **TX_ER** input on the external PHY should be tied to ground as the EtherCAT device never generates any transmit errors.

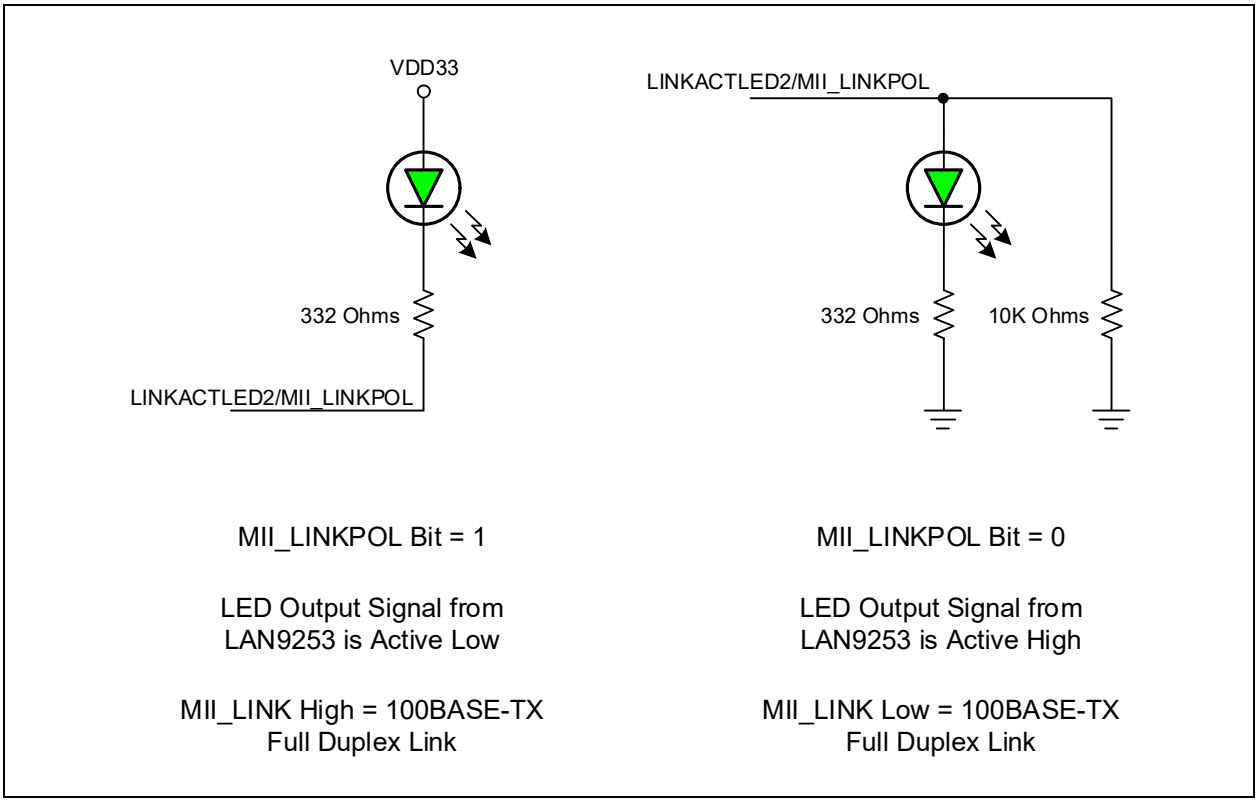
8.3 MII Interface Series Terminations

Provisions should be made for series resistors for all outputs on the MII/RMII interface. Series resistors enable designers to closely match the output driver impedance of the LAN9255 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors is 22Ω.

8.4 Other Pins Related to MII Interface

- **MII_CLK25** (pin 53) is a free-running 25 MHz clock that can be used as the clock input to the external PHY.
- **MII_LINK** (pin 100) is an input pin on the LAN9255 that is driven by the external PHY to indicate that a 100 Mbps full-duplex link is established. The polarity is configurable via the MII_LINKPOL strap.
- The **TX_SHIFT1** (pin 31) and **TX_SHIFT0** (pin 32) pins configure the value of the MII TX timing shift for the MII port of the LAN9255. The shifts in timing are as follows:
  - 00 = 20 ns
  - 01 = 30 ns
  - 10 = 0 ns
  - 11 = 10 ns
- See the *LAN9253 Data Sheet* for complete details. If MII is used, it is suggested to have both external pull-up and pull-down resistor options for both pins for complete flexibility. A typical value is 4.7 kΩ. If MII is not used, external resistors are not needed on these pins.
- The **MII_LINKPOL** (pin 57) strap pin configures the polarity of the **MII_LINK** pin (pin 100). When latched low, MII_LINK low indicates a 100BASE-TX full-duplex link has been established. When latched high, MII_LINK high indicates a 100BASE-TX full-duplex link has been established. This pin has a weak internal pull-up and can be driven low with an external 1.0 kΩ resistor to system ground.

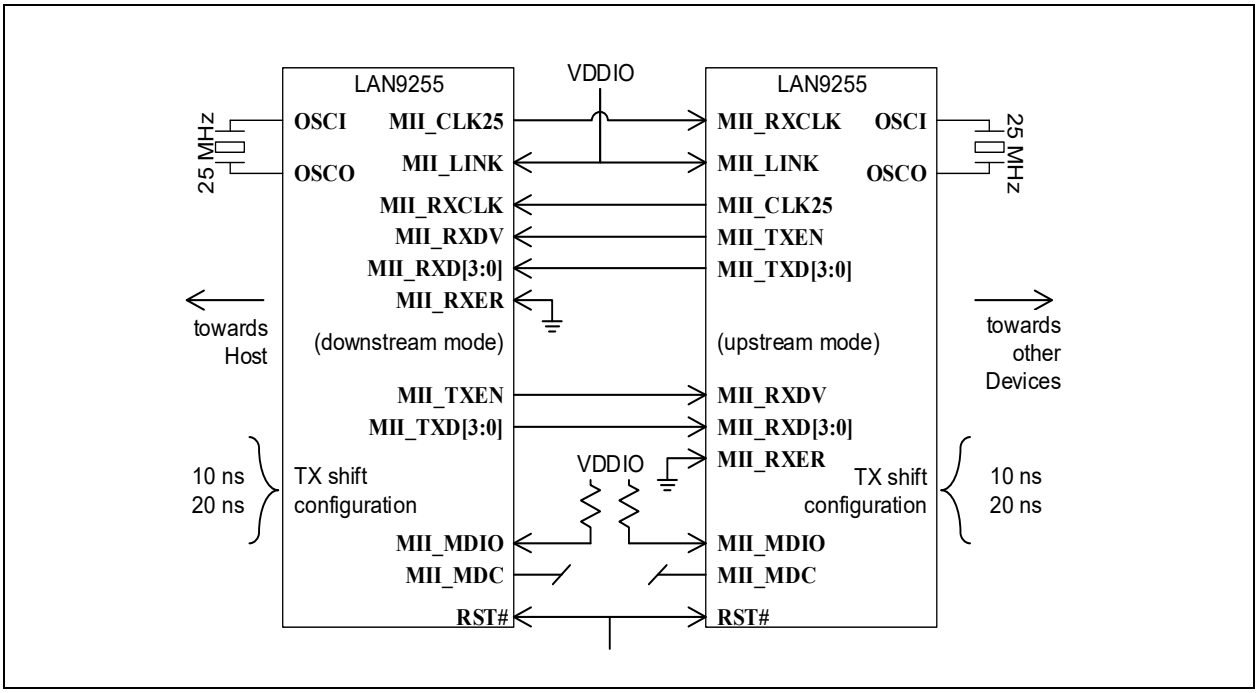
FIGURE 8-1: LED ACTIVE-LOW/HIGH CIRCUITS



8.5 MII Back-to-Back Connections

- Two EtherCAT devices can be connected using a back-to-back MII connection as shown in Figure 8-2. One device is placed in 3 Port Upstream mode and the other in 3-Port Downstream mode.
- The clock sources of each EtherCAT device may be different. The 25 MHz output (**MII_CLK25**) is provided for one device to drive the **RX_CLK** input to the other device.
- The TX signals from each EtherCAT device may be delayed with respect to the **CLK25** output by using TX shift compensation so that they align properly to meet the RX timing requirement of the other device.
- The MII_RXER signals are not used since the EtherCAT devices never generate errors.

FIGURE 8-2: ETHERCAT® BACK-TO-BACK MII CONNECTION



8.6 Placing and Routing in PCB Layout for MII Interface

- If the designer has determined that series terminations are required, they should be placed appropriately. Any series termination should be placed as close as possible to the associated driver of the MII signal.
- The value of the series termination (if utilized) and the impedance of the internal driver of the LAN9255 should roughly equal that of the PCB trace impedance. The value of the series termination can be adjusted slightly to achieve the best signal integrity possible. (Using 22Ω to 33Ω series termination resistors is recommended.)
- If all traces lengths of the MII signals are less than one inch (2.5 cm) long, the series termination resistors can be ignored because the short traces have not formed the transmission line yet.

9.0 EEPROM INTERFACE

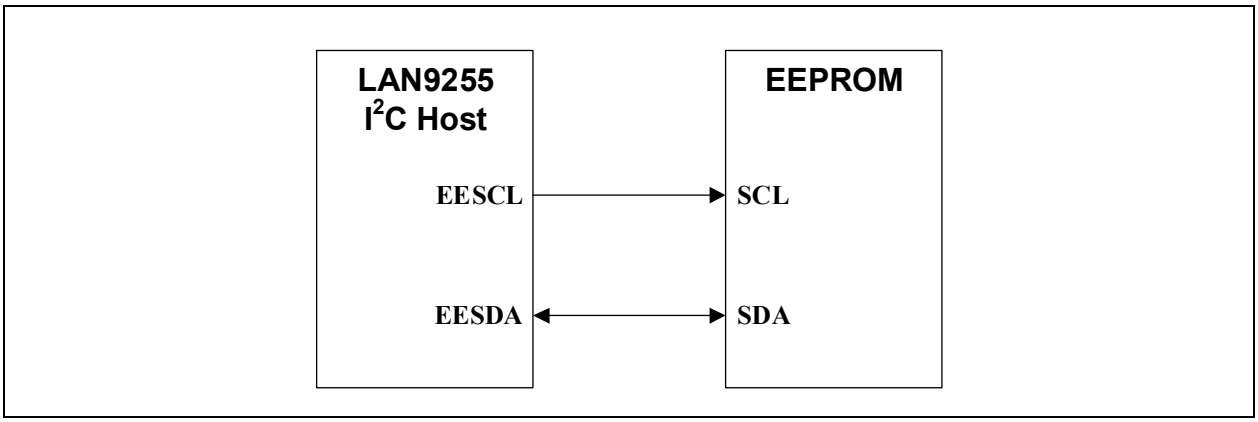
The LAN9255 contains an I^2C host controller for connection to an external EEPROM. EtherCAT requires an EEPROM, but the LAN9253 also supports EEPROM Emulation, by which the MCU emulates an EEPROM. EEPROM Emulation mode is described in Section 9.3, "EEPROM Emulation Mode".

The EEPROM interface uses the **EESCL** and **EESDA** pins. **EESCL** and **EESDA** require an external pull-up resistor. Both 1 byte and 2 byte addressed EEPROMs are supported. The size is determined by the **E2PSIZE** configuration strap.

9.1 EEPROM Pins

- **EESDA** (pin 82): When the device is accessing an external EEPROM, this pin is the I^2C serial data input/open-drain output. Note that this pin must be pulled-up by a 10 kΩ external resistor.
- **EESCL** (pin 83): When the device is accessing an external EEPROM, this pin is the I^2C clock open-drain output. Note that this pin must be pulled-up by a 10 kΩ external resistor.
- Please review the EEPROM Configurable Register section in the *LAN9253 Data Sheet* for the specific EEPROM functionality.
- The connection to an EEPROM is shown in Figure 9-1.

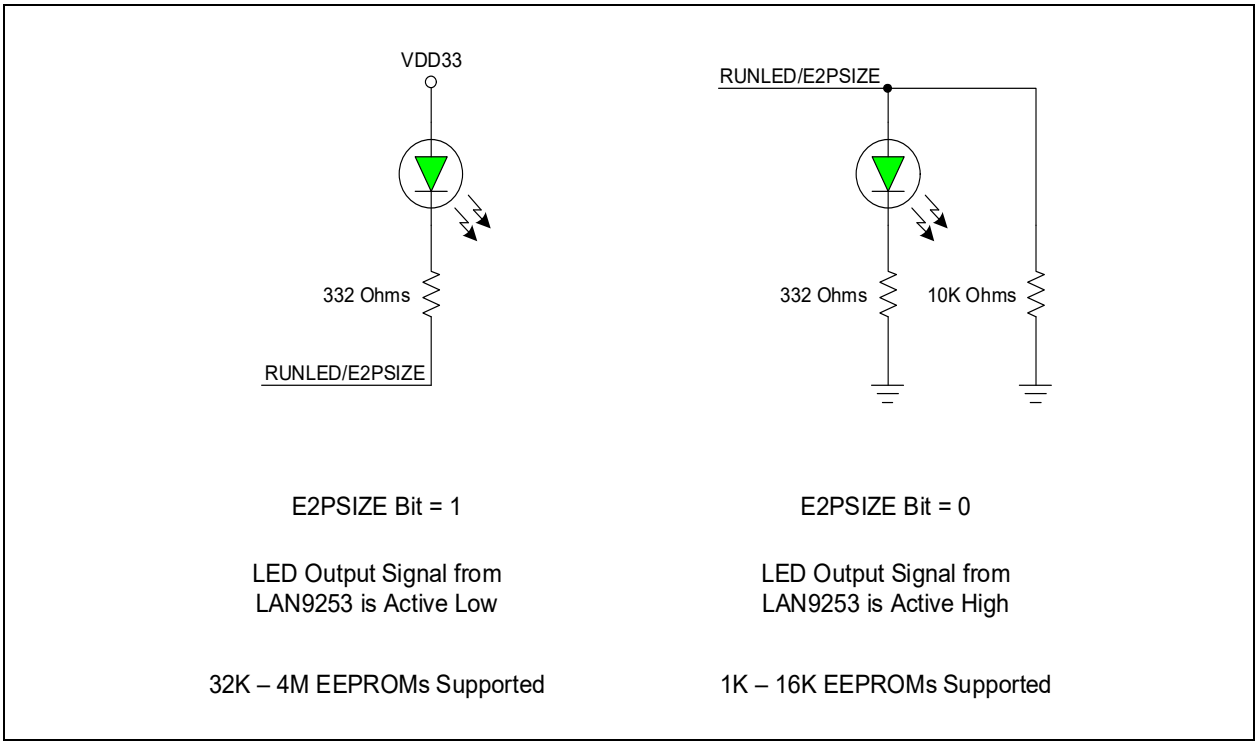
FIGURE 9-1: CONNECTION BETWEEN LAN9255 AND EEPROM



9.2 EEPROM Related Strapping Pin

- **E2PSIZE** (pin 89): This strap pin configures the I^2C EEPROM size.
  - When latched low, EEPROM sizes 128 x 8-bit (1K) through 2048 x 8-bit (16K) are supported.
  - When latched high, EEPROM sizes 4096 x 8-bit (32K) through 512K x 8-bit (4M) are supported.
- This pin has a weak internal pull-up and can be driven low with an external 1.0 kΩ resistor to ground.
- The connection is shown in Figure 9-2.

FIGURE 9-2: E2PSIZE STRAPPING OPTIONS



9.3 EEPROM Emulation Mode

- LAN9255 can be configured to EEPROM Emulation mode to eliminate the need for an EEPROM, therefore reducing systems cost.
- For normal EEPROM operation, the **EE_EMUL2** or **EE_EMUL1** configuration straps should include an external pull-up.
- Strap **EE_EMUL [2:0]** (pins 83, 82, and 89) to select the appropriate mode:
  - 000: SPI
  - 001: HBI Indexed 16-bit EtherCAT Direct Mapped
  - 010: HBI Multiplexed 1 Phase 16-bit EtherCAT Direct Mapped
  - 011: HBI Multiplexed 2 Phase 16-bit EtherCAT Direct Mapped
  - 100: SPI EtherCAT Direct Mapped
  - 101: Beckhoff SPI mode
  - 110: N/A (EEPROM is enabled)
  - 111: N/A (EEPROM is enabled)
- Typically, all host interfaces (HBI and SPI) are disabled since much of the device is configured by the EEPROM contents.
- When EEPROM Emulation mode is used, a host interface configuration must be selected in order to allow the host microprocessor to access the EEPROM registers.
- In EEPROM Emulation mode, the software can emulate EEPROM host to access LAN9255 EEPROM registers.

10.0 DIGITAL I/O PINS

- The **SYNC0/SYNC1** pins are the Distributed Clock Sync output signals. They are used to indicate the occurrence of time events. They may be configured to be either push-pull or open-drain/source.
- The **GPI/GPO[15:0]** pins are general purpose inputs/outputs and are directly mapped to the General Purpose Inputs Register and General Purpose Outputs Register. Each pin is individually configurable to be either input or output.

11.0 ETHERNET/ETHERCAT® LED INDICATORS

There are LEDs for Ethernet/EtherCAT Port 0, Port 1, and Port 2.

11.1 Port LED Pins

- All LED output pins are also used for configuration strapping at the rising edge of reset. The strapping level of each LED pin determines whether it is an active-high or active-low output.
- If an LED pin is strapped low, then it becomes an active-high signal. Connect the LED anode to the LED pin, and connect the LED cathode to ground through a resistor.
- If an LED pin is strapped high, then it becomes an active-low signal. Connect the LED anode to 3.3V through a resistor, and connect the LED cathode to the LED pin.
- **LINKACTLED0** (pin 95): This pin is the Link/Activity LED output (off = no link, on = link without activity, blinking = link and activity) for Port 0 (Port A).
- **LINKACTLED1** (pin 90): This pin is the Link/Activity LED output (off = no link, on = link without activity, blinking = link and activity) for Port 1 (Port B).
- **LINKACTLED2** (pin 57): This pin is the Link/Activity LED output (off = no link, on = link without activity, blinking = link and activity) for Port 2 (MII).

11.2 Other LED-Related Pins

- **RUNLED/STATE_RUNLED** (pin 89): This pin can be configured via the AL Status Register to be either Run LED or STATE_RUNLED output. When configured for STATE_RUNLED, it can be used to control the RUN side of a bi-color RUN/ERR LED. Details are in the *LAN9253 Data Sheet*.
- **ERRLED/PME/100FD_B/LEDPOL4** (pin 17) is the configuration strap-in to select the different function. There are four cases as below:
  - **ERRLED** is enabled via the EEPROM contents and should be set to disabled. In the event of an EEPROM loading error, the ERRLED function is forced enabled and false PME events might occur. ERRLED is controlled either by the EtherCAT device or by the local MCU. If ERRLED is needed, the pin should connect to an external LED through a current limit resistor as error LED.
  - If the design has PME wake-up interrupt feature, the pin as **PME** can be connected to one of the MCU GPIO pin. Selecting pin 17 as PME depends on the Power Management Control Register (PMT_CTRL) bits [9:7].
  - **100FD_B**: For 2-Port mode on Port B (as selected by CHIP_MODE1), pin 17 is a strap pin with internal pull-down (PD). Check the strap setting based on below and design.

    0: Auto-negotiation and AMDIX enabled by default

    1: Auto-negotiation and AMDIX disabled (Force 100 Mbps full duplex) by default.
  - **LEDPOL4**: For LED 4 Polarity configuration strap-in pin, check the strap setting based on design and the following:

    0: The LED is set as active-high by default.

    1: The LED is set as active-low by default.

12.0 SAM E53J ETHERNET MAC INTERFACE

The SAM E53J has an Ethernet MAC which may be connected to an external PHY (or switch). The RMII option is described in this section. The SAM E53J can also be configured as MII, but this is less commonly used since MII uses additional signals. For MII signal details, refer to the *SAM D5x/E5x Family Data Sheet*.

12.1 RMII™ Interface

- The SAM E53J RMII signals and their connections to PHY are shown in Table 12-1.
- Series resistors are always recommended on the RMII signals. They should be positioned close to the signal source. The suggested value is from 22Ω to 33Ω.
- There are two possible RMII clocking architectures:
  - PHY sources the 50 MHz REFCK and drives it directly to the SAM E53J.
  - The 50 MHz REFCK is sourced from an oscillator or other external source. REFCK is an input to both the LAN9255 and the PHY. The lengths of the two clock paths should be matched with each other to within 4 inches (10 cm).
- The RMII interface may be used to connect to a switch instead of a PHY. The connections are the same, but users must ensure that input pins of the SAM E53J are connected to the output pins of the switch, and vice versa. RMII pin naming (**RX** and **TX**) on switches is not standardized as it is on PHYs. Do not rely on the switch's pin names to determine the proper connections.

TABLE 12-1: SAM E53J RMII™ SIGNALS TO EXTERNAL PHY

SAM E53J RMII Function	LAN9255 Pin	Connects to RMII™ PHY Device	Location of Series Resistors
RXD1 (input)	**PA12** (pin 61)	RXD1	Near PHY
RXD0 (input)	**PA13** (pin 62)	RXD0	Near PHY
REFCK (input)	**PA14** (pin 63)	REFCK (in or out)	Near source (**Note 1**)
RXER (input)	**PA15** (pin 64)	RXER	Near PHY
CRS_DV (input)	**PA16** (pin 67)	CRS_DV	Near PHY
TXEN (output)	**PA17** (pin 68)	TXEN	Near LAN9255
TXD0 (output)	**PA18** (pin 69)	TXD0	Near LAN9255
TXD1 (output)	**PA19** (pin 73)	TXD1	Near LAN9255
MDC	**PA20** (pin 84) (**Note 2**)	MDC	Near LAN9255
MDIO	**PA21** (pin 87) (**Note 2**)	MDIO	—

Note 1: Depending on the PHY device and chosen RMII clocking architecture, the source of REFCK may be either the PHY or an external oscillator.

2: For compatibility with Microchip software, it is suggested to use pins **PA20** and **PA21** for MDIOC and MDIO. However, the SAM E53J also has the capability to assign these functions to pins **PAB14** and **PB15**, respectively.

13.0 SAM E53J PROGRAMMING AND DEBUG PORTS

13.1 Serial Wire Debug interface

For programming and/or debugging the SAM E53J, the device should be connected using the Serial Wire Debug interface. This interface is currently supported by several Microchip and third-party programmers and debuggers, such as the Atmel-ICE, MPLAB® ICD 4, and MPLAB PICkit™ 4 Embedded Debugger.

- Refer to the Schematic Checklist section of the *SAM D5x/E5X Family Data Sheet* for details on debugging as well as programming connections and options. For connecting to any other programming or debugging tool, refer to the specific programmer or debugger's user guide. Some connector examples are also shown in the Schematic Checklist section of the *SAM D5x/E5x Family Data Sheet*.
- The Serial Wire Debug interface consists of pins **SWCLK/PA30** (pin 120) and **SWDIO/PA31** (pin 121). The **RESETN** (pin 108) pin must also connect to the programmer/debugger connector.
- A 1 kΩ pull-up resistor is required on **SWCLK/PA30** (pin 120) for reliable operation.

14.0 MISCELLANEOUS

14.1 Other Important Pin Settings

- **RBIAS** (pin 111) pin must connect to ground through a 12.1 kΩ resistor with a tolerance of 1.0%. The **RBIAS** pin is used to set up critical bias currents for the embedded 10/100 Ethernet physical devices.
- **RST#** (pin 13) pin is the Active-low Reset input to the LAN9253. During Power-On Reset (POR) and during an EtherCAT system reset command, the LAN9253 drives this pin low as an open-drain output. **RESETN** (pin 108) is the Active-low Reset input to the SAM E53J. It is suggested that these two pins be connected together in combination with a 10 kΩ pull-up resistor. **RESETN** also needs to connect directly to the programming/debugger header. An external Reset source is not required. However, if it is added, it should be open-drain.
- The **REG_EN** (pin 13) pin enables or disables the two +1.2V internal regulators of the LAN9253. Connecting this pin to +3.3V will enable the regulators. Connecting this pin to system ground will disable both regulators. This pin has no internal pull-up or pull-down, so an external pull-up or pull-down resistor is required.
- The LAN9253 has an IEEE 1149.1-compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board-level testing to ensure system functionality and board manufacturability. For details, see the *LAN9253 Data Sheet*. Note that Boundary Scan is not supported in the SAM E53J.
- **TESTMODE** (pin 81): This input pin must be tied to VSS system ground to ensure proper operation.
- To take advantage of the JTAG interface, the **TESTMODE** pin must be driven high. Then, for normal operation, the **TESTMODE** pin must be driven low. This pin has an internal pull-down to ensure normal operation as a No Connect (NC).
- **IRQ** (pin 88) Interrupt request output: The polarity, source, and buffer type of this signal are programmable via the Interrupt Configuration Register (IRQ_CFG). By default, it is open-drain and active-low. For this mode, an external pull-up resistor is required. For more information, refer to the System Interrupts section of the *LAN9253 Data Sheet*.
- Configuration strap values are latched on Power-on Reset and system Reset. Microchip will guarantee that the proper high/low level will be latched in on any device pin with an internal pull-up or pull-down where the device pin is a true No Connect. However, when the configuration strap pin (typically an output pin) is connected to a load, the input leakage current associated with the input load may have an adverse effect on the high/low level ability of the internal pull-up/pull-down. In this case, Microchip recommends to include an external resistor to augment the internal pull-up/pull-down to ensure the proper high/low level for configuration strap values. Lower VDDIO voltages will further exacerbate this condition.
- The recommended pull-up and pull-down resistors values for strap pins are 10 kΩ to 1 kΩ.
- Incorporate an SMD ferrite bead footprint to connect the chassis ground to the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor/ferrite bead far away from LAN9255 device in PCB layout placement for better ESD.

14.2 Placing and Routing in PCB Layout for Other Pins

- Place the **RBIAS** resistor as close to pin 111 of the LAN9255 as possible.
- There are no components placement issues associated with the pull-up/down resistors, HBI, Digital I/O, SPI/SQI, LED, and EEPROM.
- The **RBIAS** resistor (pin 111) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the **RBIAS** resistor.
- There are no critical routing instructions for the pull-up/down resistors, HBI, Digital I/O, SPI/SQI, LED, and EEPROM.
- Microchip recommends utilizing at least a four-layer design for boards for the LAN9255 device. The design engineer should be aware, however, that as tighter EMC standards are applied to the product and as faster signal rates are utilized by the design, the product design may benefit by utilizing up to eight layers for the PCB construction.
- As with any high-speed design, the use of series resistors and AC terminations is very application dependent. Buffer impedances should be anticipated and series resistors must be added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated due to the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.
- Bulk capacitors for each power plane should be routed immediately into power planes with traces as short and wide as possible.

- Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.
- Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, and so on). The electrical engineer must work with the PCB designer to determine all these variables.

NOTES:

15.0 HARDWARE CHECKLIST SUMMARY

TABLE 15-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"			
	Section 2.2, "Pin Check"	The pins match the data sheet and Table 2-1.		
Section 3.0, "Power"	Section 3.1, "+3.3V Power Supply Connections"	The voltage required for **VDD33**, **VDD33TRXRX1**, **VDD33TXRX2**, and **VDD33BIAS** is 3.3V. Ferrite beads are recommended on all except **VDD33**. Bulk decoupling must be positioned on both sides of each ferrite bead and a 0.1 µF cap must be placed near each pin. Check connections in Figure 3-1.		
	Section 3.2, "+1.8V to +3.3V Variable I/O Power Supply Connections"	**VDDIOB**, **VDDIO_J**, **VDDIO_S**, and **VDDANA** may be 1.8V to 3.3V and must all be in the same voltage. Ensure that a 0.1 µF cap is placed near each pin.		
	Section 3.3, "VDDCORE and VSW"	Do not supply external power to **VDDCORE**. Make sure to decouple it with 4.7 µF and 100 nF. If the SAM E53J regulator is operated in Switching mode, connect 10 µF between **VSW** and **VDDCORE**. If operated in Linear mode, leave **VSW** open. See Figure 3-3 and Figure 3-4.		
	Section 3.4, "VDDCR"	If **REG_EN** is pulled high, do not supply external power to **VDDCR**. Make sure to decouple these pins with 0.1 µF cap at pins 52 and 76, and 470 pF plus ≥ 1 µF at pin 12. **OSCVDD12** is unconnected. See Figure 3-1. If **REG_EN** is pulled low, supply external 1.2V to **OSCVDD12** and **VDDCR**. See Figure 3-2. In either case, **VDD12TX1** and **VDD12TX2** must be tied together and derive power from **VDDCR** or the external 1.2V source.		
	Section 3.5, "Ground and Power Connections"	Do not split the ground plane. Make sure to connect **GNDANA**, **OSCVSS**, and the exposed die paddle **VSS** to one ground plane. Check all power connections against Figure 3-1 or Figure 3-2 and either Figure 3-3 or Figure 3-4 as determined by the regulator modes.		
	Section 3.6, "Placing Power Pins in PCB Layout"	If going into PCB layout stage, check the components placement based on this section requirement for power.		
	Section 3.7, "Routing Power Pins in PCB Layout"	If going into PCB layout stage, check the traces routing based on this section requirement for power.		
Section 4.0, "Ethernet/ EtherCAT® Signals"	Section 4.1, "Copper Port Differential Pair PHY Interface"	Check if the differential pair connections are correct, with a 49.9Ω termination resistor from each **TX** and **RX** line connected to **VDD33TXF1/2**. On each port, connect the **RX** and **TX** transformer center taps to **VDD33TXF1/2** and decouple to **GND** w/ 22 nF cap. See Figure 4-1.		
	Section 4.2, "Copper Port Magnetics to RJ45 Connections"	Check if the magnetics-to-RJ45 connections are correct, with 75Ω resistor from the cable-facing center taps connected to a 1000 pF, 2 kV capacitor. Terminate the unused RJ45 pin pairs 4/5 and 7/8 based on Figure 4-2.		
	Section 4.3, "Using RJ45 with Integrated LED"	Use RJ45 with integrated LED if the product working environment is not very noisy. Otherwise, use an independent LED solution.		
	Section 4.4, "Placing Copper Ports in PCB Layout"	If going into PCB layout stage, make sure to check the components placement based on Figure 4-2 and this section's requirements for the copper ports.		
	Section 4.5, "Routing Copper Ports in PCB Layout"	If going into PCB layout stage, check the traces routing based on this section's requirements for the copper ports.		

TABLE 15-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 5.0, "Clock Circuit"	Section 5.1, "LAN9253 Crystal or Oscillator Clock Connections"	Remember that a 25 MHz crystal or clock is needed on **OSCI/OSCO**. The crystal minimum drive level is 300 µw. If using an oscillator, the recommended voltage is 3.3V. Frequency tolerance must be ±50 ppm. Calculate the crystal load capacitors based on the crystal C_L specifications. Refer to Figure 5-1.		
	Section 5.2, "SAM E53J Crystal or Oscillator Clock Connections"	Connect the **CLK_25** output to the **PA14** or **PB22** clock input of the SAM E53. Alternatively, provide a separate 8 MHz to 40 MHz clock, or a crystal to either **PA14** and **PA15** or **PB22** and **PB23**. Additionally, a 32.768 kHz crystal is optional for the SAM E53. Connect to **PA00** and **PA01**.		
	Section 5.3, "Other Clock Pins"	Verify whether the strapping of the **CLK_25** pin is appropriate based on the input reference clock or crystal and the presence or absence of **CLK_25**. Note that there is a VDD/2 strapping option in addition to either high or low.		
	Section 5.4, "Placing and Routing Crystal in PCB Layout"	If going into PCB layout stage, check the components' placement and traces routing based on this section's requirement for crystal/oscillator circuit.		
Section 6.0, "Configuration for System Applications"	Section 6.1, "Microcontroller Mode with SPI/SQI Interface"	The main connection between the LAN9253 and SAM E53 should be the SQI/QSPI bus. Do not use the Host Bus Interface (HBI) or Digital I/O mode. See Figure 6-1.		
	Section 6.4, "System Block Diagram"	Verify if the selection is either 2-Port mode, 3-Port Downstream mode, or 3-Port Upstream mode, and make sure that correct strapping is used for the system configuration.		
Section 7.0, "Microcontroller Mode Via SPI/SQI Interface"	Section 7.1, "QSPI/SQI Host-to-Client Connection"	Verify the connection of the SQI/QSPI interfaces between the LAN9253 and SAM E53 as shown in Figure 7-1.		
Section 8.0, "Expansion Mode with MII Interface for Extra Port"	Section 8.1, "MII Signals and Connections"	If the design uses Expansion mode with MII interface, check the MII connections with external PHY based on Figure 8-1.		
	Section 8.2, "MII Interface for EtherCAT® Device"	For EtherCAT MII, PHY output pins **TX_CLK**, **COL**, and **CRS** should not connect to anything. PHY pin **TXER** should be grounded.		
	Section 8.3, "MII Interface Series Terminations"	Series termination resistors are suggested for all MII signals. Locate them near the source. See Figure 8-1 for the locations.		
	Section 8.4, "Other Pins Related to MII Interface"	Check the MII-related strap pins setting based on Figure 8-1 and this section's requirements.		
	Section 8.5, "MII Back-to-Back Connections"	If two LAN9255 devices are connected to MII back-to-back, check if is correct based on Figure 8-2.		
	Section 8.6, "Placing and Routing in PCB Layout for MII Interface"	If going into PCB layout stage, check the components' placement and traces routing based on this section's requirements for MII interface.		
Section 9.0, "EEPROM Interface"	Section 9.1, "EEPROM Pins"	If the design uses EEPROM, check EEPROM connection based on Figure 9-1.		
	Section 9.2, "EEPROM Related Strapping Pin"	Check EEPROM related strap pin settings for the correct EEPROM size used based on Figure 9-2.		
	Section 9.3, "EEPROM Emulation Mode"	If the design uses EEPROM Emulation mode, check the EEPROM strap pins to enable EEPROM Emulation mode and have the correct settings.		
Section 10.0, "Digital I/O Pins"		Make sure that the **SYNC0/SYNC1** pins and **GPI/GPO[15:0]** pins are configured properly.		

TABLE 15-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 11.0, "Ethernet/ EtherCAT® LED Indicators"	Section 11.1, "Port LED Pins"	Check if LED use is correct for each copper port. The polarity of each LED is determined by whether the pin is strapped high or low.		
	Section 11.2, "Other LED-Related Pins"	Check other LED related strap pins to see if they were set correctly.		
Section 12.0, "SAM E53J Ethernet MAC Interface"	Section 12.1, "RMII™ Interface"	If the design uses the RMII interface of the SAM E53, check the RMII connections with the external PHY as shown in Table 12-1. The SAM E53 does not source the RMII clock, so there must be another source. Series resistors are recommended on all **RMII** pins.		
Section 13.0, "SAM E53J Programming and Debug Ports"	Section 13.1, "Serial Wire Debug interface"	For programming and debugging the SAME53, a connector should be provided. Review the pinout for the chosen device for correctness. Ensure that there is a pull-up resistor on **SWCLK/PA30**.		
Section 14.0, "Miscellaneous"	Section 14.1, "Other Important Pin Settings"	Check other important pin settings carefully. For example, **RBIAS** resistor must be used with 12.1 kΩ resistor, **RST#** pin, **REG_EN** pin and so on based on the details in this section.		
	Section 14.2, "Placing and Routing in PCB Layout for Other Pins"	If going into PCB layout stage, check the components' placement and trace routing based on this section's requirements for other pins.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003834A (03-09-21)	Initial release	

NOTES:

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