

Capacitor-Coupled Switched Shunt (CCSS) Regulator

Features

- Efficiencies up to 75% at 20 mA
- Less than 20 mW Standby Power
- Optional 6V, 12V, or 24V Fixed Output Voltage, or adjustable from 6V to 28V
- Output Current Scalable up to 50 mA
- 120 VAC to 240 VAC Input
- No Magnetics
- Inherent Short-circuit Protection

Applications

- Household Appliances
- White Goods
- Lighting Controls
- Utility Meters

General Description

The SR10 is a non-isolated, capacitor-coupled switched shunt regulator designed to operate directly from the AC line. Output voltage can be either fixed at 6V, 12V, or 24V using an internal feedback divider or be adjusted over a 6V to 28V range using an external feedback divider. Output current capability is scalable to 50 mA by selection of the series coupling capacitor C_S on the AC line. Standby power can be under 20 mW, and efficiencies of 75% are possible depending upon configuration and degree of transient protection.

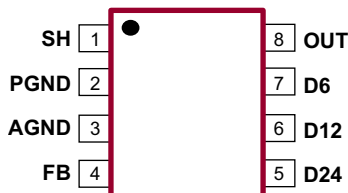
All components except for C_S are low voltage, easing PCB layout and alleviating high-voltage creepage concerns.

Inherent short circuit protection is provided by the reactance of the C_S series capacitor, which limits current even with a dead short on the output. Overcurrent protection (OCP) shuts off the shunt during a line transient.

Refer to “AN-H65 CSS Application Note” for further information.

Package Type

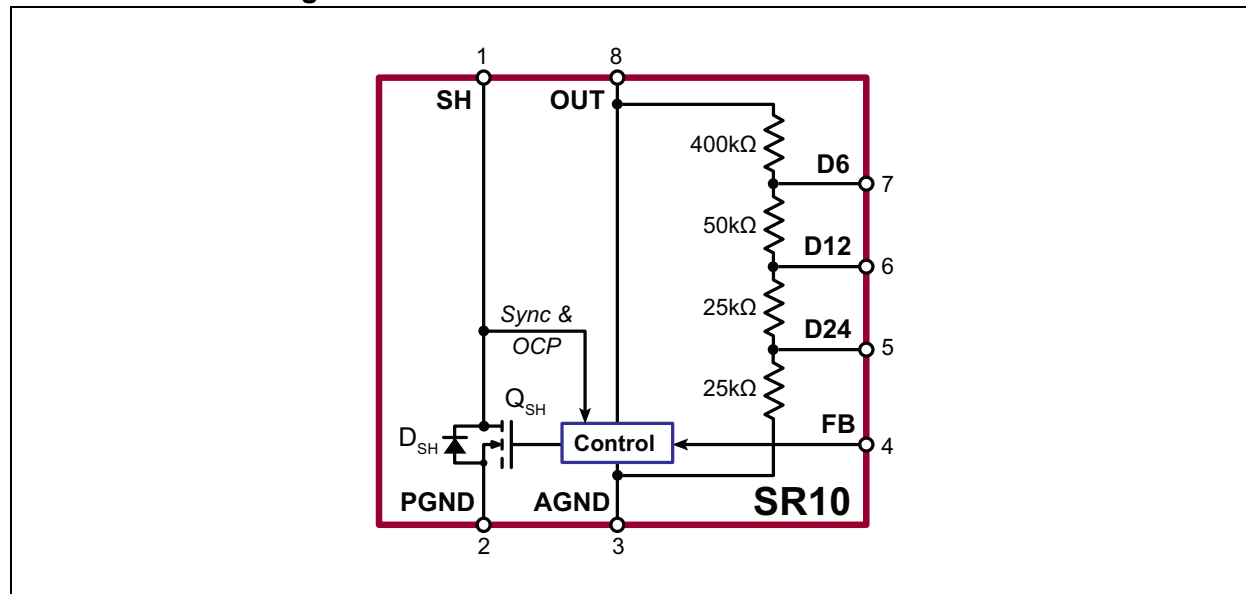
8-lead SOIC
(Top view)



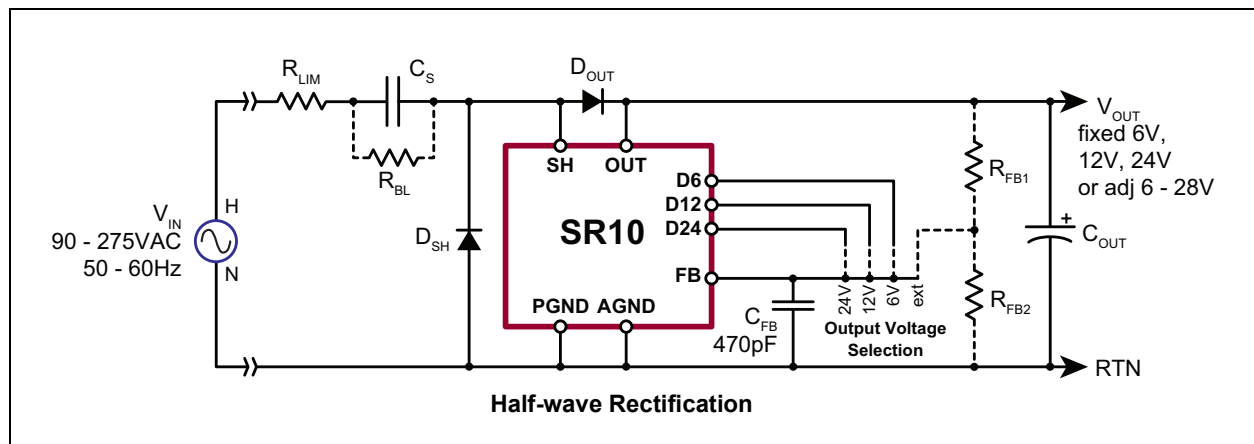
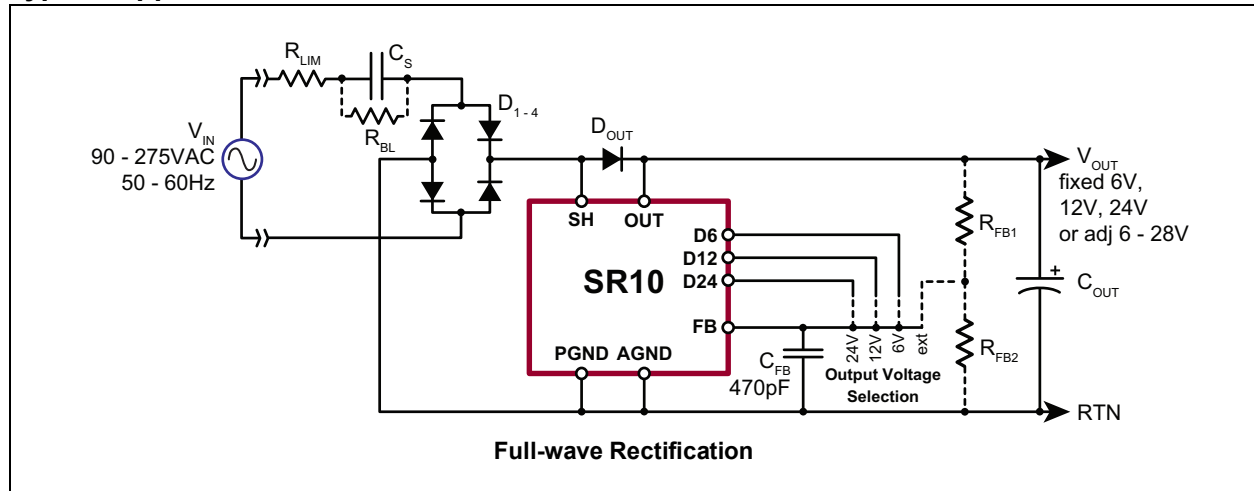
See [Table 2-1](#) for pin information.

SR10

Functional Block Diagram



Typical Application Circuits



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{OUT}, V_{SH}	40V
V_{FB}	5V
$P_{GND-AGND}$	±300 mV
$I_{IN(RMS)}$ (SH to PGND)	300 mARMS
I_{DSH} (PGND to SH)	300 mA
Operating Junction Temperature, T_J	–40°C to +125°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Peak Shunt Current	V_{FB}	—	—	—	—	See Figure 3-2 .
Output voltage	V_{OUT}	6	—	28	V	

ELECTRICAL CHARACTERISTICS

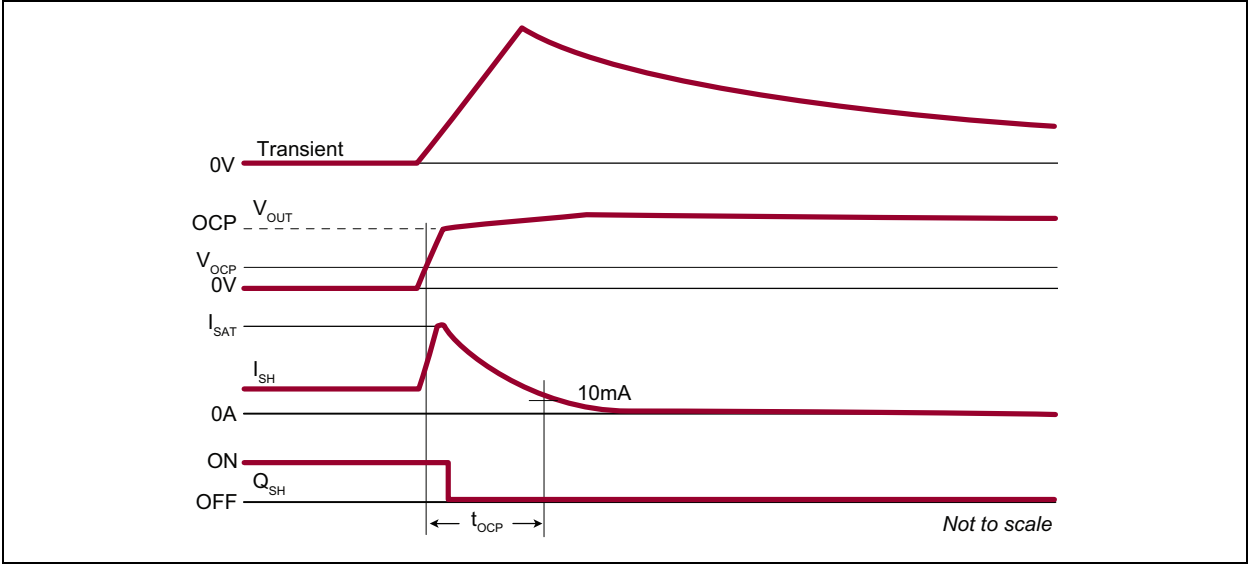
Electrical Specifications: $T_A = 25^\circ\text{C}$ unless otherwise noted. Voltages are referenced to PGND/AGND pin.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Feedback Threshold (Shunt Turn-off)	V_{FB}	1.02	1.2	1.38	V	$T_A = 25^\circ\text{C}$,
		1.02	1.2	1.38		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (Note 1)
FB Input Bias Current	I_{FB}	—	—	±1	µA	
Internal Feedback Divider Ratio	D6	4.85	5	5.15	V/V	$V_{OUT} = 6\text{V}$
	D12	9.7	10	10.3		$V_{OUT} = 12\text{V}$
	D24	19.4	20	20.6		$V_{OUT} = 24\text{V}$
Internal Divider Resistance	R_{DIV}	—	500	—	kΩ	OUT to AGND (Note 1)
Shunt on Resistance	R_{SH}	—	3	7	Ω	100 mA SH to PGND 100 mA PGND to SH
Maximum Shunt Current	I_{SH}	220	—	—	mA	$V_{SH} < 1.2\text{V}$, 25°C
		180	—	—		85°C (Note 1)
Shunt Diode Voltage Drop	V_D	—	880	—	mV	$I_D = 220\text{ mA}$
Bias Current into OUT Pin	I_{BIAS}	—	220	400	µA	28V applied to the OUT pin
Pull-down Resistance on SH	R_{PD}	40	50	60	kΩ	$V_{SH} = 1.5\text{V}$
Voltage at SH to Turn the Shunt on SYNC	V_{SYNC}	2	2.3	2.5	V	
Voltage at SH to Turn the Shunt off when on OCP	V_{OCP}	2	2.3	2.5	V	Shunt on
Shunt Current Fall Time	t_{FALL}	—	15	—	µs	90%–10%, $I_{SH} = 100\text{ mA}$
OCP Response Time	t_{OCP}	—	15	—	µs	Shunt on, $I_{SHUNT} < 10\text{ mA}$ (See Figure 3-4 .)

Note 1: Guaranteed by design

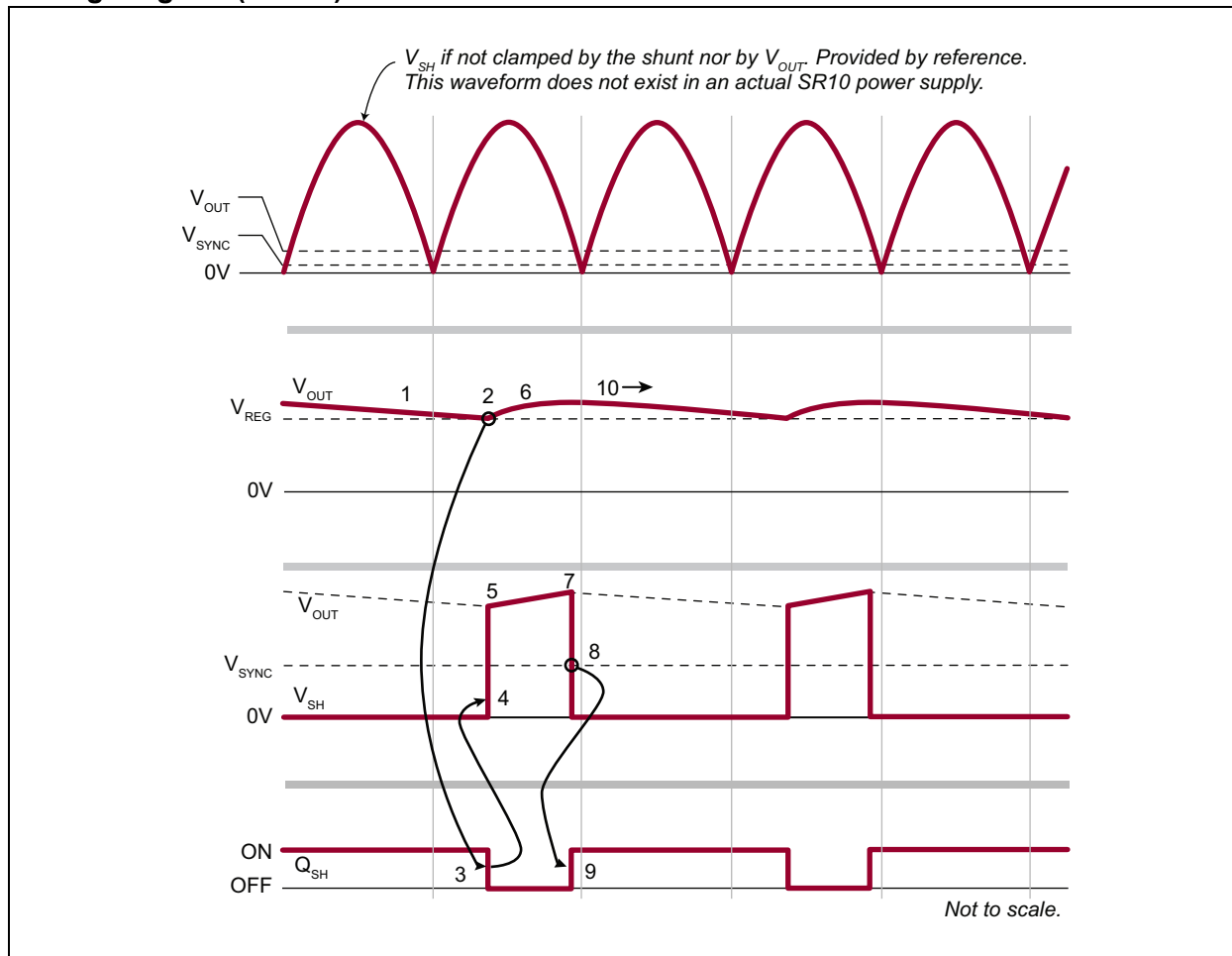
TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Maximum Junction Temperature	T_J	-40	—	+125	°C	
PACKAGE THERMAL RESISTANCE						
8-lead SOIC	θ_{JA}	—	101	—	°C/W	

OCP Timing Diagram



Timing Diagram (Note 1)



Note 1: (1) Output voltage decays under load until (2) it hits the regulation point which (3) turns off the shunt, (4) freeing V_{SH} to rise (5) until it is clamped by V_{OUT} where (6) input current flows to the output, causing V_{OUT} to rise (7) until V_{SH} falls below V_{OUT} . (8) When it reaches V_{SYNC} (9) the shunt is turned on and current no longer flows to the output. (10) The cycle repeats.

2.0 PIN DESCRIPTION

All pins of SR10 are low voltage. Other details on the pins are listed in [Table 2-1](#). See [Package Type](#) for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SH	Shunt
2	PGND	Power ground for the shunt
3	AGND	Analog ground for the controller
4	FB	Feedback input
5	D24	Internal feedback divider 24V tap
6	D12	Internal feedback divider 12V tap
7	D6	Internal feedback divider 6V tap
8	OUT	Connect to regulator output

3.0 APPLICATION INFORMATION

The SR10 is a capacitor-coupled, switched shunt regulator. Capacitor-coupling to the AC line limits input current due to the finite charge per cycle that can be transferred. Contrasting with a traditional Zener shunt, the switched shunt operates either fully on or fully off, resulting in low standby power consumption.

3.1 Output Current Capability

Output current capability is largely a function of the C_S capacitor and the input voltage. Table 3-1 provides approximate current capability for various C_S values and line voltages. Actual current will be less due to losses. Higher output voltages slightly reduce output current capability.

3.1.1 C_S TABLE

Table 3-1 is based on the previously provided equations for C_S . Actual output current may be less due to losses (~5% less). AC line voltage is assumed to be 90 VRMS–135 VRMS at 60 Hz or 190 VRMS–275 VRMS at 50 Hz. Slashed cells exceed recommended operating conditions for peak shunt current at 85°C.

For universal 120V and 240V operation, choose C_S based on 120 VAC and make sure that operation at 240 VAC does not fall in a slashed cell. The relevant cells are adjacent to each other. For example, if 50 mA at 12V is needed and a full rectification is used, a C_S capacitor of $2.2 \mu\text{F} \pm 10\%$ provides 53.8 mA at 120 VAC (90 VAC low line). But at 240 VAC, the cell to the right (240 VAC column) is slashed, and universal operation is not possible. This assumes 120 VAC low line is 90 VAC and 240 VAC high line is 275 VAC. For other high/low voltages, use the equation.

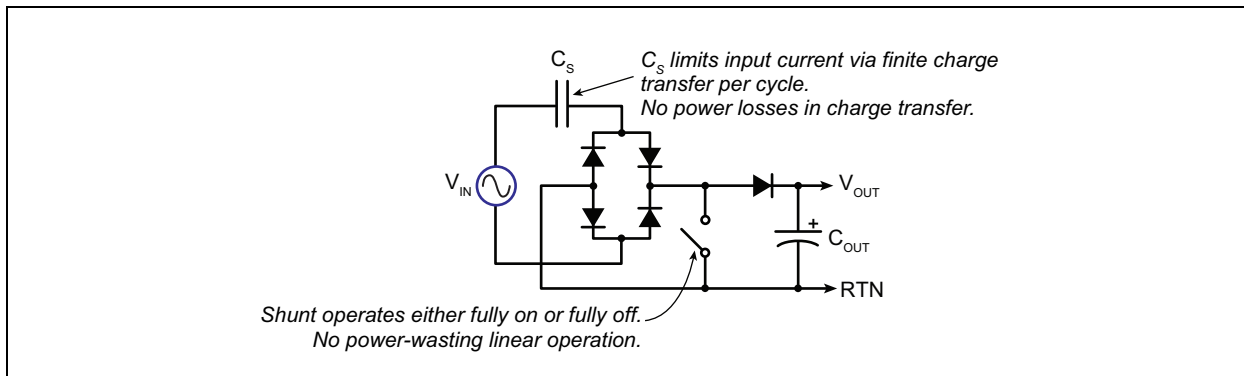


FIGURE 3-1: Simplified Schematics.

TABLE 3-1: OUTPUT CURRENT CAPABILITY (mA)

CS	CS	6V Output				12V Output				24V Output			
		Half		Full		Half		Full		Half		Full	
		120V	240V	120V	240V	120V	240V	120V	240V	120V	240V	120V	240V
		60 Hz	50 Hz	60 Hz	50 Hz	60 Hz	50 Hz	60 Hz	50 Hz	60 Hz	50 Hz	60 Hz	50 Hz
220 nF	10%	2.9	5.2	5.7	10.3	2.9	5.2	5.4	10.1	2.7	5.1	4.8	9.6
	20%	2.6	4.7	5	9.2	2.5	4.6	4.8	9	2.4	4.5	4.3	8.5
330 nF	10%	4.4	7.9	8.5	15.5	4.3	7.8	8.1	15.1	4.1	7.6	7.2	14.4
	20%	3.9	7	7.6	13.8	3.8	6.9	7.2	13.4	3.6	6.8	6.4	12.8
470 nF	10%	6.3	11.2	12.1	22	6.1	11.1	11.5	21.5	5.8	10.8	10.3	20.5
	20%	5.6	10	10.8	19.6	5.4	9.9	10.2	19.1	5.2	9.6	9.1	18.2
680 nF	10%	9.1	16.2	17.5	31.9	8.9	16	16.6	31.2	8.4	15.7	14.9	29.7
	20%	8.1	14.4	15.6	28.4	7.9	14.3	14.8	27.7	7.5	13.9	13.2	26.4
1.0 μF	10%	13.3	23.9	25.7	46.9	13	23.6	24.4	45.8	12.4	23	21.9	43.7
	20%	11.9	21.2	22.9	41.7	11.6	21	21.7	40.7	11	20.5	19.4	38.8
1.5 μF	10%	20	35.8 1	38.6	70.4 1	19.5	35.4 1	36.7	68.7 1	18.6	34.6 1	32.8	65.5 1
	20%	17.8	31.8 1	34.3	62.5 1	17.4	31.4 1	32.6	61.1 1	16.5	30.7 1	29.1	58.2 1
2.2 μF	10%	29.4	52.5 1	56.6	103.2 1	28.6	51.9 1	53.8	100.8 1	27.2	50.7 1	48.1	96.1 1
	20%	26.1 1	46.6 1	50.3 1	91.7 1	25.5 1	46.1 1	47.8 1	89.6 1	24.2 1	45.1 1	42.7 1	85.4 1

Note 1: Exceeds recommended operating limits

3.2 Output Voltage

The output voltage may be adjusted over the range of 6V to 28V using either the SR10's internal feedback divider or by using an external divider. The internal divider has taps for 6V, 12V, and 24V which are brought out to pins D6, D12, and D24, respectively. Connecting the appropriate tap to the feedback pin FB provides the chosen output voltage.

If an output voltage other than that provided by the internal divider is required, an external feedback divider from V_{OUT} to the FB pin may be used. The range is from 6V to 28V.

3.3 Additional Information

For a more detailed description or for sample circuits, an application note and a demo board are available. The "AH-H65 CCSS Application Note" explains the operating principle of the capacitor-coupled switched shunt regulator. It also provides design equations and guidelines as well as specifies special testing considerations.

The "SR10DB1SR10 Demo Board" details jumper-selectable half-wave or full-wave rectification, jumper-selectable output voltage, and socketed components that allow easy optimization.

TABLE 3-2: OUTPUT VOLTAGE CONNECTIONS

Connection	Output Voltage
FB Connected to D6	6V
FB Connected to D12	12V
FB Connected to D24	24V
FB Connected to External Divider	$V_{OUT} = 1.2V \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$

Note 1: A 470 pF capacitor from FB pin to AGND pin minimizes the effects of a noisy AC line.

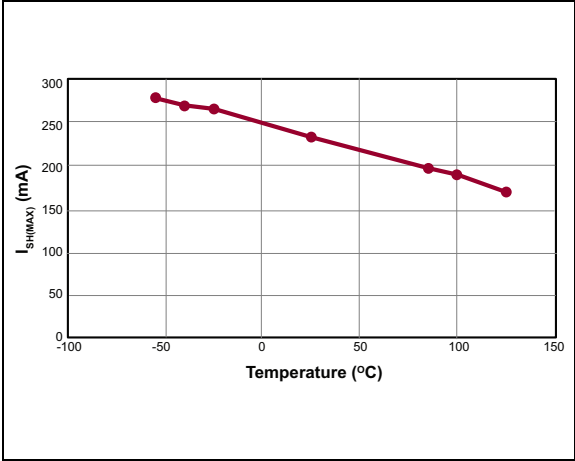


FIGURE 3-2: Maximum Shunt Current.

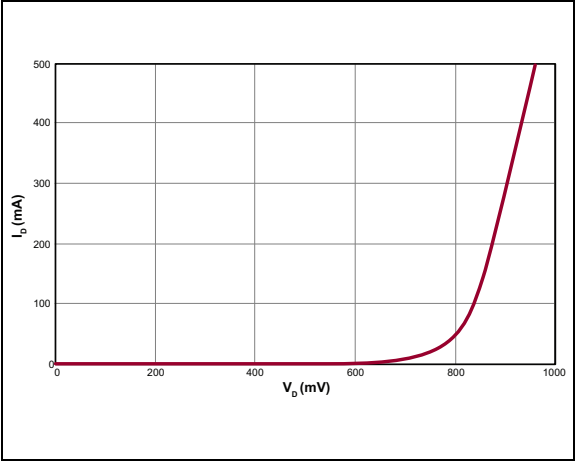


FIGURE 3-3: Shunt Diode Characteristics.

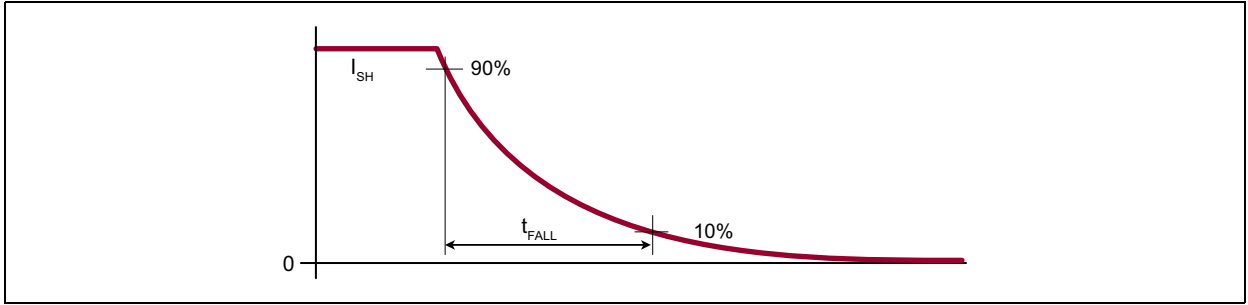
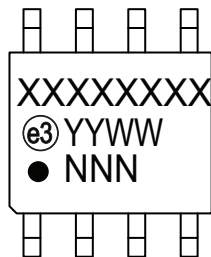


FIGURE 3-4: Shunt Turn-off Fall Time.

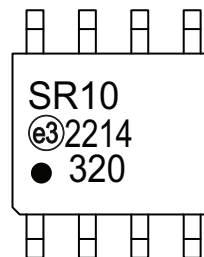
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-lead SOIC



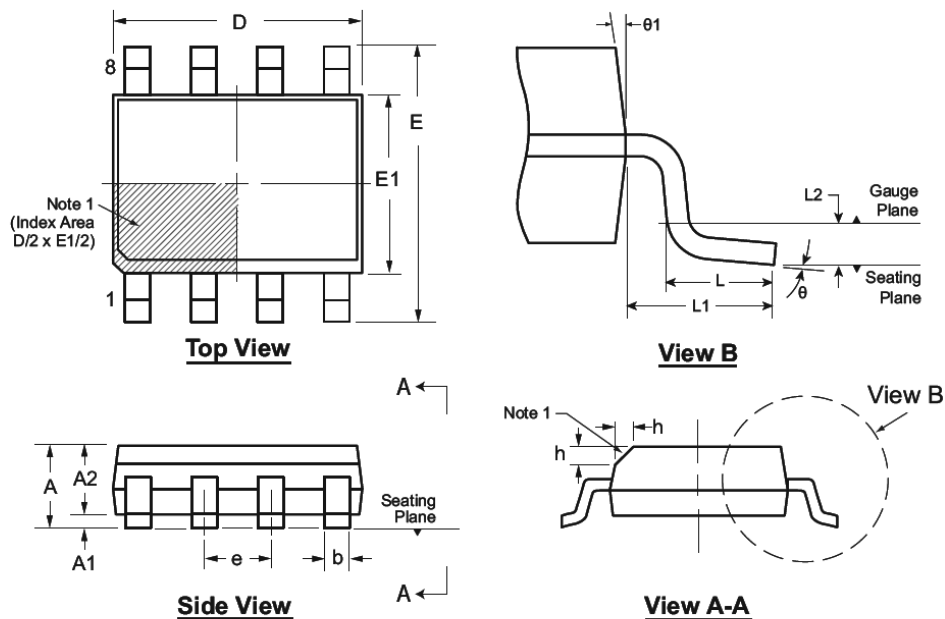
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

8-Lead SOIC (Narrow Body) Package Outline (LG/TG) 4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier, an embedded metal marker, or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (September 2022)

- Converted Supertex Doc# DSFP-SR10 to Microchip DS20005770A
- Changed the package marking format
- Changed the quantity of the LG package from 2500/Reel to 3300/Reel to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>					
Device	Package Options		Environmental		Media Type
Device:	SR10	=	Capacitor-Coupled Switched Shunt (CCSS) Regulator		
Package:	LG	=	8-lead SOIC		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	3300/Reel for an LG Package		

Example:

a) SR10LG-G: Capacitor-Coupled Switched Shunt (CCSS) Regulator, 8-lead SOIC, 3300/Reel for an LG Package.

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ISBN: 978-1-6683-1263-6

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