AN1907

Microchip LAN9252 Migration from Beckhoff ET1100

Author: *Kansal Mariam Banu Shaick Ibrahim*
Microchip Technology Inc.

INTRODUCTION

The LAN9252 is a 2/3-port EtherCAT® slave controller with dual integrated Ethernet PHYs which each contain a full-duplex TX transceiver and support 100 Mbps (100BASE-TX) operation. The LAN9252 supports HP Auto-MDIX, allowing the use of direct connect or cross-over LAN cables. 100BASE-FX is supported via an external fiber transceiver. The device can be configured as a 3-port slave, providing an additional MII port. This port can be connected to an external PHY, forming a tap along the current daisy chain, or to another LAN9252 creating a 4-port solution.

The purpose of this document is to provide transition details for migrating a design from Beckhoff ET1100 to Microchip's LAN9252.

FUNCTIONAL OVERVIEW

The LAN9252 EtherCAT device implements a 3-port EtherCAT slave controller with 4K bytes of Dual Port memory (DPRAM), 4 SyncManagers, 3 Fieldbus Memory Management Units (FMMUs) and a 64-bit Distributed Clock.

Each port receives an Ethernet frame, performs frame checking and forwards it to the next port. Time stamps of received frames are generated when they are received. The Loop-back function of each port forwards Ethernet frames to the next logical port if there is either no link at a port, or if the port is not available, or if the loop is closed for that port. The Loop-back function of port 0 forwards the frames to the EtherCAT Processing Unit. The loop settings can be controlled by the EtherCAT master.

Packets are forwarded in the following order: Port 0->EtherCAT Processing Unit->Port 1->Port 2.

The EtherCAT Processing Unit (EPU) receives, analyzes and processes the EtherCAT data stream. The main purpose of the EtherCAT Processing unit is to enable and coordinate access to the internal registers and the memory space of the EtherCAT Slave Controller (ESC), which can be addressed both from the EtherCAT master and from the local application. Data exchange between the master and slave application is comparable to a dual-ported memory (process memory), enhanced by special functions such as consistency checking (SyncManager) and data mapping (FMMU).

* EtherCAT® is registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

1.0 HARDWARE TRANSITION

Figure 1 depicts the hardware transition from the ET1100 to the LAN9252 at an application level. A summary of the differences in ESC features is provided in Table 1. Functional level block diagrams of the ET1100 and LAN9252 are shown for comparison in Figure 2 and Figure 3, respectively.

FIGURE 1: ET1100 TO LAN9252 APPLICATION TRANSITION

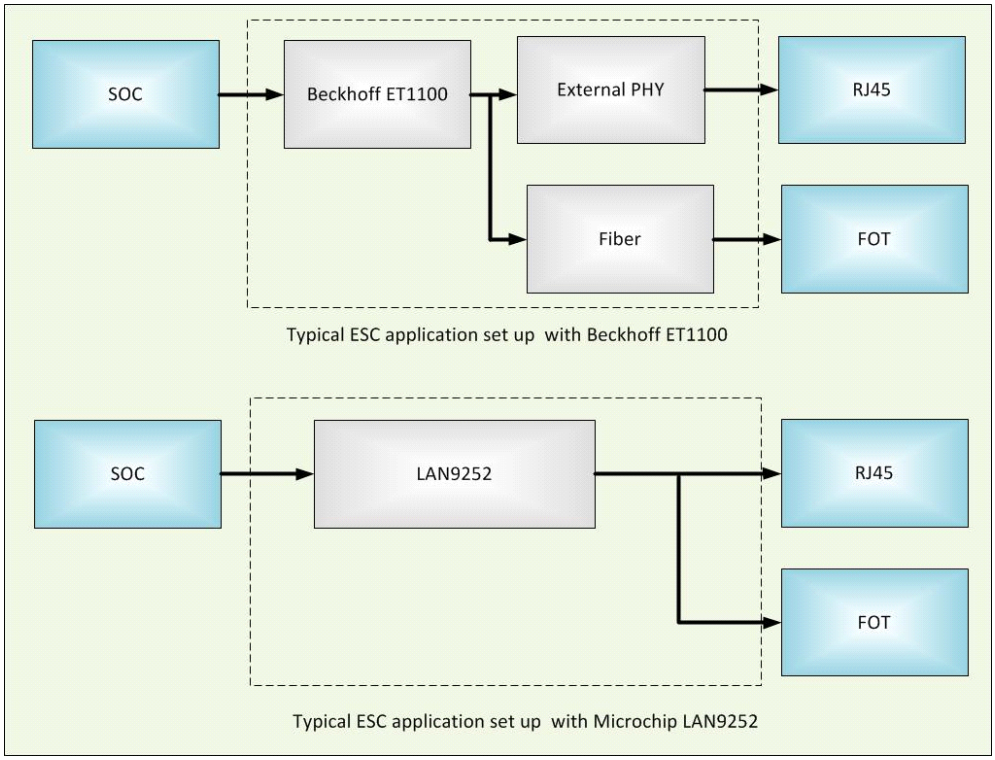


TABLE 1: ESC MAIN FEATURE COMPARISON

Feature	ET1100	LAN9252
Ports	2-4 (Each EBUS/ MII)	2 x Internal PHY 1 x MII
FMMU	8	3
Sync Managers	8	4
RAM (Kbyte)	8	4
Distributed Clock	64bit	64bit
Process Data Interfaces		
Digital I/O	32 bit	16 bit
Normal SPI Slave (SPICLK <= 30MHz)	YES (SPICLK <= 20MHz)	YES (SPICLK <= 30MHz)
Fast SPI Slave (SPICLK <= 80MHz)	-	YES
DUAL/QUAD SPI Slave (SPICLK <= 80MHz)	-	YES
SQI SPI Slave (SPICLK <= 80MHz)	-	YES
8/16 bit De-multiplexed bus interface	Async/Sync	Async
8/16 bit multiplexed bus interface	-	Async

FIGURE 2: ET1100 ESC BLOCK DIAGRAM

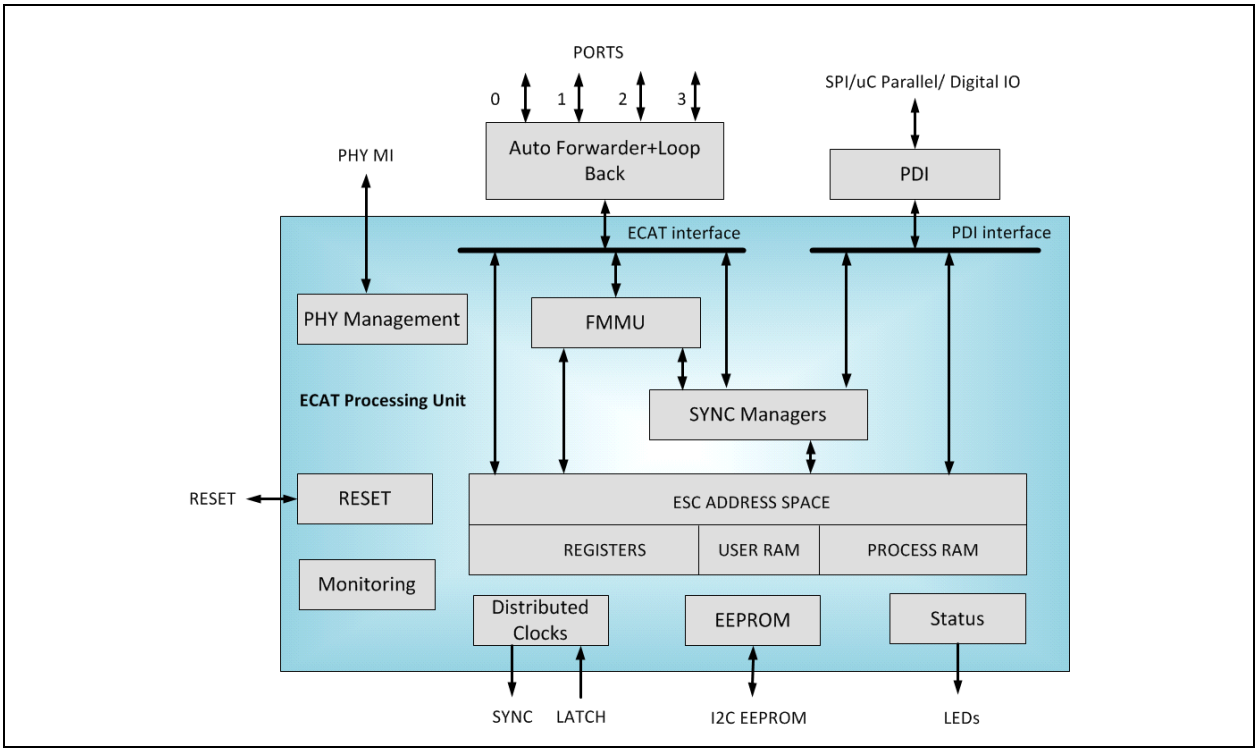
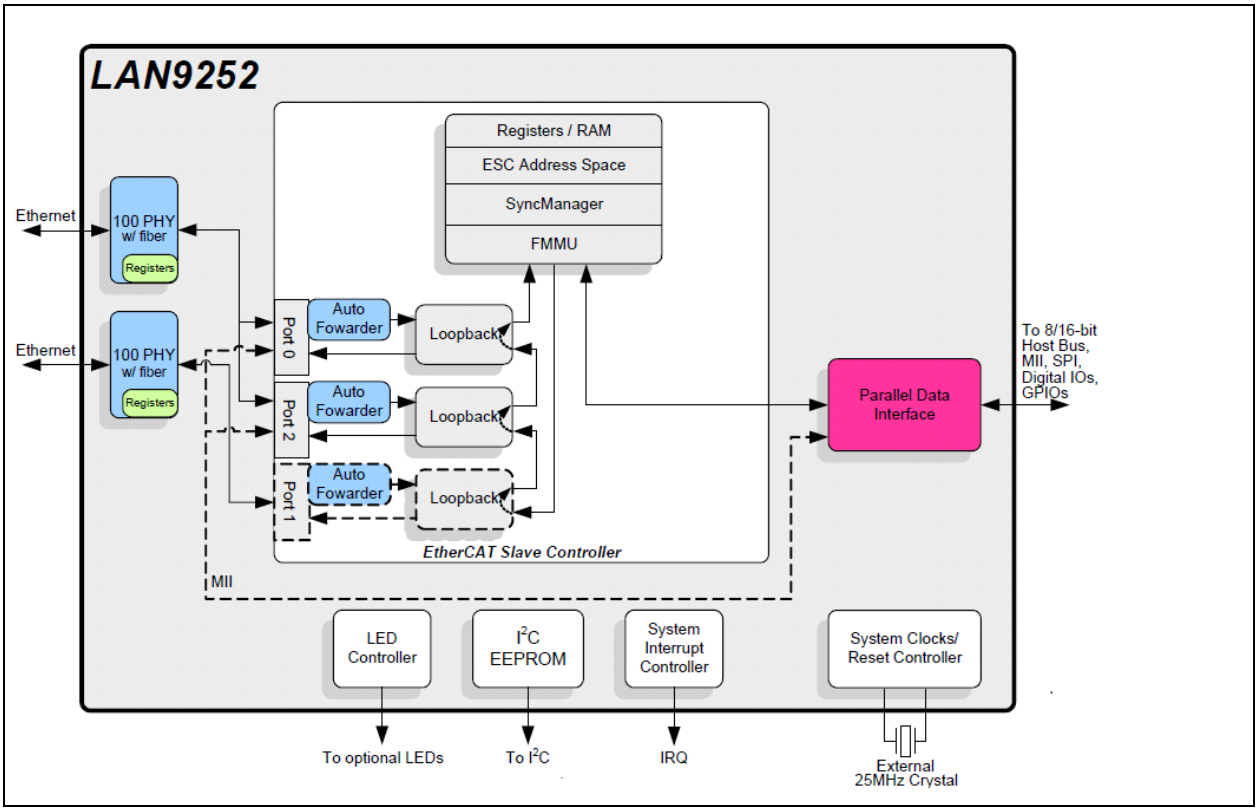


FIGURE 3: LAN9252 ESC BLOCK DIAGRAM



The following subsections detail the main distinctive features of the LAN9252.

1.1 EtherCAT CSR and Process Data RAM Access

The EtherCAT CSRs provide register-level access to the various parameters of the EtherCAT Core. EtherCAT related registers can be classified into two main categories based upon their method of access: direct and indirect.

The directly accessible EtherCAT registers are part of the main system CSRs. These registers provide data/command registers (for access to the indirect EtherCAT Core registers).

The indirectly accessible EtherCAT Core registers reside within the EtherCAT Core and must be accessed indirectly via the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA) and EtherCAT CSR Interface Command Register (ECAT_CSR_CMD). The indirectly accessible EtherCAT Core CSRs provide full access to the many configurable parameters of the EtherCAT Core.

The EtherCAT Core Process Data RAM can be accessed indirectly via the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA) and EtherCAT CSR Interface Command Register (ECAT_CSR_CMD), starting at 1000h. The EtherCAT Core Process Data RAM can also be accessed more efficiently using the EtherCAT Process RAM Read Data FIFO (ECAT_PRAM_RD_DATA) and EtherCAT Process RAM Read Command Register (ECAT_PRAM_RD_CMD).

1.2 Internal PHYs

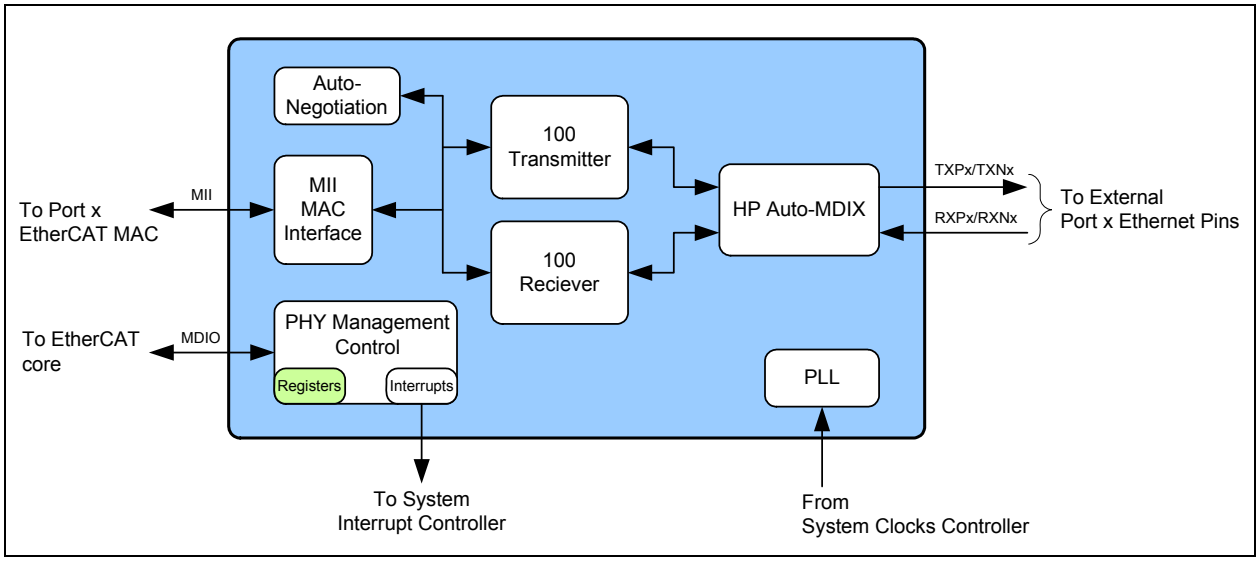
The device integrates two IEEE 802.3 PHYs which include Auto-Negotiation, HP Auto-MDIX, and can be configured for either 100 Mbps copper (100BASE-TX) or 100 Mbps fiber (100BASE-FX) operation.

Functionally, each PHY can be divided into the following sections:

- 100BASE-TX Transmit and 100BASE-TX Receive
- Auto-Negotiation
- HP Auto-MDIX
- PHY Management Control and PHY Interrupts
- PHY Power-Down Modes
- Resets
- Link Integrity Test
- Cable Diagnostics
- Loopback Operation
- 100BASE-FX Far End Fault Indication

The major blocks of the physical PHY are detailed in Figure 4.

FIGURE 4: LAN9252 PHY BLOCK DIAGRAM



To enable star or tree network topologies, the device can be configured as a 3-port slave, providing an additional MII port. This port can be connected to an external PHY.

By default, the internal PHYs are configured for 100Mbps, full-duplex operation. Auto-Negotiation is enable for 100BASE-TX mode and disable for 100BASE-FX mode. The EtherCAT Core will also check and update the configuration if necessary.

By default, the external PHY should be configured for 100Mbps, full-duplex operation with Auto-Negotiation enabled. The EtherCAT Core will check and update the configuration if necessary.

1.3 Chip Modes

The LAN9252 supports the following chip modes:

- **2-Port Mode**: Ports 0 and 1 are connected to internal PHYs A and B.
- **3-Port Downstream Mode**: Ports 0 and 1 are connected to internal PHYs A and B. Port 2 is connected to the external MII pins.
- **3-Port Upstream Mode**: Ports 2 and 1 are connected to internal PHYs A and B. Port 0 is connected to the external MII pins.

These modes are selected via the CHIP_MODE1 and CHIP_MODE0 EtherCAT chip mode straps, as shown in Table 2.

TABLE 2: CHIP_MODE[1:0] CONFIGURATION

CHIP_MODE1	CHIP_MODE0	Mode
0	0	2-Port Mode
0	1	RESERVED
1	0	3-Port Downstream Mode
1	1	3-Port Upstream Mode

1.4 Process Data Interface (PDI)

The following subsections detail the Hardware and Software transition from ET1100 to LAN9252.

The PDI comparison between ET1100 and LAN9252 are listed below in Table 3.

TABLE 3: PDI COMPARISON

PDI Types	ET1100	LAN9252
Digital I/O Interface	Support **32** configurable digital I/Os	Support **16** configurable digital I/Os
SPI- Normal R/W	Support 4-wire, SPI CLOCK up to 20MHz	Support 4-wire, SPI CLOCK up to 30MHz
SPI- FAST R/W	Not Supported	Support 4-wire, SPI CLOCK up to 80MHz
SPI- DUAL/QUAD DATA R/W	Not Supported	Support 4 or 6-wire, SPI CLOCK up to 80MHz
SPI- DUAL/QUAD ADDRSS/DATA R/W	Not Supported	Support 4 or 6-wire, SPI CLOCK up to 80MHz
SQI R/W	Not Supported	Support 6-wire, SPI CLOCK up to 80MHz
Asynchronous **multiplexed** address and data bus interface	Not Supported	Support HBI Multiplexed 1 Phase 8-bit
		Support HBI Multiplexed 1 Phase 16-bit
		Support HBI Multiplexed 2 Phase 8-bit
		Support HBI Multiplexed 2 Phase 16-bit

TABLE 3: PDI COMPARISON (CONTINUED)

PDI Types	ET1100	LAN9252
Asynchronous **de-multiplexed** address and data bus interface	Support 8 bit µController interface	Support HBI Indexed 8-bit
	Support 16 bit µController interface	Support HBI Indexed 16-bit
Synchronous **de-multiplexed** address and data bus interface	Support 8 bit µController interface	Not Supported
	Support 16 bit µController interface	Not Supported

1.4.1 DIGITAL I/O PDI

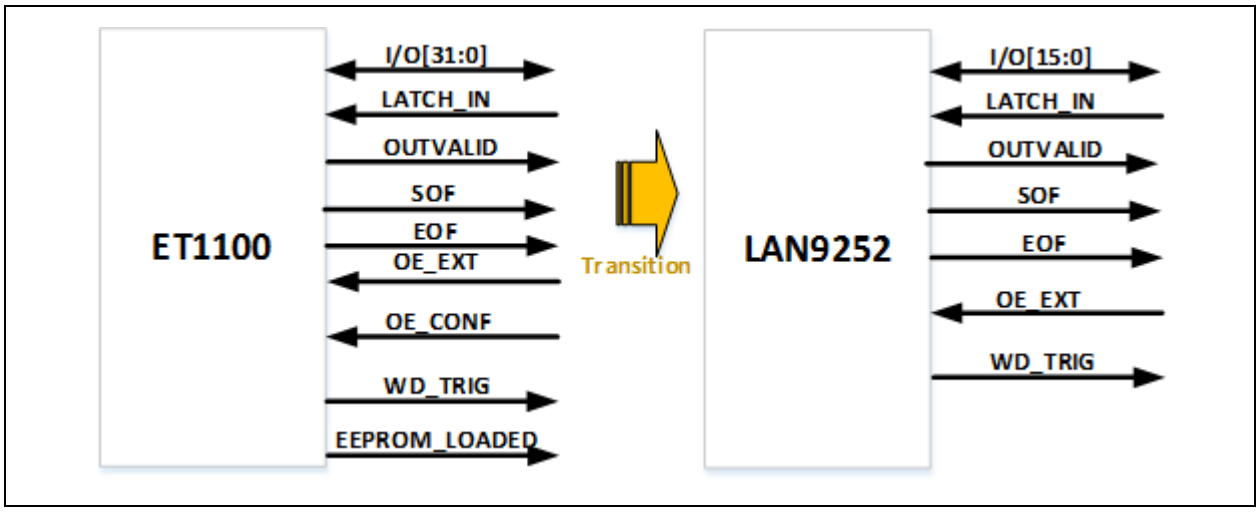
1.4.1.1 Hardware Transition

While transition from ET1100 to LAN9252 in Digital I/O PDI, following things needs to be taken care of.

1. Number of configurable digital I/Os will be reduced from 32 to 16.
2. EEPROM_LOADED pin function is not available in LAN9252.
   a) The EEPROM_LOADED in ET1100 indicates that the PDI is operational.
   b) The EEPROM_LOADED in ET1100 is optional for PDI
3. OE_CONF pin function will not be available in LAN9252. Hence the output driver will be enabled only by using OE_EXT.
   a) OE_CONF in ET1100 controls the output driver's behavior after the output enable signal OE_EXT is set to low or the SyncManager Watchdog is expired.
   b) OE_CONF in ET1100 is ignored in bidirectional mode, I/O will be driven low during output events if OE_EXT is 0 or the watchdog is expired

Figure 5 depicts the hardware transition from ET1100 to LAN9252 in Digital I/O PDI mode.

FIGURE 5: DIGITAL I/O PDI TRANSITION



1.4.2 SYNCHRONOUS DE-MULTIPLEXED BUS INTERFACE

The De-multiplexed Synchronous 8/16bit PDI is only supported by ET1100 and the LAN9252 doesn't support synchronous 8/16bit interface.

Hence the user may choose alternative PDI options such as Asynchronous 8/16 bit multiplexed interface, Asynchronous 8/16 bit de-multiplexed interface or SPI/SQI as discussed in the following sections.

1.4.3 ASYNCHRONOUS DE-MULTIPLEXED BUS INTERFACE

1.4.3.1 Hardware Transition

While transition from ET1100 to LAN9252 in Asynchronous de-multiplexed bus interface, following things needs to be taken care in hardware:

1. 8-bit uController interface
   a) The Asynchronous 8-bit uController interface of ET1100 can be directly replaced with HBI Indexed 8-bit mode of LAN9252
   b) No of address line is reduced from 16 to 5. Since LAN9252 uses indexed addressing mode and the ECAT registers are indirectly accessible through index registers and CSR/FIFO.
2. 16-bit uController interface
   a) The Asynchronous 16-bit uController interface of ET1100 can be directly replaced with HBI Indexed 16-bit mode of LAN9252
   b) No of address line is reduced from 15 to 4. Since LAN9252 uses indexed addressing mode and the ECAT registers are indirectly accessible through index registers and CSR/FIFO.
   c) A[0] in LAN9252 is ignored in 16-bit indexed mode.
3. EEPROM_LOADED pin function is not available in LAN9252.
   a) The EEPROM_LOADED in ET1100 indicates that the PDI is operational.
   b) The EEPROM_LOADED in ET1100 is optional for PDI

Figure 6 depicts the hardware transition from ET1100 to LAN9252 in 8-bit Asynchronous interface.

FIGURE 6: 8-BIT ASYNCHRONOUS BUS INTERFACE TRANSITION

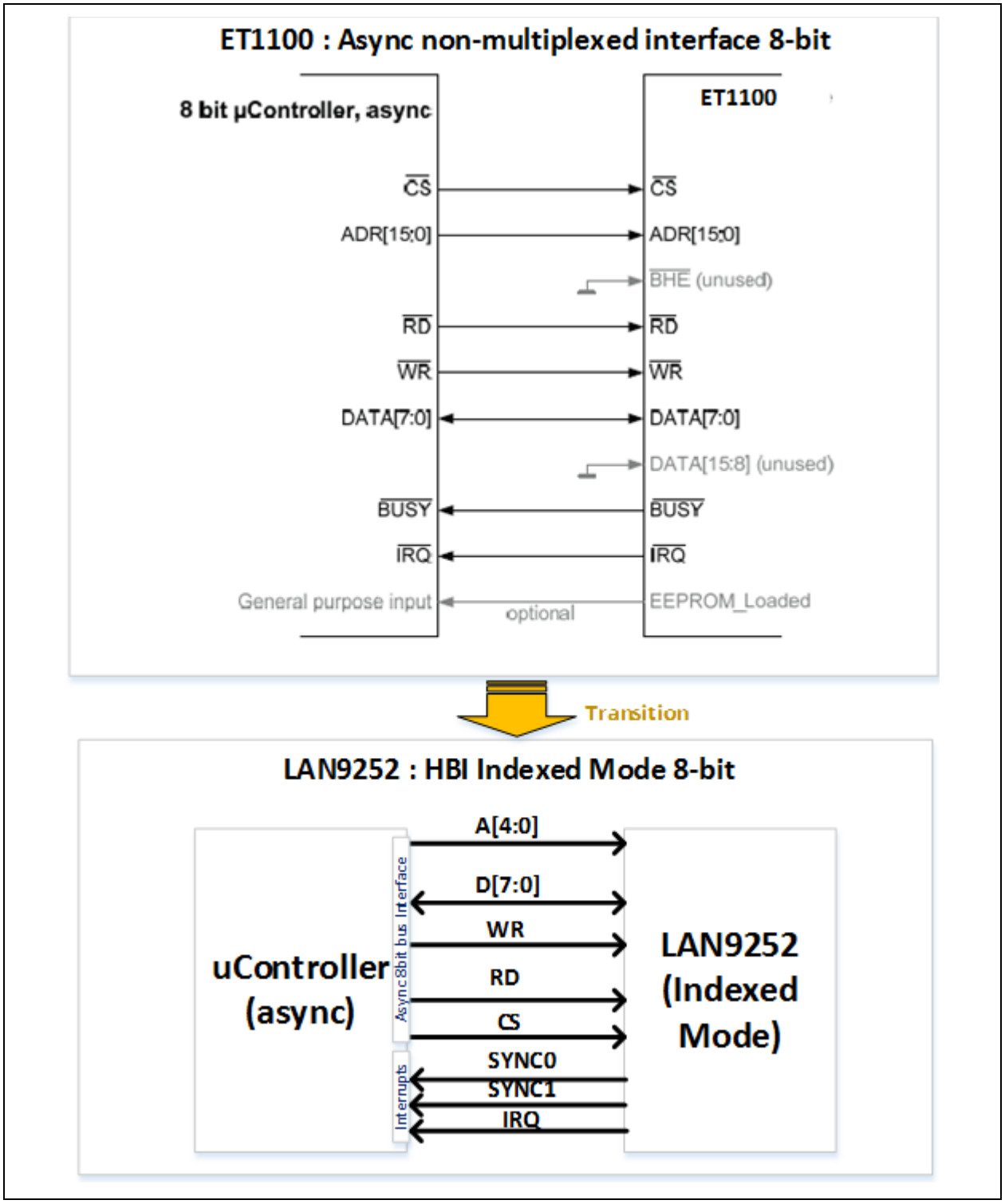
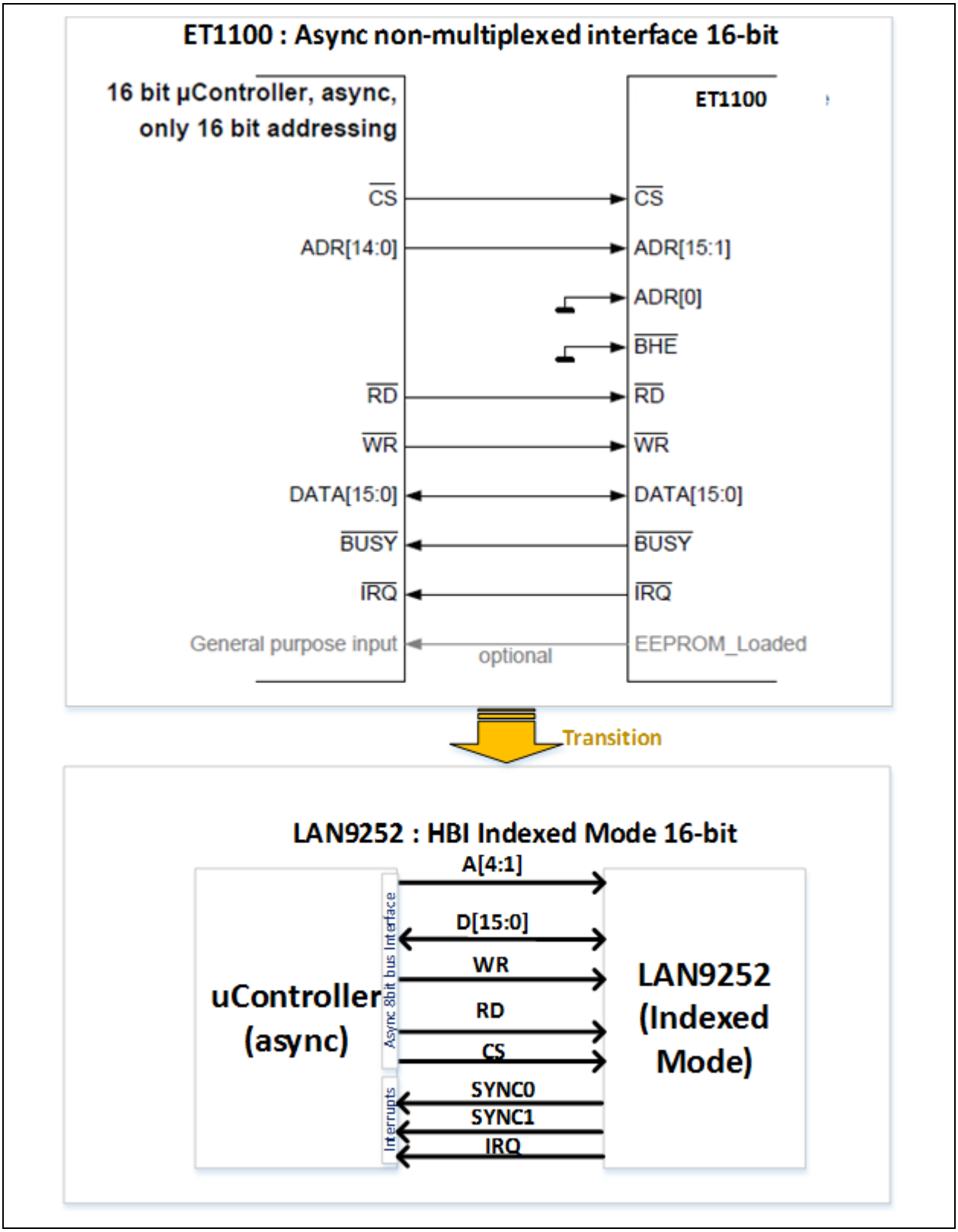


Figure 7 depicts the hardware transition from ET1100 to LAN9252 in 16-bit Asynchronous interface.

FIGURE 7: 16-BIT ASYNCHRONOUS BUS INTERFACE TRANSITION



1.4.3.2 Software Transition

While transition from ET1100 to LAN9252 in Asynchronous de-multiplexed bus interface, following things needs to be taken care in software.

1. PDI type value in the PDI control register “0x0140” is varied between ET1100 and LAN9252.
   a) 8-bit Async uController interface.
      PDI type = 0X09h for ET1100
      PDI type = 0X8Ch for LAN9252
   b) 16-bit Async uController interface.
      PDI type = 0X08h for ET1100
      PDI type = 0X8Dh for LAN9252
2. Addressing mode transition:
   a) The ET1100 uses direct accessing mode
      This allows access to the EtherCAT core registers directly from host without any intermediate FIFOs
      The host needs to send EtherCAT register address via 16 address lines ADR[15:0] (in 8-bit mode) and via 15 address lines ADR[15:1] (in 16-bit mode) to access EtherCAT core registers directly.
   b) The LAN9252 uses in-direct accessing mode
      This allows access to the System CSRs and internal FIFOs and memories
      The ECAT Control and Status Registers (Address range from 0000h to 0FFFh) will be accessed indirectly by using CSR registers.
      The ECAT Process RAM (Address range from 1000h to 1FFFh) will be accessed indirectly by using 16 deep 32-bit wide FIFO
      The host needs to send Index register address via 5 address lines A[4:0] (in 8-bit mode) and via 4 address lines ADR[4:1] (in 16-bit mode) to access EtherCAT core registers indirectly.
      The indexed addressing mode is explained in the following section

1.4.3.2.1 LAN9252: Indexed Address Mode

In Indexed Address mode, access to the internal registers and memory of the device are indirectly mapped using Index and Data registers. The desired internal address is written into the device at a particular offset. The value written is then used as the internal address when the associate Data register address is accessed. Three Index / Data register sets are provided allowing for multi-threaded operation without the concern of one thread corrupting the Index set by another thread. Endianness can be configured per Index / Data pair. Another Data register is provided for access to the FIFOs.

The host address register map is given below Table 4, "HOST BUS INTERFACE INDEXED ADDRESS MODE REGISTER MAP". In 8-bit data mode, the host address input (ADDR[4:0]) is a BYTE address. In 16-bit data mode, ADDR0 is not provided and the host address input (ADDR[4:1]) is a WORD address.

The EtherCAT Process RAM can be accessed directly through FIFOs and the FIFOs are accessed when reading or writing at address 18h-1Bh.

For more detailed timing diagram, refer to LAN9252 Data Sheet “DS00001909A”.

TABLE 4: HOST BUS INTERFACE INDEXED ADDRESS MODE REGISTER MAP

Byte Address	Symbol	Register Name
00h-03h	HBI_IDX_0	Host Bus Interface Index Register 0
04h-07h	HBI_DATA_0	Host Bus Interface Data Register 0
08h-0Bh	HBI_IDX_1	Host Bus Interface Index Register 1
0Ch-0Fh	HBI_DATA_1	Host Bus Interface Data Register 1
10h-13h	HBI_IDX_2	Host Bus Interface Index Register 2
14h-17h	HBI_DATA_2	Host Bus Interface Data Register 2
18h-1Bh	PROCESS_RAM_FIFO	Process RAM Write Data FIFO Process RAM Read Data FIFO
1Ch-1Fh	HBI_CFG	Host Bus Interface Configuration Register

1.4.4 SPI SLAVE INTERFACE

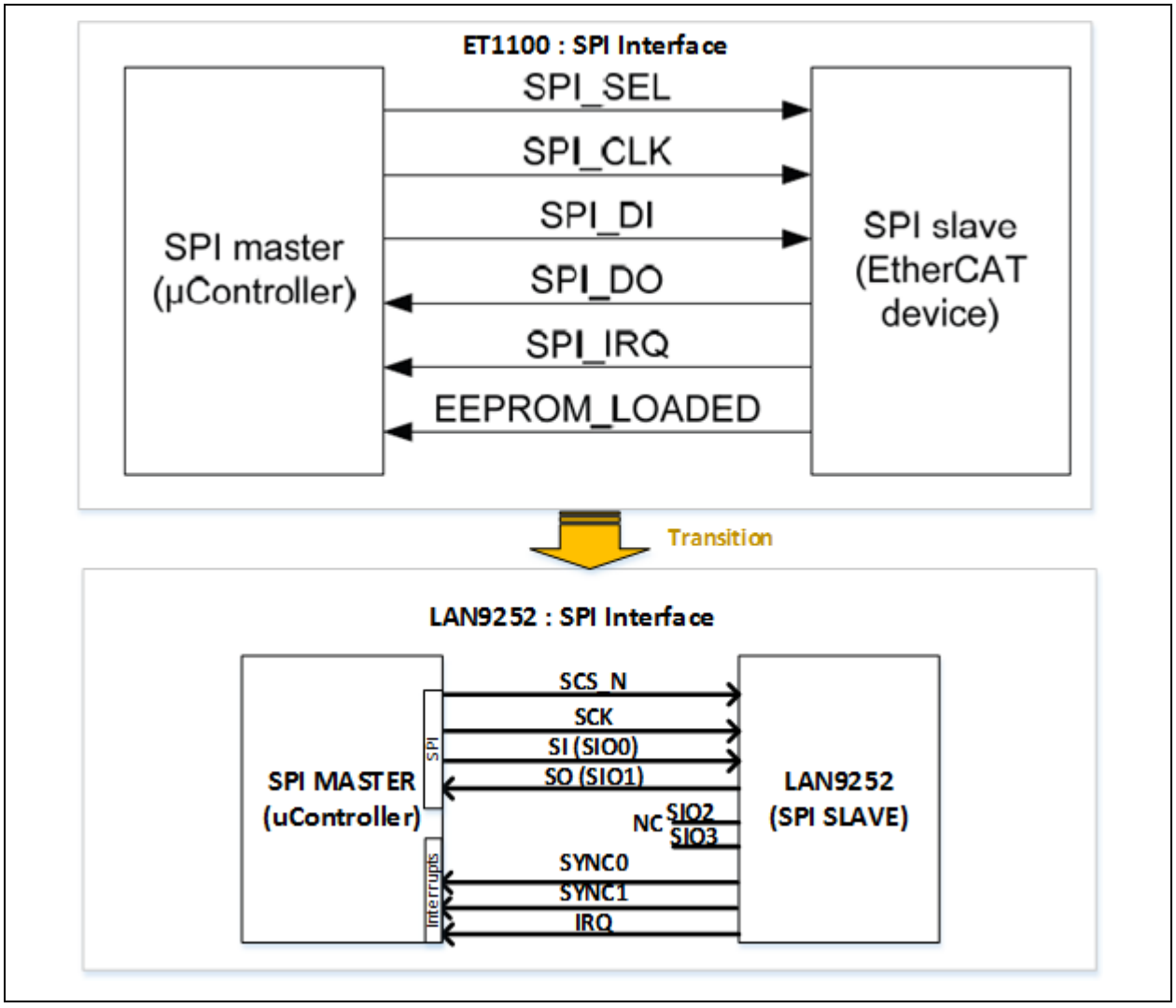
1.4.4.1 Hardware Transition

While transition from ET1100 to LAN9252 in SPI Slave interface, following things needs to be taken care in hardware.

1. EEPROM_LOADED pin function is not available in LAN9252.
   a) The EEPROM_LOADED in ET1100 indicates that the PDI is operational.
   b) The EEPROM_LOADED in ET1100 is optional for PDI
2. SPI_IRQ from ET1100 will be replaced by IRQ signal of LAN9252. The SPI interrupt can be mapped internally to IRQ by using software.
3. When LAN9252 is configured in SPI mode,
   a) Provides an additional 16 GPIOs when Chip Mode Selection is set to 2 Port mode.
   b) Third networking port can be enabled to provide an additional MII port when Chip Mode Selection is set to 3 Port mode.
   c) Above mentioned two modes are explained in following sections.
4. Additional SPI features provided by LAN9252
   a) LAN9252 supports additional SPI PDI types (as listed below) which isn't supported by ET1100.
      DUAL/QUAD SPI Read/Write up to 80MHz
      SQI Read/Write up to 80MHz
   b) By selecting one of these features will reduce SPI access time and will increase throughput performance.
   c) The various SPI modes and Read/Write operation will be controlled by using SPI instructions.

Figure 8 depicts the hardware transition from ET1100 to LAN9252 in SPI Slave interface.

FIGURE 8: SPI SLAVE INTERFACE TRANSITION

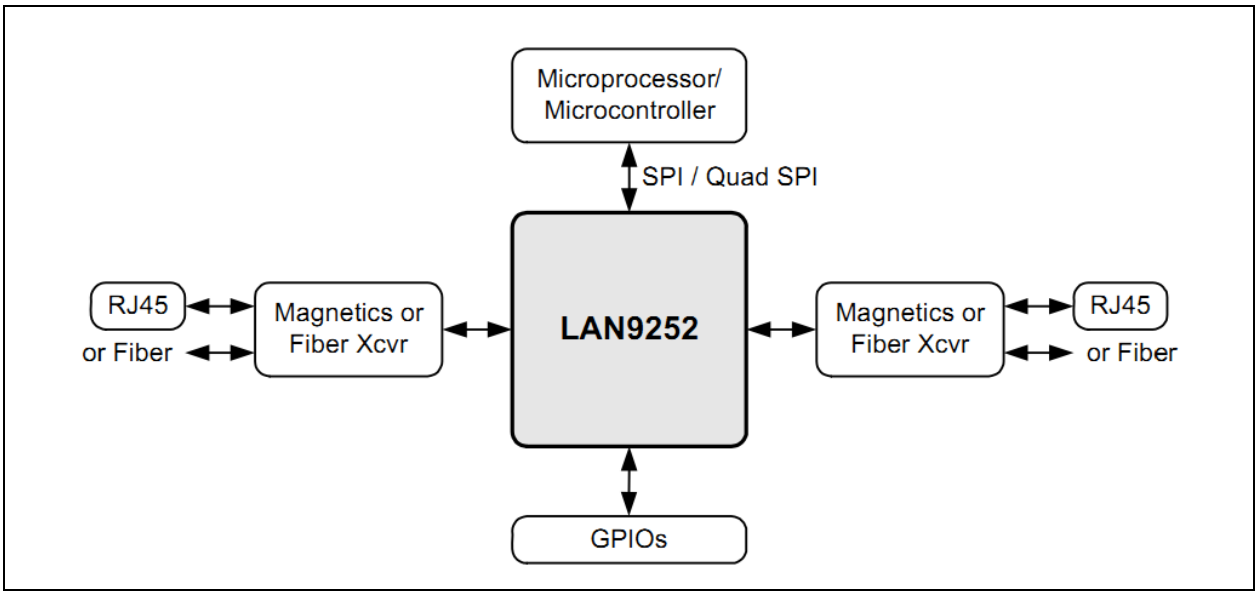


1.4.4.1.2 LAN9252: SPI + GPIOs

While the LAN9252 is configured in SPI mode, it also provides an additional 16 GPIOs when Chip Mode Selection is set to 2 Port mode (as shown below in Figure 9).

Note:	Chip Mode Selection is explained in Section 1.3, "Chip Modes," on page 5.

FIGURE 9: LAN9252 PDI WITH SPI + 16 GPIOS



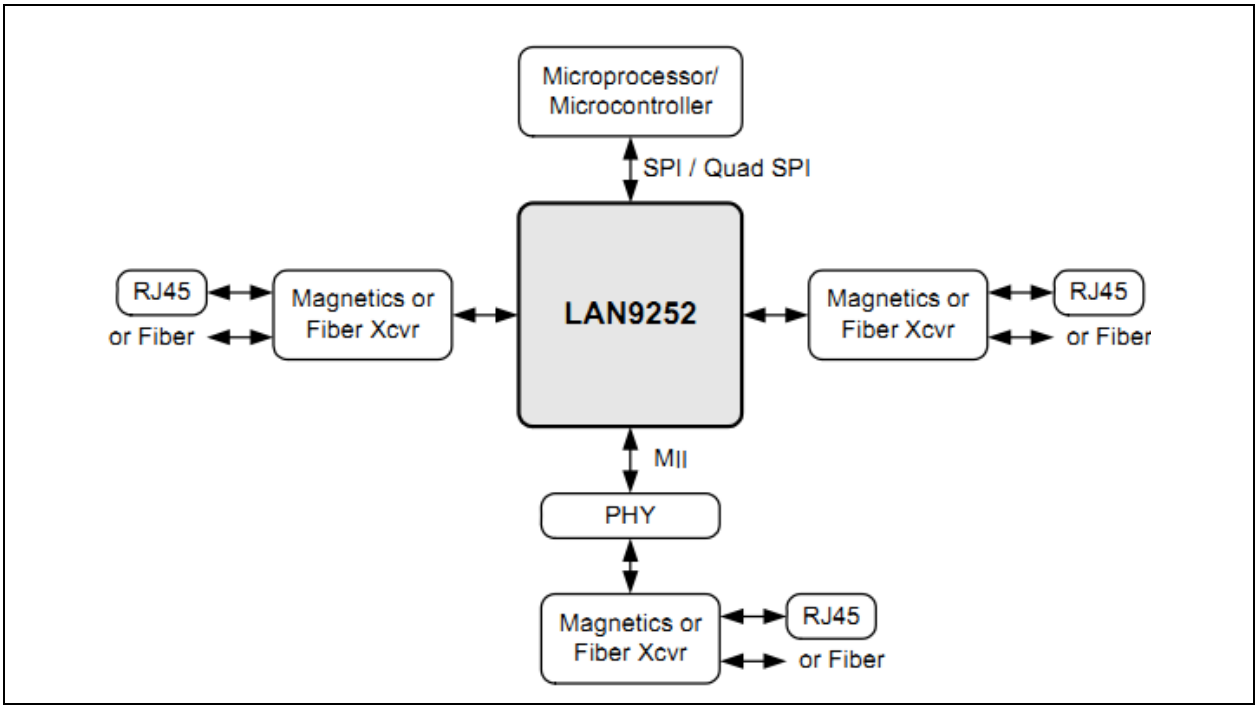
1.4.4.1.3 LAN9252: Expansion Mode (SPI + MII)

While the LAN9252 is configured in SPI mode, a third networking port can be enabled to provide an additional MII port when Chip Mode Selection is set to 3 Port mode (as shown below in Figure 10).

This port can be connected to an external PHY, to enable star or tree network topologies, or to another LAN9252 to create a four port solution. This port can be configured for the upstream or downstream direction.

Note: Chip Mode Selection is explained in Section 1.3, "Chip Modes," on page 5.

FIGURE 10: LAN9252 PDI WITH SPI + MII



1.4.4.2 Software Transition

While transition from ET1100 to LAN9252 in SPI Slave interface, following things needs to be taken care in software

1. PDI type value in the PDI control register “0x0140” is different between ET1100 and LAN9252.
   a) PDI type = 0X05 for ET1100
   b) PDI type = 0X80 for LAN9252
2. EtherCAT core registers accessing mode transition:
   a) The ET1100 uses direct accessing mode
      This allows access to the EtherCAT core registers directly from host without any intermediate FIFOs
   b) The LAN9252 uses indirect accessing mode
      This allows access to the System CSRs and internal FIFOs and memories
      The ECAT Control and Status Registers (Address range from 0000h to 0FFFh) will be accessed indirectly by using CSR registers.
      The ECAT Process RAM (Address range from 1000h to 1FFFh) will be accessed indirectly by using 16 deep 32-bit wide FIFO
3. Due to indirect accessing mode, the LAN9252 requires additional steps than ET1100 as shown in the following flow diagrams.

Figure 11 depicts the Software transition from ET1100 to LAN9252 in Control and Status registers Read Access over SPI Slave interface.

FIGURE 11: ET1100 TO LAN9252 ECAT CONTROL AND STATUS REGISTERS READ ACCESS TRANSITION OVER SPI

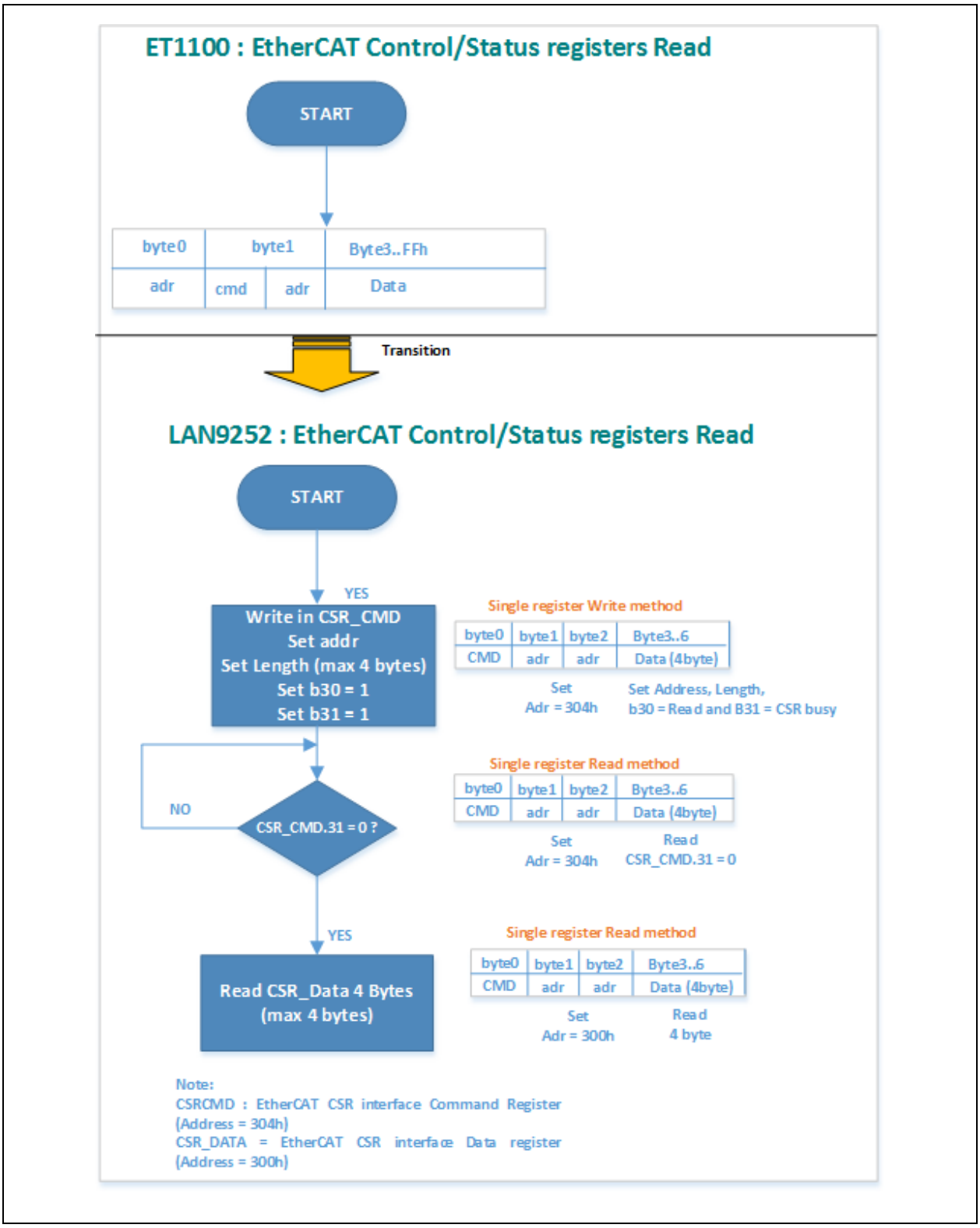


Figure 12 depicts the Software transition from ET1100 to LAN9252 in Control and Status registers Write Access over SPI Slave interface.

FIGURE 12: ET1100 TO LAN9252 ECAT CONTROL AND STATUS REGISTERS WRITE ACCESS TRANSITION OVER SPI

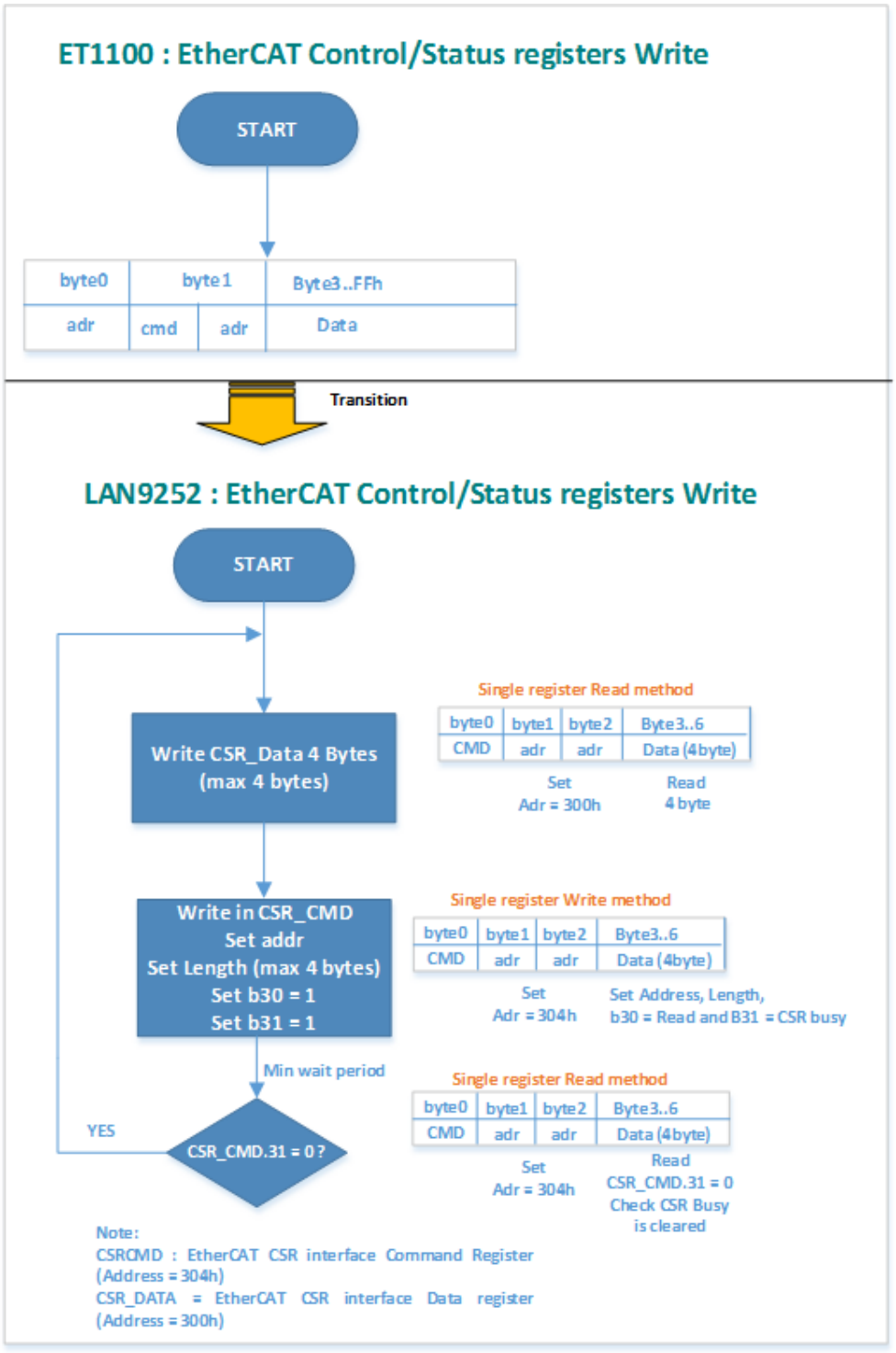


Figure 13 depicts the Software transition from ET1100 to LAN9252 in Process RAM Read Access over SPI Slave interface (Example: Read 6 bytes of process data over SPI).

FIGURE 13: ET1100 TO LAN9252 ECAT PROCESS RAM READ ACCESS TRANSITION OVER SPI

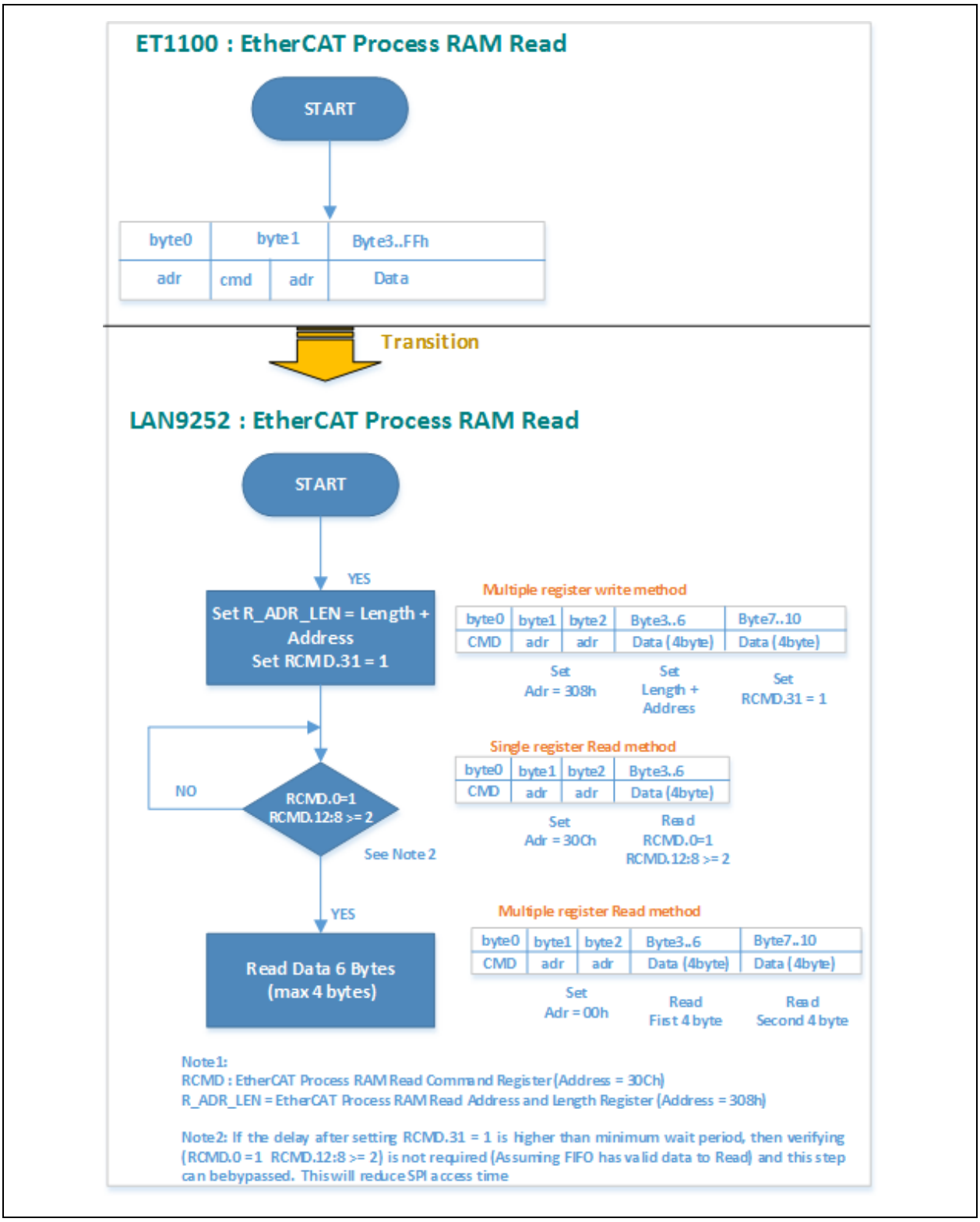
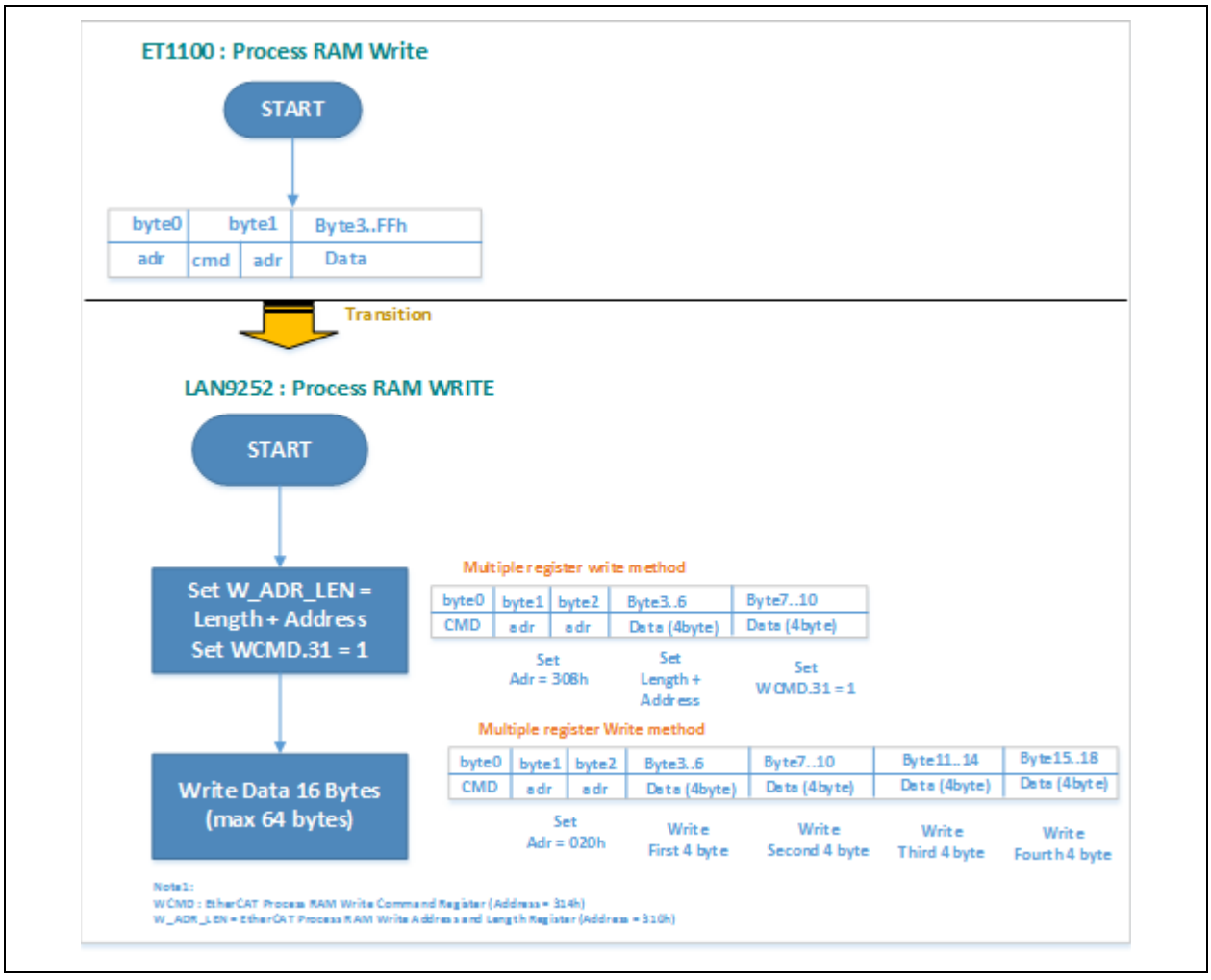


Figure 14 depicts the Software transition from ET1100 to LAN9252 in Process RAM Write Access over SPI Slave interface (Example: writes 16 bytes of process data over SPI).

FIGURE 14: ET1100 TO LAN9252 ECAT PROCESS RAM WRITE ACCESS TRANSITION OVER SPI



1.4.5 ASYNCHRONOUS MULTIPLEXED BUS INTERFACE

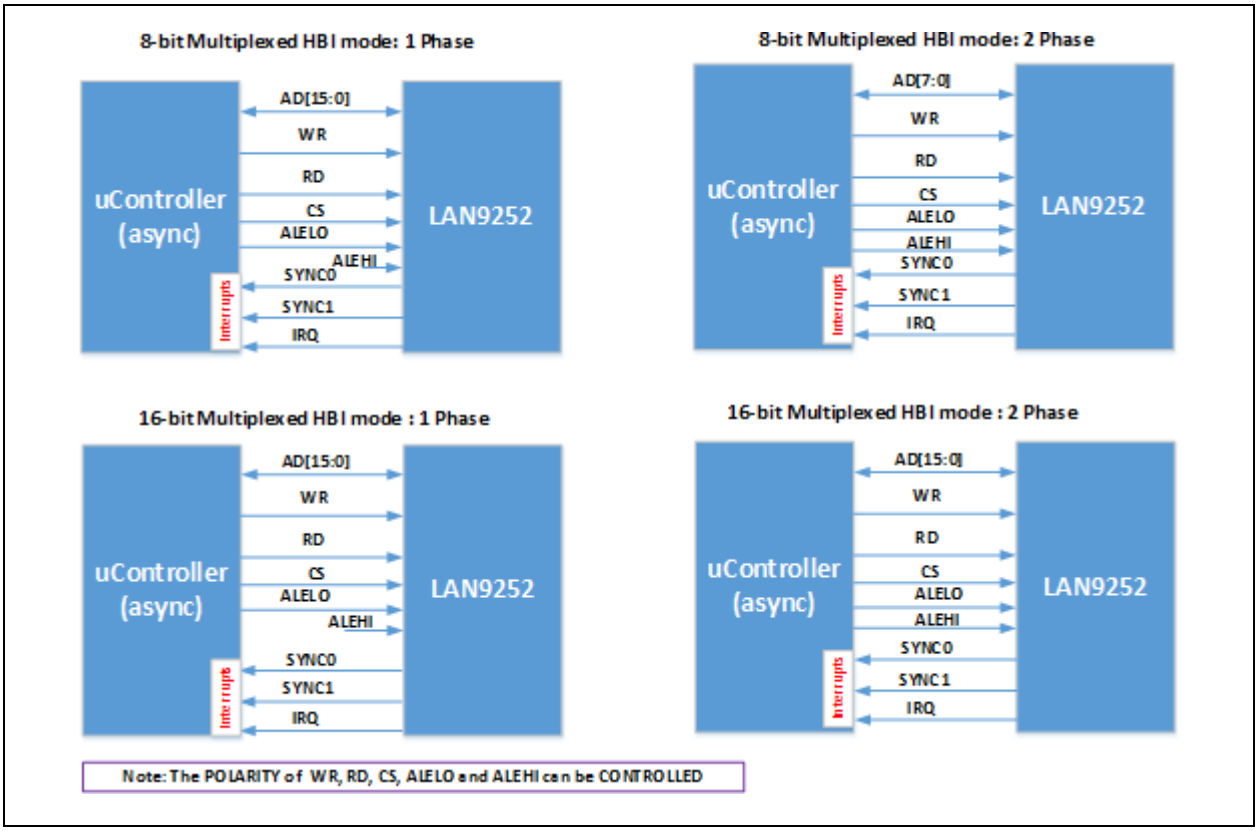
The LAN9252 also supports Asynchronous multiplexed 8/16bit PDI which doesn't supported by ET1100.

Hence the user can also select any one of PDI options listed below if the host is supported.

1. 8-bit Multiplexed HBI mode – 1 Phase
2. 16-bit Multiplexed HBI mode – 1 Phase
3. 8-bit Multiplexed HBI mode – 2 Phase
4. 16-bit Multiplexed HBI mode – 2 Phase

Figure 15 depicts the hardware connections between uController and LAN9252 in various Multiplexed HBI modes.

FIGURE 15: LAN9252 HARDWARE CONNECTIONS IN VARIOUS MULTIPLEXED HBI MODES



1.4.6 DUAL/QUAD AND SQI SLAVE INTERFACE

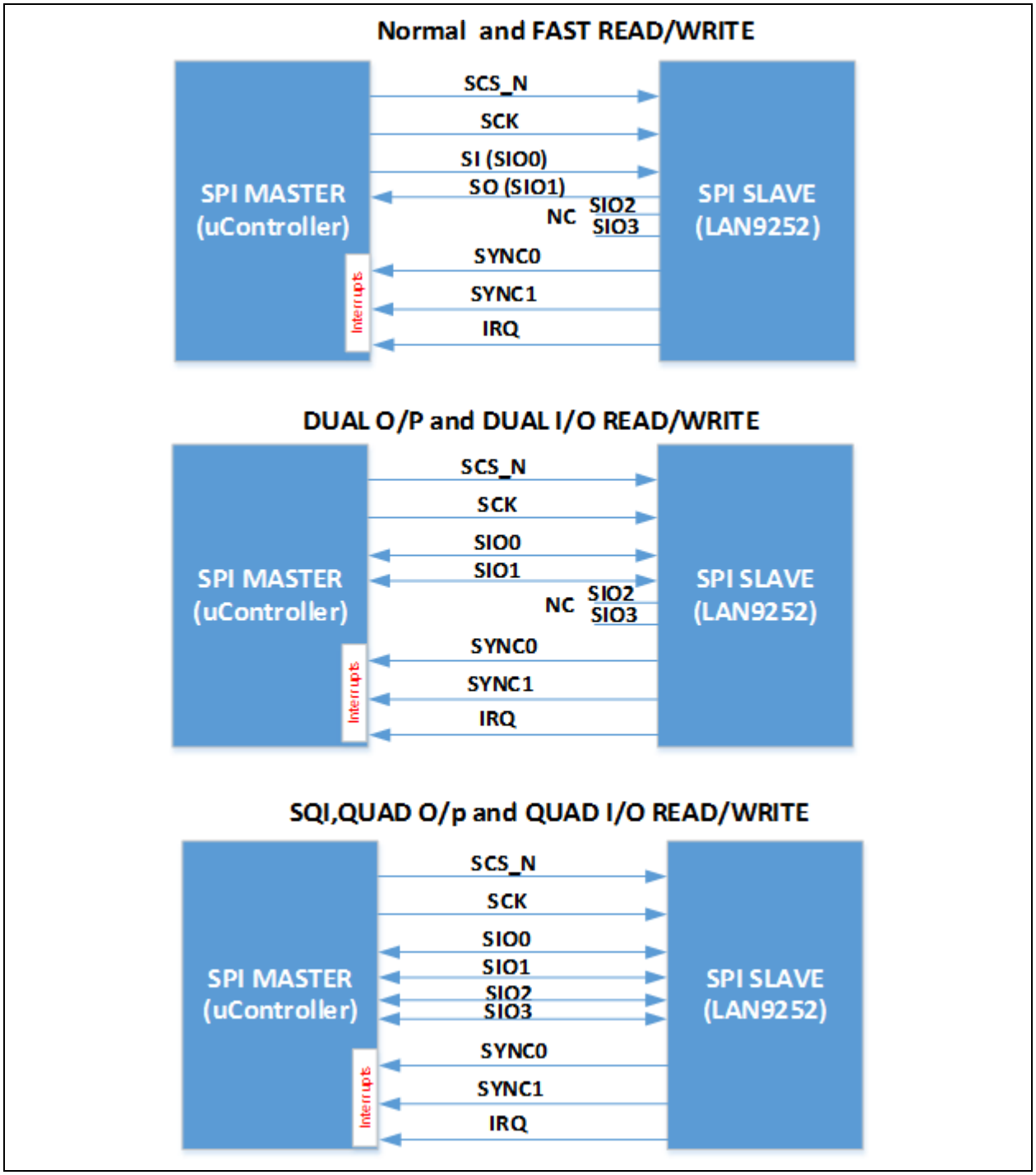
The LAN9252 also supports high speed Dual/Quad SPI and SQI (up to 80MHz) which doesn't supported by ET1100.

Hence the user can also select any one of SPI PDI options listed below if the host is supported. This will reduce SPI access time based on the faster SPI frequency and number of SPI lines used for sharing data (2 lines for DUAL SPI, 4 lines for QUAD and SQI)

1. FAST SPI
2. DUAL Output OR DUAL I/O SPI
3. QUAD Output OR QUAD I/O SPI
4. SQI

Figure 16 depicts the hardware connections between uController and LAN9252 in various SPI modes.

FIGURE 16: LAN9252 HARDWARE CONNECTIONS IN VARIOUS SPI MODES



2.0 SOFTWARE TRANSITION

This section details the software transitions in relation to the Process Data Interfaces (PDI).

Porting firmware from the ET1100 to the LAN9252 is simplified by the effective abstraction of the EtherCAT slave stack architecture. The HAL (Hardware Abstraction Layer) provides hooks (Application Programming Interface) to the middle-ware and application layers of the EtherCAT stack, thus encapsulating the hardware changes and mitigating the burden of porting applications to various hardware platforms. Therefore, simply making LAN9252-specific modifications to the HAL layer allows the application to run effectively as if it was an ET1100.

For PIC32 users:

Please refer to *AN1916 Integrating Microchip's LAN9252 SDK with Beckhoff's EtherCAT SSC* for details on modifying the HAL for the LAN9252.

For other SoC users:

Please refer to the LAN9252 datasheet to modify the HAL for the LAN9252.

2.1 Slave Configuration Header (ecat_def.h)

A list of the defined hardware settings is located in the ecat_def.h header file. The following changes should be made to it:

1. The mailbox and PDRAM read/write sizes must be changed per the LAN9252 specification, as shown in Figure 17.

FIGURE 17: ECAT_DEF.H MAILBOX & PDRAM READ/WRITE SIZE EDITS

```
/**
MAX_PD_WRITE_ADDRESS: Maximum address for the process output data (Sync Manager
inside the application memory of the EtherCAT Slave Controller which could be se
#ifndef MAX_PD_WRITE_ADDRESS
#define MAX_PD_WRITE_ADDRESS    0x1FFF
#endif

/**
MAX_PD_READ_ADDRESS: Maximum address for the process input data (Sync Mar
inside the application memory of the EtherCAT Slave Controller which coul
#ifndef MAX_PD_READ_ADDRESS
#define MAX_PD_READ_ADDRESS     0x1FFF
#endif

/**
MAX_MBX_WRITE_ADDRESS: Maximum address for the write (receive) mailbox (Sync Man
#ifndef MAX_MBX_WRITE_ADDRESS
#define MAX_MBX_WRITE_ADDRESS   0x1FFF
#endif

/**
MAX_MBX_READ_ADDRESS: Maximum address for the read (send) mailbox (Sync Manager
#ifndef MAX_MBX_READ_ADDRESS
#define MAX_MBX_READ_ADDRESS    0x1FFF
#endif
```

2. The ESC EEPROM Emulation must be disabled for the LAN9252, as shown in Figure 18.

FIGURE 18: ECAT_DEF.H ESC EEPROM EMULATION DISABLE EDIT

```
/**
ESC_EEPROM_EMULATION: If this switch is set EEPROM emulation is supported. Not a
#ifndef ESC_EEPROM_EMULATION
#define ESC_EEPROM_EMULATION                    0 //This define was already ev
#endif
```

2.2 Interrupt Configuration

If AL_EVENT_ENABLED or DC_SUPPORTED is defined as 1 in the existing ET1100 firmware, the following steps must be followed:

1. Set the same interrupt polarity for the LAN9252 and PIC24. For example, if the PIC24 ESC interrupt line is configured as negative edge, then the LAN9252 IRQ line should be configured as Active low. Refer to the HW_Init() API in 9252_HW.c from the LAN9252 SDK.

FIGURE 19: INTERRUPT CONFIGURATION

```
    //IRQ enable,IRQ polarity, IRQ buffer type in Interrupt Configuration regist
    //Write 0x54 - 0x00000101
    data = 0x00000101;

#ifndef USE_SPI
    #if defined(HBI_INDEXED_16BIT) | defined(HBI_INDEXED_8BIT)
        PMPWriteDWord (0,0x54);
        PMPWriteDWord (4,data);
    #else
        PMPWriteDWord (0x54, data);
    #endif
#else
    SPIWriteDWord (0x54, data);
#endif
```

2. The SYNC0/SYNC1 interrupt polarity should also be configured for both the LAN9252 and PIC24. For example, if the PIC24 SYNC0/SYNC1 line is configured as negative edge, then the LAN9252 SYNC0/SYNC1 should be configured as active low. The SYNC0/SYNC1 configuration can be changed via EEPROM, as shown in Table 5.

TABLE 5: SYNC0/SYNC1 EEPROM CONFIGURATION

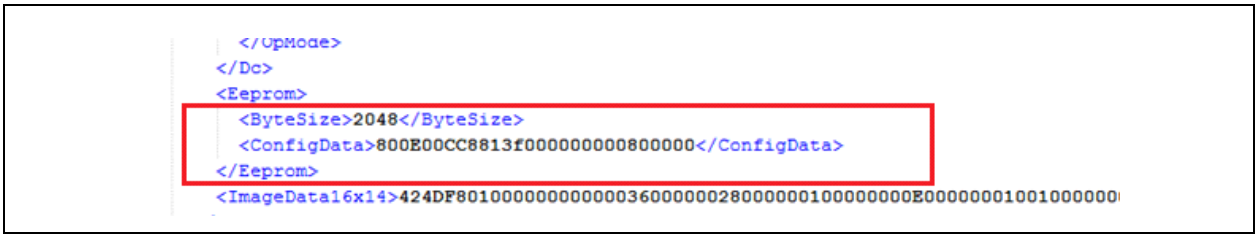
Sync/Latch PDI Configuration Register (0151h)	SYNC1 Map	1 / [15]
	SYNC1/LATCH1 Configuration	1 / [14]
	SYNC1 Output Driver/Polarity	1 / [13:12]
	SYNC0 Map	1 / [11]
	SYNC0/LATCH0 Configuration	1 / [10]
	SYNC0 Output Driver/Polarity	1 / [9:8]

2.3 ESI File

The ESC configuration differs between the LAN9252 and the ET1100. Therefore, the following changes must be made to the ESI file:

1. Open the ET1100 ESI file to be changed.
2. Find “ConfigData” in the XML file, change it as shown in Figure 20, and save the file.

FIGURE 20: ESI CONFIGDATA EDIT



Refer to the LAN9252 datasheet for details on modifying the LAN9252 EEPROM contents.

2.4 SPI Slave Controller

SPI commands differ between LAN9252 and ET1100. Therefore, appropriate changes must be made to the SPI driver.

2.4.1 ET1100 SPI ADDRESS MODES

The SPI slave interface supports two address modes: 2-Byte Addressing Mode and 3-Byte Addressing Mode. With 2-byte addressing, the lower 13 address bits A[12:0] are selected by the SPI master, while the upper 3 bits A[15:13] are assumed to be 000b inside the SPI slave, thus only the first 8 Kbyte in the EtherCAT slave address space can be accessed. 3-byte addressing is used for accessing the whole 64 Kbyte address space of an EtherCAT slave. A summary of these modes is provided in Table 6.

TABLE 6: ET1100 ADDRESS MODES

Byte	2-Byte Address Mode		3-Byte Address Mode	
0	A[12:5]	Address Bits [12:5]	A[12:5]	Address Bits [12:5]
1	A[4:0] CMD0[2:0]	Address Bits [4:0] Read/Write Command	A[4:0] CMD0[2:0]	Address Bits [4:0] Read/Write Command
2	D0[7:0]	Data Byte 0	A[15:13] CMD1[2:0] res[1:0]	Address Bits [15:13] Read/Write Command Reserved Bits (Set to 00b)
3	D1[7:0]	Data Byte 1	D0[7:0]	Data Byte 0
4	D2[7:0]	Data Byte 2	D1[7:0]	Data Byte 1

2.4.2 ET1100 SPI COMMANDS

The CMD0 command in the second address/command byte (Table 6) may be READ, READ with following Wait State bytes, WRITE, NOP, or Address Extension. A summary of these commands is provided in Table 7.

TABLE 7: ET1100 SPI COMMANDS

CMD[2]	CMD[1]	CMD[0]	Command
0	0	0	NOP (No Operation)
0	0	1	Reserved
0	1	0	Read
0	1	1	Read with following Wait State Bytes
1	0	0	Write

TABLE 7: ET1100 SPI COMMANDS (CONTINUED)

CMD[2]	CMD[1]	CMD[0]	Command
1	0	1	Reserved
1	1	0	Address Extension (3 Address/Command Bytes)
1	1	1	Reserved

2.4.3 LAN9252 SPI

In SPI mode, the 8-bit instruction is started on the first rising edge of the input clock after SCS# goes active. The instruction is always input serially on SI/SIO0.

For read and write instructions, two address bytes follow the instruction byte. Depending on the instruction, the address bytes are input either serially, or 2/4 bits per clock. Although all registers are accessed as DWORDs, the address field is considered a byte address. Fourteen address bits specify the address. Bits 15 and 14 of the address field specify that the address is auto-decremented (10b) or auto-incremented (01b) for continuous accesses.

Table 8 details the available LAN9252 SPI commands.

TABLE 8: LAN9252 SPI COMMANDS

Instruction	Description	Bit Width	INST Code	ADDR Bytes	DUMMY Bytes	Data Bytes
Configuration						
EQIO	Enable SQI	1-0-0	38h	0	0	0
RSTQIO	Reset SQI	1-0-0	FFh	0	0	0
Read						
READ	Read	1-1-1	03h	2	0	4 to ∞
FASTRE	Read at higher speed	1-1-1	0Bh	2	1	4 to ∞
SDOR	SPI dual output read	1-1-2	3Bh	2	1	4 to ∞
SDIOR	SPI dual IO read	1-2-2	BBh	2	2	4 to ∞
SQOR	SPI quad output read	1-1-4	6Bh	2	1	4 to ∞
SQIOR	SPI quad IO read	1-4-4	EBh	2	4	4 to ∞
Write						
WRITE	Write	1-1-1	02h	2	0	4 to ∞
SDDW	SPI dual data write	1-1-2	32h	2	0	4 to ∞
SDADW	SPI dual addr/data write	1-2-2	B2h	2	0	4 to ∞
SQDW	SPI quad data write	1-1-4	62h	2	0	4 to ∞
SQADW	SPI quad addr/data write	1-4-4	E2h	2	0	4 to ∞

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001907C (01-25-16)	Throughout document.	Fixed incorrect references from ET100 to ET1100.
	Section , "Functional Overview," on page 1	Updated first and fourth paragraphs.
	Section 1.0, "Hardware Transition," on page 2	Fixed grammar.
	Table 1, “ESC Main Feature Comparison,” on page 2	Fixed spacing issues in several cells.
	Section 1.1, "EtherCAT CSR and Process Data RAM Access," on page 4	Fixed grammar.
	Table 3, “PDI comparison,” on page 5	Fixed spacing issues in several cells.
	Section 1.4.1.1, "Hardware Transition," on page 6	Fixed incorrect information in item 1. Fixed grammar.
	Section 1.4.3.1, "Hardware Transition," on page 7	Fixed grammar. Changed all instances of “No” to “Number.”
	Section 1.4.3.2, "Software Transition," on page 10	Changed all instances of “X” (capital letter) to “x” (small letter).
	FIGURE 10: LAN9252 PDI with SPI + MII on page 14	Updated Figure title.
	Section 1.4.4.1, "Hardware Transition," on page 11	Fixed spacing issues.
	Section 1.4.4.1.2, "LAN9252: SPI + GPIOs," on page 13	Updated note so reference/link to Section 1.3, "Chip Modes," on page 5 works.
	Section 1.4.4.1.3, "LAN9252: Expansion Mode (SPI + MII)," on page 14	Updated note so reference/link to Section 1.3, "Chip Modes," on page 5 works.
	Section 1.4.4.2, "Software Transition," on page 14	Changed all instances of “X” (capital letter) to “x” (small letter). Updated item 3.
	FIGURE 12: ET1100 to LAN9252 ECAT Control and Status Registers Write Access Transition Over SPI on page 16	Updated Figure title.
	FIGURE 13: ET1100 to LAN9252 ECAT Process RAM Read Access Transition Over SPI on page 17	Updated Figure title. Updated figure.

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
DS00001907C (01-25-16) [continued]	FIGURE 14: ET1100 to LAN9252 ECAT Process RAM Write Access Transition Over SPI on page 18	Updated Figure title.
	Section 1.4.5, "Asynchronous multiplexed bus Interface," on page 18	Fixed grammar.
	Section 1.4.6, "Dual/QUAD and SQI slave Interface," on page 19	Fixed grammar.
	Section 2.0, "Software Transition," on page 21	Updated second and last paragraphs.
	FIGURE 16: LAN9252 Hardware Connections In Various SPI Modes on page 20	Fixed distorted image.
	Section 2.1, "Slave Configuration Header (ecat_def.h)," on page 21	Added note.
	Section 2.2, "Interrupt Configuration," on page 22	Added note.
DS00001907B (08-27-15)	Operating Modes and Process Data Interface (PDI) Selection and Configuration	Sections removed and replaced with Section 1.4, "Process Data Interface (PDI)"
	Table 1, "ESC Main Feature Comparison"	Table modified.
	Figure 3, "LAN9252 ESC Block Diagram"	Figure modified.
	Slave Configuration Header (ecat_def.h), Interrupt Configuration, and ESI File	Added new sections.
DS00001907A (03-19-15)	Initial release.	

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

ISBN: 978-1-5224-0212-1

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

07/14/15