TC7662A

Charge Pump DC-to-DC Converter

Features

- Wide Operating Range
  - 3V to 18V
- Increased Output Current (40 mA)
- Pin Compatible with ICL7662/SI7661/TC7660/LTC1044
- No External Diodes Required
- Low Output Impedance @ I_L = 20 mA
  - 40Ω Typ.
- No Low-Voltage Terminal Required
- CMOS Construction
- Available in 8-Pin PDIP and 8-Pin CERDIP Packages

Applications

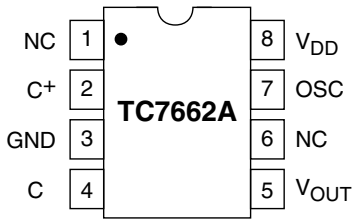
- Laptop Computers
- Disk Drives
- Process Instrumentation
- µP-based Controllers

Device Selection Table

Part Number	Package	Operating Temp. Range
TC7662ACPA	8-Pin PDIP	0°C to +70°C
TC7662AEPA	8-Pin PDIP	-40°C to +85°C
TC7662AIJA	8-Pin CERDIP	-25°C to +85°C
TC7662AMJA	8-Pin CERDIP	-55°C to +125°C

Package Type

8-Pin PDIP
8-Pin CERDIP

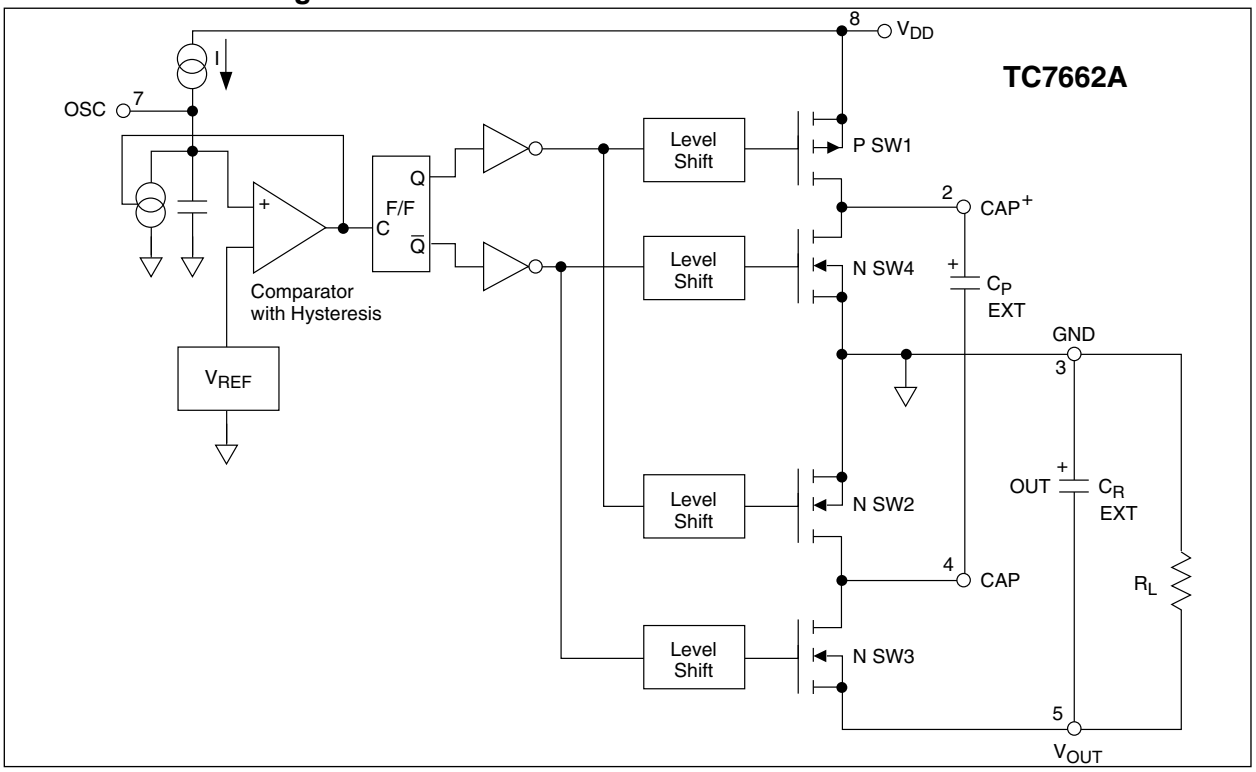


General Description

The TC7662A is a pin-compatible upgrade to the industry standard TC7660 charge pump voltage converter. It converts a +3V to +18V input to a corresponding -3V to -18V output using only two low-cost capacitors, eliminating inductors and their associated cost, size and EMI. In addition to a wider power supply input range (3V to 18V versus 1.5V to 10V for the TC7660), the TC7662A can source output currents as high as 40 mA. The on-board oscillator operates at a nominal frequency of 12 kHz. Operation below 12 kHz (for lower supply current applications) is also possible by connecting an external capacitor from OSC to ground.

The TC7662A is recommended for designs requiring greater output current and/or lower input/output voltage drop. It is available in 8-pin PDIP and CERDIP packages in commercial and extended temperature ranges.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage V_{DD} to GND ..... +18V
Input Voltage (Any Pin) ..... (V_{DD} + 0.3) to (V_{SS} – 0.3)
Current into Any Pin ..... 10 mA
Output Short Circuit ..... Continuous (at 5.5V Input)
ESD Protection ..... ±2000V
Package Power Dissipation ($T_A \leq 70°C$)
- 8-Pin CERDIP ..... 800 mW
- 8-Pin PDIP ..... 730 mW

Package Thermal Resistance
- CPA, EPA θ_{JA} ..... 140°C/W
- IJA, MJA θ_{JA} ..... 90°C/W

Operating Temperature Range
- C Suffix ..... 0°C to +70°C
- I Suffix ..... -25°C to +85°C
- E Suffix ..... -40°C to +85°C
- M Suffix ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = 15V, T_A = +25°C, Test circuit (Figure 3-1) unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply Voltage	V_{DD}	3	—	18	V	
Supply Current	I_S	—	—	—	µA	$R_L = \infty$
		—	510	700		V_{DD} = +15V
		—	560	—		0°C ≤ T_A ≤ +70°C
		—	650	—		-55°C ≤ T_A ≤ +125°C
		—	190	—		V_{DD} = +5V
		—	210	—		0°C ≤ T_A ≤ +70°C
		—	210	—		-55°C ≤ T_A ≤ +125°C
Output Source Resistance	R_O	—	40	50	Ω	I_L = 20 mA, V_{DD} = +15V
		—	50	60		I_L = 40 mA, V_{DD} = +15V
		—	100	125		I_L = 3 mA, V_{DD} = +5V
Oscillator Frequency	F_{OSC}	—	12	—	kHz	
Switching Frequency	F_{SW}	—	6	—	kHz	**Note 1**
Power Efficiency	P_{EFF}	93	97	—	%	V_{DD} = +15V
		—	—	—		R_L = 2 kΩ
Voltage Efficiency	V_{EFF}	99	99.9	—	%	V_{DD} = +15V
		—	—	—		$R_L = \infty$
		96	—	—		Over operating temperature range.

Note 1: The pump switching frequency with external clocking, as with internal clocking, will be 1/2 of the oscillator frequency.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, CERDIP)	Symbol	Description
1	NC	No connection
2	C^+	Charge pump capacitor positive terminal
3	GND	Ground terminal
4	C^-	Charge pump capacitor negative terminal
5	V_{OUT}	Output voltage
6	NC	No connection
7	OSC	Oscillator control input. Bypass with an external capacitor to slow the oscillator
8	V_{DD}	Power supply positive voltage input

3.0 DETAILED DESCRIPTION

The TC7662A is a capacitive charge pump (sometimes called a switched-capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional block diagram shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C_P to the supply voltage, V_{DD}. This assumes that the ON resistance of the MOSFETs in series with the capacitor produce a charging time (3 time constants) less than the ON time provided by the oscillator frequency, as shown in Equation 3-1:

EQUATION 3-1:

$$3(R_{DS(ON)} \times C_P) < \frac{C_P}{0.5 f_{OSC}}$$

In the next cycle, SW1 and SW2 are turned OFF and, after a very short interval with all switches OFF (preventing large currents from occurring due to cross conduction), SW3 and SW4 are turned ON. The charge in C_P is then transferred to C_R, *but with the polarity inverted*. In this way, a negative voltage is derived.

An oscillator supplies pulses to a flip-flop that is fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has a pin that controls the frequency of oscillation. Pin 7 can have a capacitor added that is connected to ground. This will lower the frequency of the oscillator by adding capacitance to the internal timing capacitor of the TC7662A (see Figure 5-4).

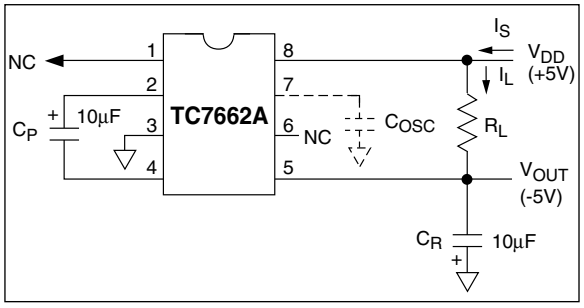


FIGURE 3-1: *TC7662A Test Circuit.*

3.1 Theoretical Power Efficiency Considerations

In theory, a voltage converter can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7662A approaches these conditions for negative voltage conversion if large values of C_P and C_R are used.

Note:	Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.

The energy lost is defined by:

EQUATION 3-2:

$$E = \frac{1}{2} \times C_P (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_P during the pump and transfer cycles. If the impedances of C_P and C_R are relatively high at the pump frequency (refer to Figure 3-1), compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is desirable not only to make C_R as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_P in order to achieve maximum efficiency of operation.

3.2 Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_P must be connected to pin 2 of the TC7662A and the + terminal of C_R must be connected to GND (pin 3).
- If the voltage supply driving the TC7662A has a large source impedance (25-30Ω), then a 2.2 µF capacitor from pin 8 to ground may be required to limit the rate of rise of the input voltage to less than 2V/µs.

4.0 TYPICAL APPLICATIONS

4.1 Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the TC7662A for generation of negative supply voltages. Figure 4-1 shows typical connections to provide a negative supply where a positive supply of +3V to +18V is available.

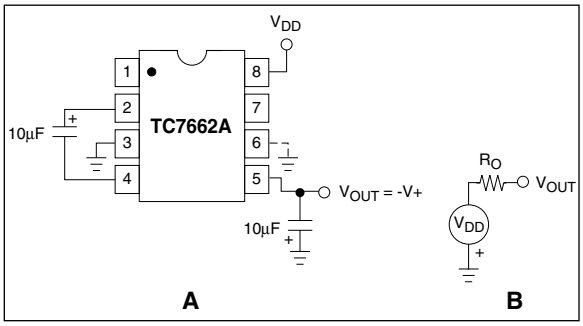


FIGURE 4-1: *Simple Negative Converter and its Output Equivalent.*

The output characteristics of the circuit in Figure 4-1 are those of a nearly ideal voltage source in series with a resistance as shown in Figure 4-1b. The voltage source has a value of -(V_{DD}). The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in the Functional Block Diagram), the switching frequency, the value of C_P and C_R, and the ESR (equivalent series resistance) of C_P and C_R. A good first order approximation for R_O is:

EQUATION 4-1:

$$R_O \cong 2(R_{SW1} + R_{SW2} + ESR_{CP}) + 2(R_{SW3} + R_{SW4} + ESR_{CP}) + \frac{1}{f_{PUMP} \times C_P} + ESR_{CR}$$

$$\left(f_{PUMP} = \frac{f_{OSC}}{2},\ R_{SWX} = MOSFET\ switch\ resistance\right)$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

EQUATION 4-2:

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_P} + 4 \times ESR_{CP} + ESR_{CR}\Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See **Section 5.0 "Typical Characteristics"**, Figure 5-5 and Figure 5-6), typically 23Ω at +25°C and 5V. Careful selection of C_P and C_R will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the 1/(f_{PUMP} x C_P) component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the 1/(f_{PUMP} x C_P) term, but may have the side effect of a net increase in output impedance when C_P > 10 µF and there is not enough time to fully charge the capacitors every cycle. In a typical application when f_{OSC} = 12 kHz and C = C_P = C_R = 10 µF:

EQUATION 4-3:

$$R_O \cong 2 \times 23 + \frac{1}{(5 \times 12^3 \times 10 \times 10^{-6})} + 4 \times ESR_{CP} + ESR_{CR}$$

$$R_O \cong (46 + 20 + 5 \times ESR_C)\Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low 1/(f_{PUMP} x C_P) term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

4.2 Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 4-2. Segment A is the voltage drop across the ESR of C_R at the instant it goes from being charged by C_P (current flowing into C_R) to being discharged through the load (current flowing out of C_R). The magnitude of this current change is 2 x I_{OUT}, hence the total drop is 2 x I_{OUT} x ESR_{CR} volts. Segment B is the voltage change across C_R during time t_2, the half of the cycle when C_R supplies current to the load. The drop at B is I_{OUT} x t_2/C_R volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

EQUATION 4-4:

$$V_{RIPPLE} \cong \left(\frac{1}{2 \times f_{PUMP} \times C_R} + 2 \times ESR_{CR} \times I_{OUT} \right)$$

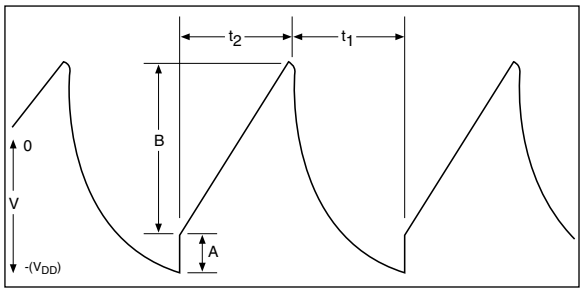


FIGURE 4-2: *Output Ripple.*

4.3 Paralleling Devices

Any number of TC7662A voltage converters may be paralleled to reduce output resistance (Figure 4-3). The reservoir capacitor, C_R, serves all devices, while each device requires its own pump capacitor, C_P. The resultant output resistance would be approximately:

EQUATION 4-5:

$$R_{OUT} = \frac{R_{OUT}(of\ \ TC7662A)}{n(number\ of\ devices)}$$

4.4 Cascading Devices

The TC7662A may be cascaded as shown (Figure 4-4) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

EQUATION 4-6:

$$V_{OUT} = -n(V_{IN})$$

Where:

n = an integer representing the number of devices cascaded

The resulting output resistance would be approximately the weighted sum of the individual TC7662A R_{OUT} values.

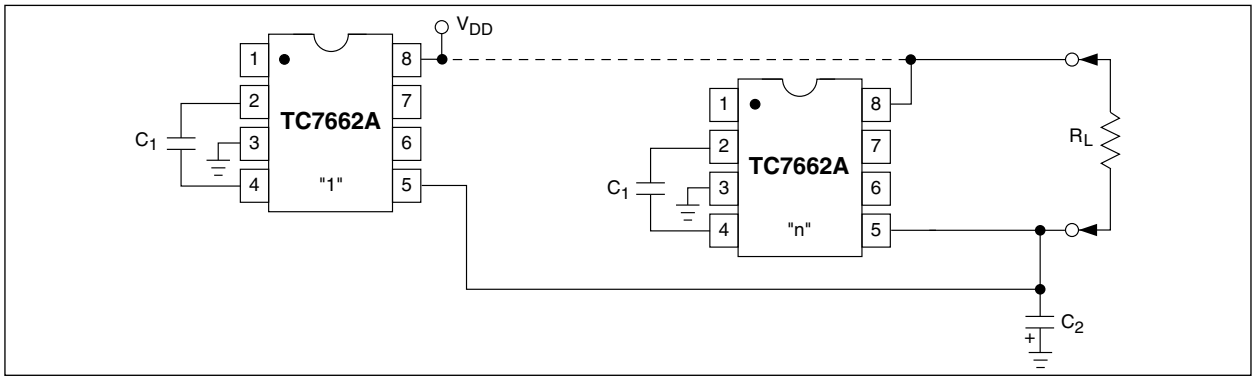


FIGURE 4-3: *Paralleling Devices Lowers Output Impedance.*

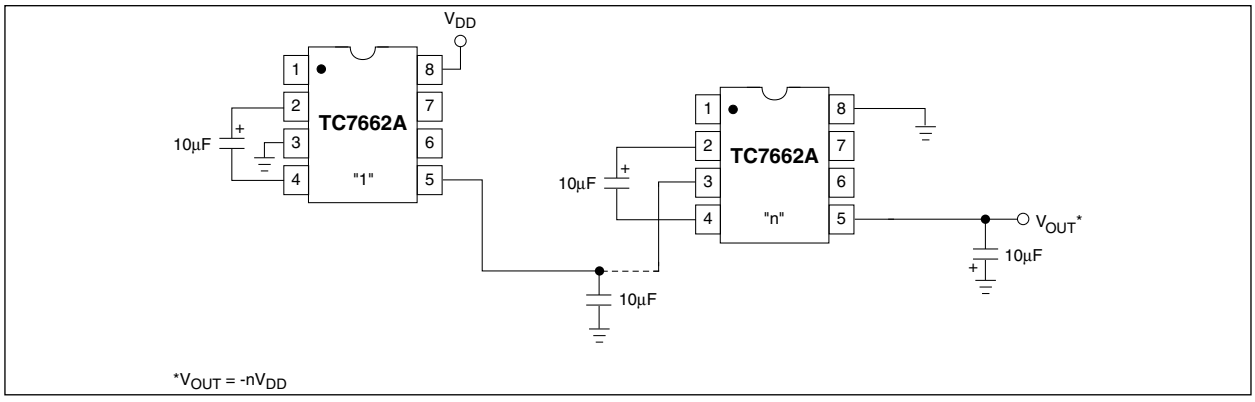


FIGURE 4-4: *Increased Output Voltage by Cascading Devices.*

4.5 Changing the TC7662A Oscillator Frequency

It is possible to increase the conversion efficiency of the TC7662A at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 4-5. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_P) and reservoir (C_R) capacitors; this is overcome by increasing the values of C_P and C_R by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and V_{DD} will lower the oscillator frequency to 2 kHz from its nominal frequency of 12 kHz (multiple of 6), and thereby necessitate a corresponding increase in the value of C_P and C_R (from 10 µF to 68 µF).

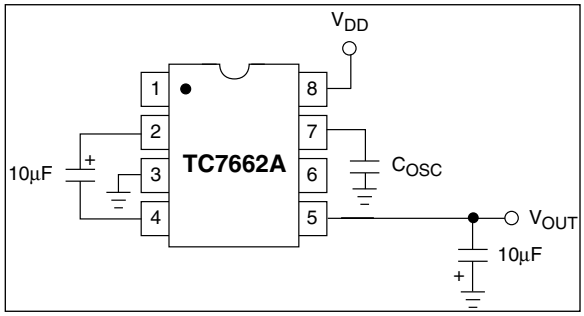


FIGURE 4-5: *Lowering Oscillator Frequency.*

4.6 Positive Voltage Doubling

The TC7662A may be employed to achieve positive voltage doubling using the circuit shown in Figure 4-6. In this application, the pump inverter switches of the TC7662A are used to charge C_P to a voltage level of $V_{DD} – V_F$ (where V_{DD} is the supply voltage and V_F is the forward voltage on C_P plus the supply voltage (V_{DD}) applied through diode D_2 to capacitor C_R). The voltage thus created on C_R becomes $(2\ V_{DD}) – (2\ V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V_{DD} = 5V and an output current of 10 mA, it will be approximately 60Ω.

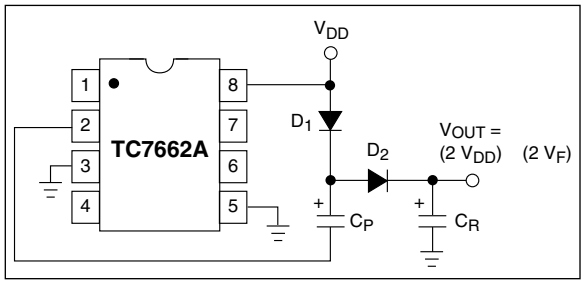


FIGURE 4-6: *Positive Voltage Multiplier.*

4.7 Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 4-7 combines the functions shown in Figure 4-1 and Figure 4-6 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

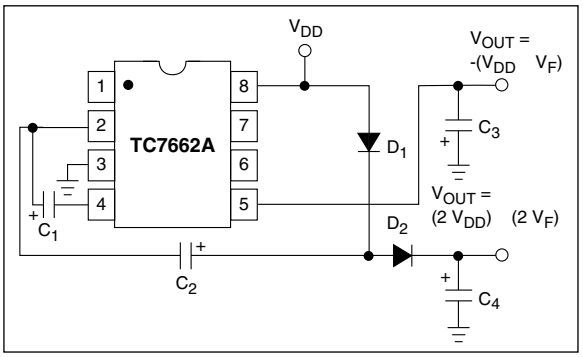


FIGURE 4-7: *Combined Negative Converter and Positive Doubler.*

4.8 Voltage Splitting

The same bidirectional characteristics can be used to split a higher supply in half, as shown in Figure 4-8. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 4-4, +15V can be converted (via +7.5V and -7.5V) to a nominal -15V, though with rather high series resistance (~250Ω).

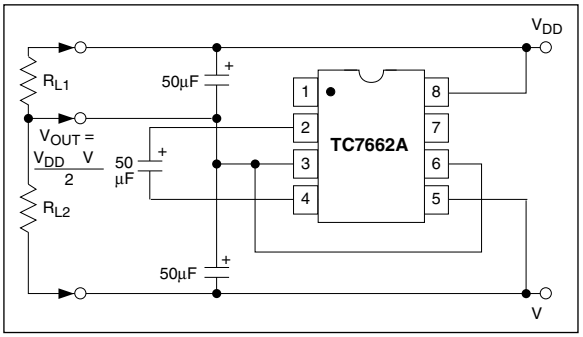


FIGURE 4-8: *Splitting a Supply in Half.*

5.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Circuit of Figure 3-1, $C_P = C_R = 10\ \mu F$, $C_{ESRCP} \approx C_{ESRCR} \approx 1\Omega$, $T_A = 25°C$ unless otherwise noted.

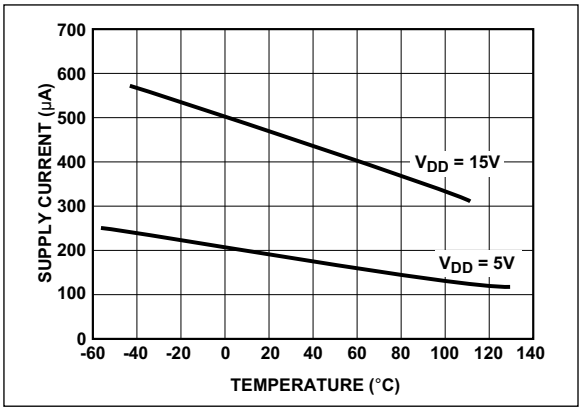


FIGURE 5-1: *Supply Current vs. Temperature.*

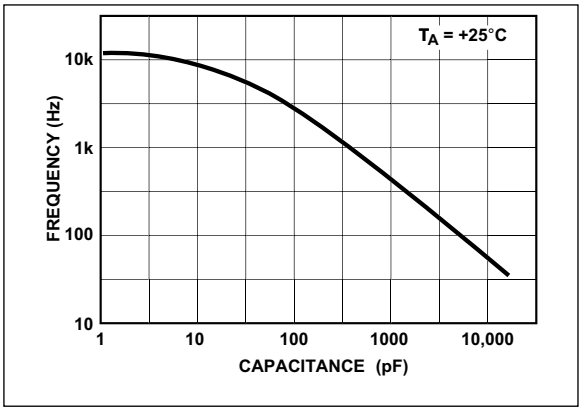


FIGURE 5-4: *Oscillator Frequency vs. C_{OSC}.*

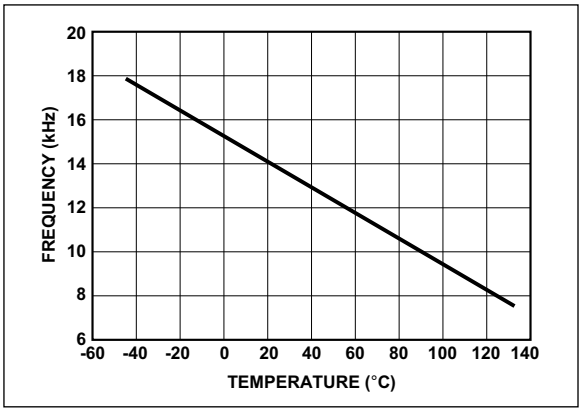


FIGURE 5-2: *Frequency vs. Temperature.*

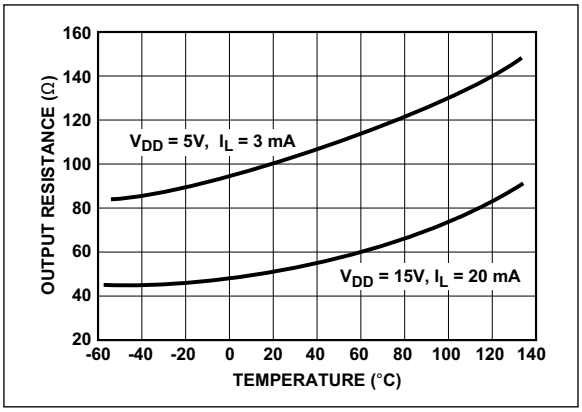


FIGURE 5-5: *Output Resistance vs. Temperature.*

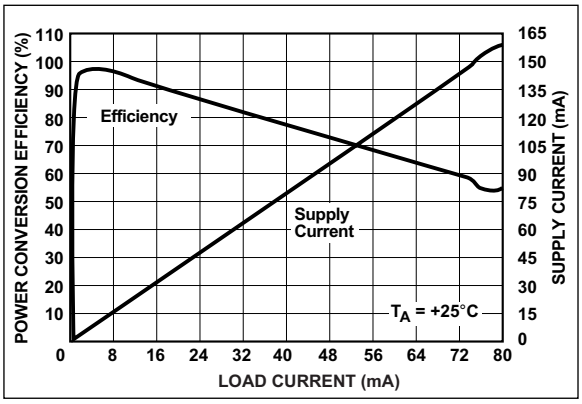


FIGURE 5-3: *Power Conversion Efficiency vs. I_{LOAD}.*

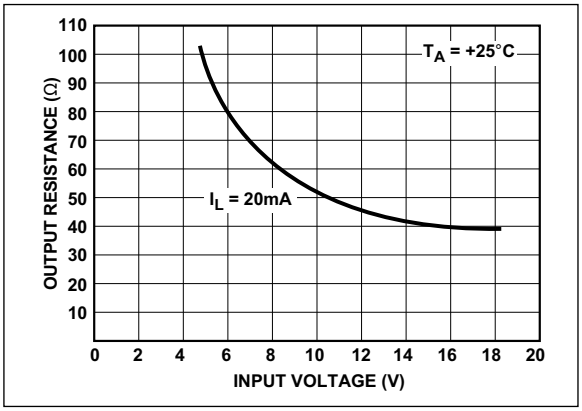
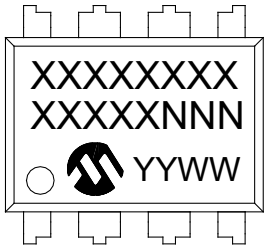


FIGURE 5-6: *Output Resistance vs. Input Voltage.*

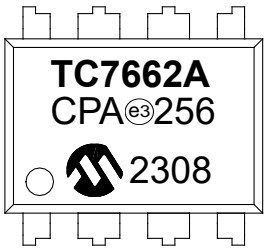
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

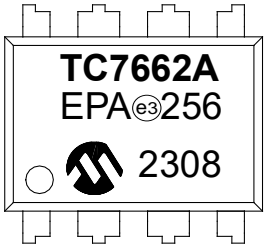
8-Lead PDIP (300 mil)



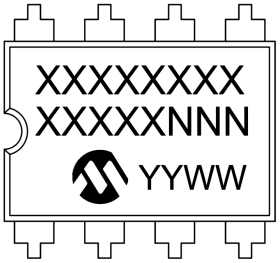
Example



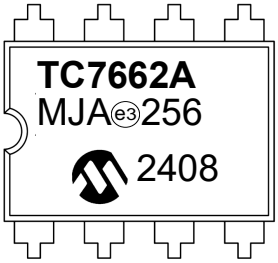
Example



8-Lead CERDIP (300 in)



Example

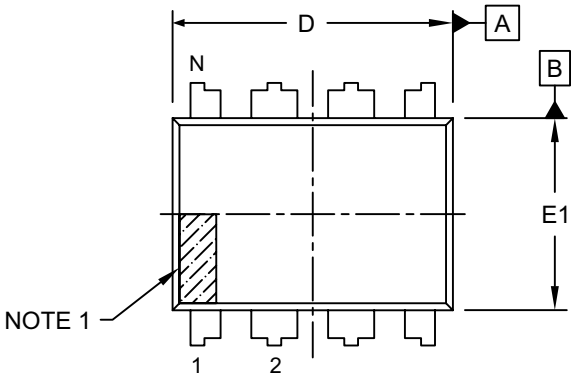


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

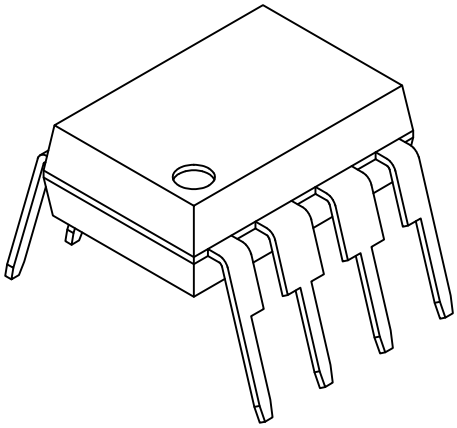
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

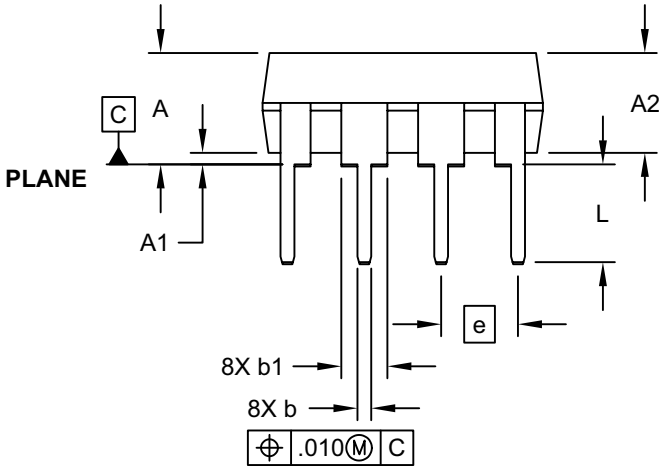
8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

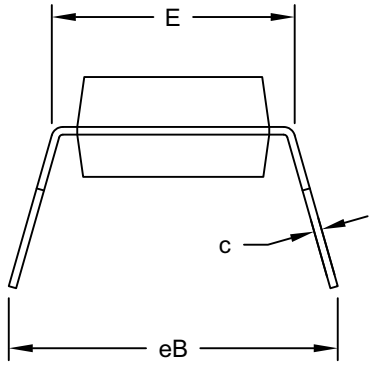


TOP VIEW





SIDE VIEW

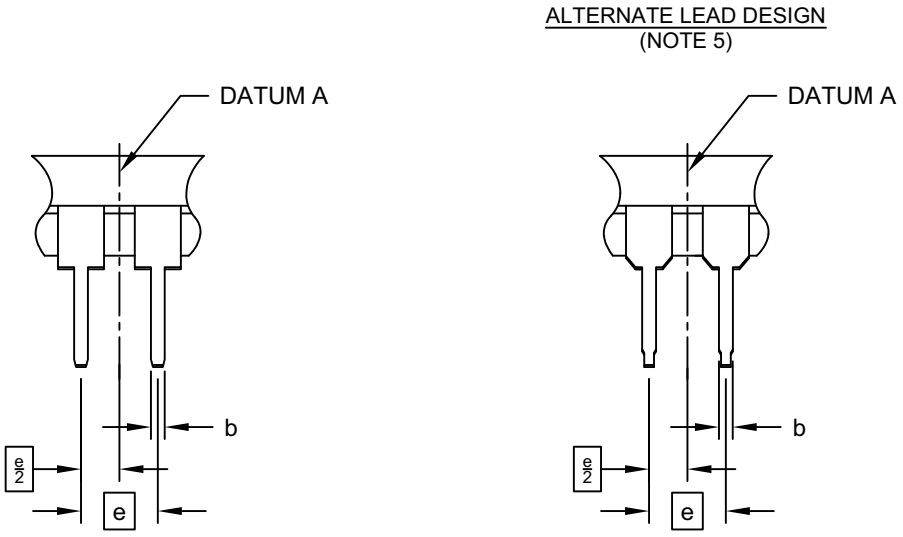


END VIEW

Microchip Technology Drawing No. C04-018-PA Rev F Sheet 1 of 2

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

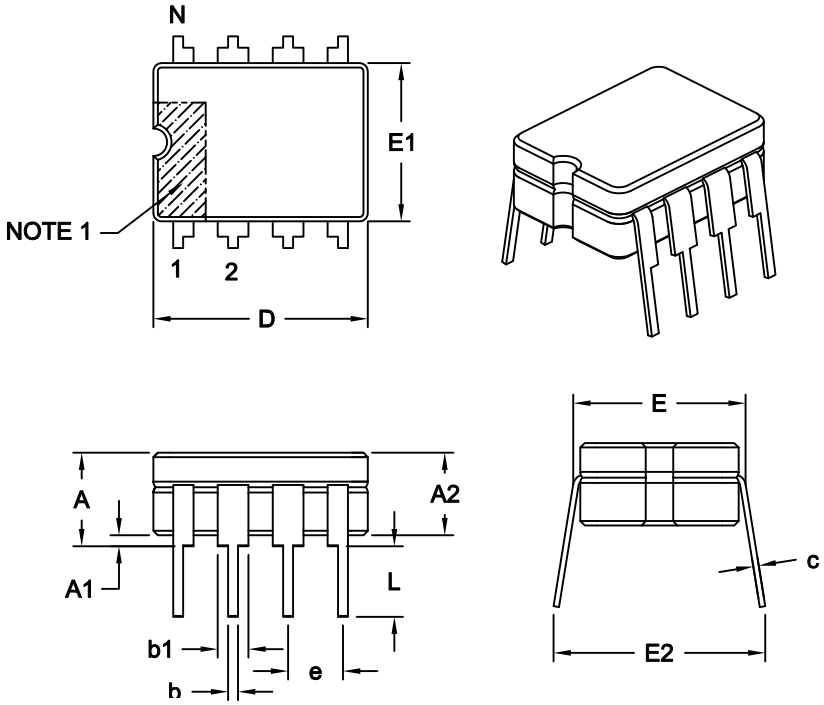
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-PA Rev F Sheet 2 of 2

8-Lead Ceramic Dual In-Line (JA) ~ .300" Body [CERDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.200
Base to Seating Plane §	A1	.015	-	-
Ceramic Package Height	A2	.140	-	.175
Shoulder to Shoulder Width	E	.290	-	.320
Ceramic Pkg. Width	E1	.230	.248	.300
Overall Length	D	.370	.380	.400
Tip to Seating Plane	L	.125	-	.200
Lead Thickness	c	.008	-	.015
Upper Lead Width	b1	.045	-	.065
Lower Lead Width	b	.015	-	.023
Overall Row Spacing	E2	.314	-	.410

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-001C

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (May 2025)

- Updated **Section 1.0, Electrical characteristics**.
- Updated **Section 6.0, Packaging Information**.
- Updated Product Identification System.
- Format changes throughout the document.

Revision B (December 2012)

- Added a note to each package outline drawing.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX
Device	Temperature Range	Package

Device:	TC7662A:	DC-to-DC Voltage Converter
Temperature Range:	C =	0°C to +70°C (Commercial)
	E =	-40°C to +85°C (Extended)
	I =	-25°C to +85°C (Commercial)
	M =	-55°C to +125°C (Extended)
Package:	PA =	8-Lead Plastic Dual In-Line - 300 mil Body (PDIP)
	JA =	8-Lead Ceramic Dual In-Line - .300 in Body (CERDIP)

Examples:

a) TC7662ACPA:	Commercial temperature, PDIP package
b) TC7662AEPA:	Extended temperature, PDIP package
c) TC7662AIJA:	Commercial temperature, CERDIP package
d) TC7662AMJA	Extended temperature, CERDIP package

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