Maxim DS1307 → MCP7940N Migration

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INTRODUCTION

This migration document describes how to replace the DS1307 RTCC with the MCP7940N RTCC.

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Note: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

The MCP7940N is an I²C™ RTCC device similar to the Maxim DS1307. The MCP7940N and DS1307 are both available in the standard 8-lead SOIC and PDIP packages.

Table 1 shows considerations that must be taken into account when migrating from DS1307 to the MCP7940N.

TABLE 1: DS1307 – MCP7940N MIGRATION REQUIRED MODIFICATIONS

No.	Required changes	HW	SW	Section Reference
1	External load capacitors required	✓	—	**Crystal Circuit**
2	MCP7940N requires additional components for the battery backup circuit	✓	—	**Battery Backup**
3	The MCP7940N battery backup function is enabled by setting the VBATEN bit	—	✓	**Battery Backup**
4	MCP7940N can work on 100 kHz and 400 kHz I²C™ frequency versus 100 kHz for DS1307	✓	✓	**Configuring The I²C Bus**
5	MCP7940N and DS1307 have different I²C™ control bytes	—	✓	**Device Addressing**
6	The MCP7940N MFP pin (SQW/OUT on DS1307) has more functions: square-wave, alarms and firmware controlled output	—	✓	**SQW/OUT Vs. MFP Functionality**
7	SQW/OUT and MFP pins have opposite power-up states	—	✓	**SQW/OUT Vs. MFP Functionality**
8	The MCP7940N oscillator is enabled by a control bit with inverse polarity	—	✓	**Starting the Oscillator**
9	Additional control and Status bits in the Date and Time registers. SRAM address range changes	—	✓	**Accessing the RTCC and SRAM Registers**

TABLE 2: MCP7940N ADDITIONAL FEATURES

No.	Feature
1	64 bytes of SRAM battery backed; DS1307 has only 56 bytes.
2	On-chip digital trimming/calibration.
3	Two programmable alarms.
4	More package options: 8-lead SOIC, TSSOP, MSOP and 2x3 TDFN.
5	100 kHz and 400 kHz I^2C™ compatible.
6	Power-Fail Time-Stamp registers.
7	1 Kbit EEPROM **(Note)** and 64 bits unique ID location.
8	Leap year indication bit.
9	MCP940N is available in E-temp.
Note:	Available only on MCP7941X.

DS1307 and MCP7940N are electrically compatible. Although there are some differences between the two devices (shown in Table 3), these do not influence the migration process.

TABLE 3: ELECTRICAL DIFFERENCES BETWEEN MCP7940 AND DS1307

No.	Description	Symbol	Differences	
			MCP7940N	DS1307
1	Supply Voltage	V_{CC}	Industrial (I): 1.8V-5.5V	4.5V-5.5V
2	V_{BAT} Battery Voltage	V_{BAT}	1.3-5.5V	2-3.5V
3	V_{BAT} Change Over	V_{TRIP} (V_{PF} on DS1307)	Typ. 1.5V	Typ. 1.25 x V_{BAT}
4	V_{BAT} Current (V_{BAT} = 3.0V)	I_{BAT}	Typ. 700 nA	Typ. 500 nA
5	High-level input Voltage	V_{IH}	Min. 0.7 x V_{CC}	Min. 2.2V
6	Low-level input Voltage	V_{IL}	Max. 0.3 x V_{CC}	Max. 0.8V
7	Standby Current	Iccs	Max. 5 µA	Max. 200 µA
8	SCL Clock Frequency	f_{SCL}	Max. 400 kHz	Max. 100 kHz
9	Active supply current	I_{CCA}	Read: Max. 300 µA (400 kHz)	Max. 1.5 mA (100 kHz)
			Write: Max. 400 µA (400 kHz)	
10	Crystal Selection	—	6-9 pF	12.5 pF

SCHEMATIC RECOMMANDATIONS

The differences between the schematics of MCP7940N and DS1307 are the load capacitors (CX1 and CX2) and the battery backup circuit.

The recommended connections for the MCP7940N and DS1307 devices are shown in Figure 1 and Figure 2.

FIGURE 1: RECOMMENDED CONNECTIONS FOR DS1307 DEVICES

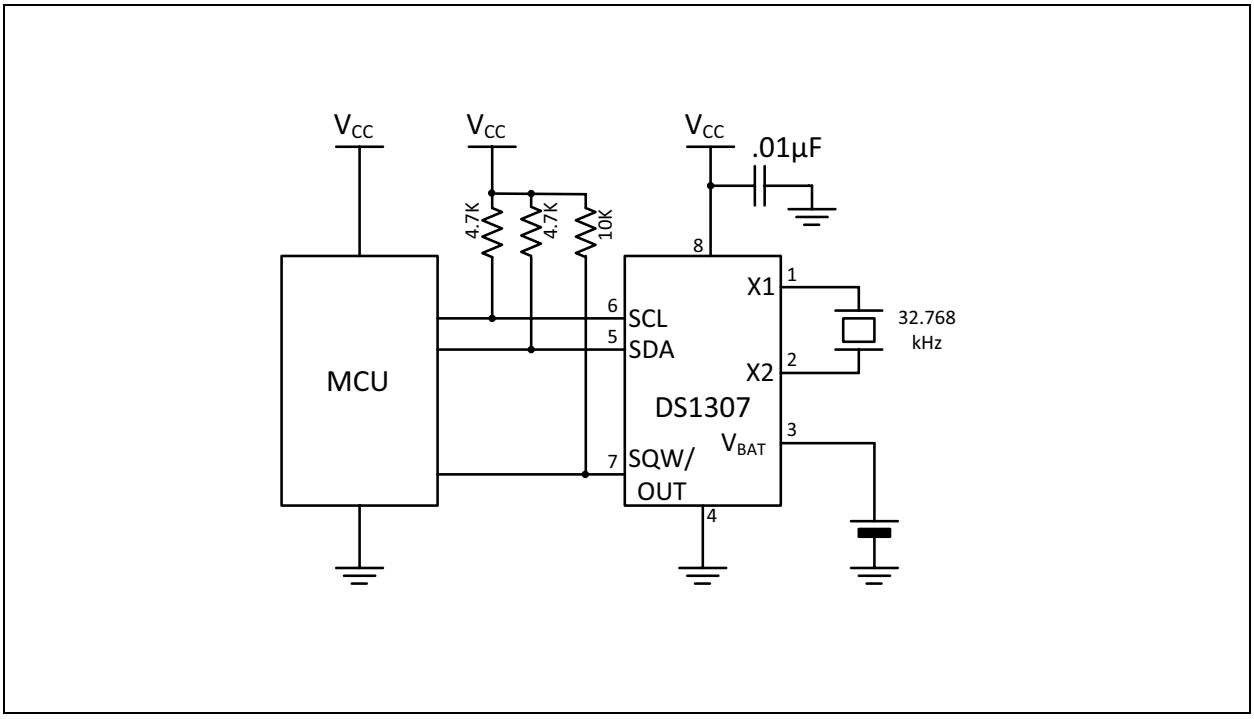
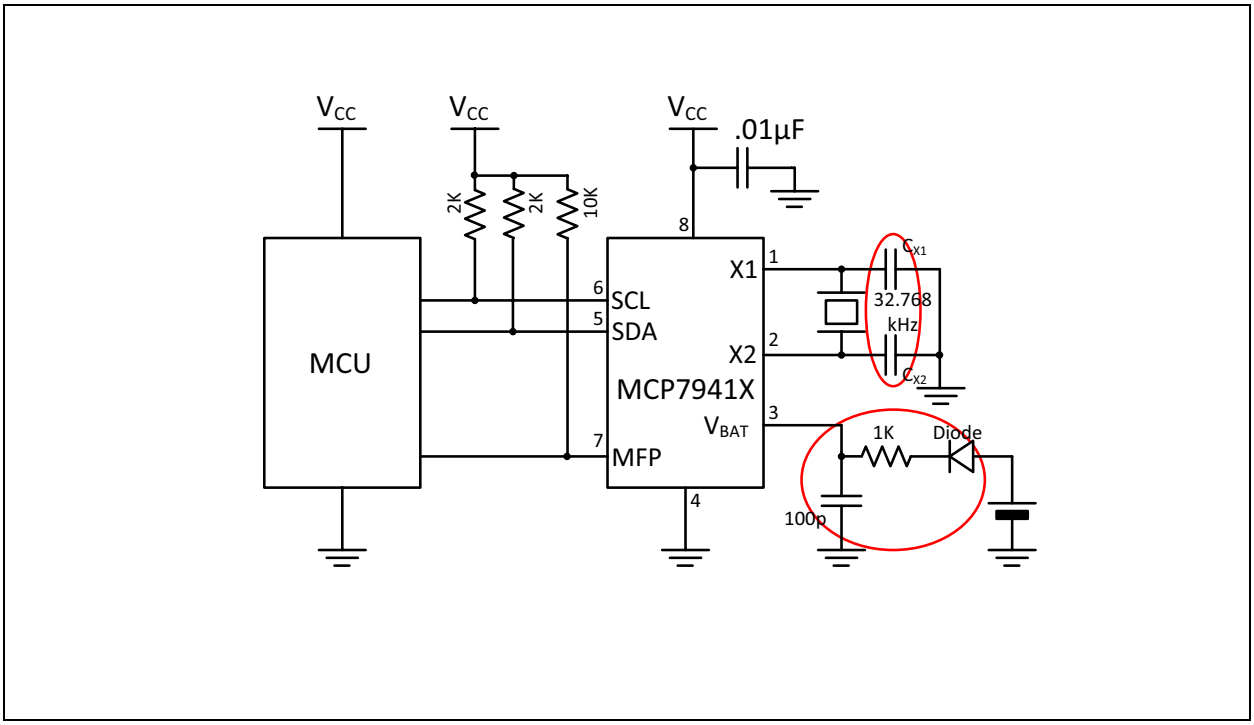


FIGURE 2: RECOMMENDED CONNECTIONS FOR MCP7940N DEVICES



CRYSTAL CIRCUIT

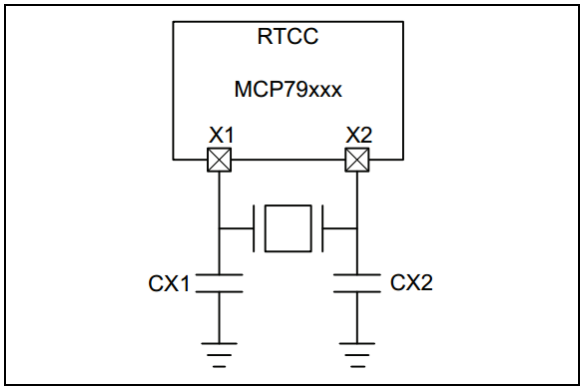
DS1307 is designed to use 32.768 kHz crystals with 12.5 pF load capacitance. The CX1 and CX2 capacitors are internal.

Figure 3 shows the MCP7940N schematic for the oscillator circuit (this device does not have internal load capacitors which must be included on the PCB). It has been designed to operate with a standard 32.768 kHz tuning fork crystal with a load capacitance of between 6-9 pF.

Microchip recommends several crystals for which MCP7940N works reliably. For more information please consult the following documents:

- AN1365, *"Recommended Usage of Microchip Serial RTCC Devices"* (DS01365)
- MCP7940N Data Sheet (DS25010)

FIGURE 3: OSCILLATOR DIAGRAM



BATTERY BACKUP

MCP7940N and DS1307 devices both have an automatic VCC switchover to VBAT, backup supply, to maintain the RTCC and SRAM during a VCC power fail.

The DS1307 battery backup feature is always enabled in hardware. On the MCP7940N, the battery backup feature is controlled by the VBATEN bit (bit 3) in the Day register (0x03). The VBATEN bit should be set to '1' to match the functionality of the DS1307.

Note: If the battery backup function is not enabled, the SRAM content will be lost and RTCC will be reset when VCC drops to VTRIP. If the device is operating in Battery Backup mode and the VBAT drops to the minimum voltage (see Table 3, VBAT parameter), the entire SRAM and RTCC data will no longer be preserved during power loss.

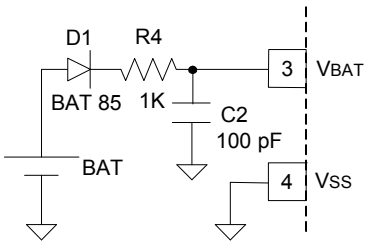
The MCP7940N and DS1307 are fully accessible through the serial interface while VCC is higher than VTRIP/VPF. These devices have different operating modes when VCC drops to VTRIP/VPF and when the backup supply voltage is higher than the supply voltage, VCC.

TABLE 4: VBAT vs. VCC

Device	Supply Condition	Serial Access	Powered By
DS1307	VCC > VPF	Yes	VCC
	VCC < VPF, VCC > VBAT	No	VCC
	VCC < VPF, VCC < VBAT	No	VBAT
	VCC > VBAT + 0.2V	No	VCC
MCP7940N	VCC > VTRIP	Yes	VCC
	VCC < VTRIP	No	VBAT

Note: The VTRIP parameter on MCP7940N is typically 1.5V. On DS1307, the VTRIP parameter is named VPF and is typically 1.25 x VBAT (VBAT = 3V).

FIGURE 4: BATTERY BACKUP



When using any supply, it is recommended to include a 1K series resistor R4 and a 100 pF capacitor C2 between the supply and the VBAT pin (as seen in Figure 4). This is required to remove the spikes that can occur when switching from VCC to VBAT.

Additionally, a series diode D1 is recommended when using a battery to eliminate any current flowing into the cell during a catastrophic failure of the RTCC device. For more information, see AN1365, *"Recommended Usage of Microchip Serial RTCC Devices"* (DS01365).

CONFIGURING THE I²C BUS

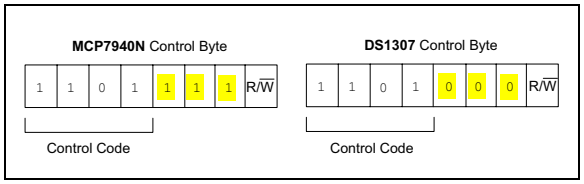
The MCP7940N is I²C 100 kHz and 400 kHz compatible (the DS1307 operates in the standard mode – 100 kHz – only). The SDA and SCL pins are open-drain terminals, therefore, they require pull-up resistors to VCC (typically 10 kΩ for 100 kHz and 2 kΩ for 400 kHz).

If the 400 kHz frequency is used, the master device must be configured to communicate at this increased speed.

DEVICE ADDRESSING

The MCP7940N and DS1307 control byte are shown in Figure 5.

FIGURE 5: ADDRESS SEQUENCE BIT ASSIGNMENTS



The MCP7940N control byte for accessing the SRAM and RTCC registers is set to '1101111x' (0xDF for a read, 0xDE for a write). The RTCC registers and the SRAM share the same address space.

The control byte for DS1307 is different, '1101000x' (0xD0 for a write, 0xD1 for a read operation).

The Read/Write operations are identical for DS1307 and MCP7940N, only the control byte is different.

SQW/OUT vs. MFP FUNCTIONALITY

The SQW/OUT pin from the DS1307 is called MFP on the MCP7940N. It has compatible functionality and is still Pin 7 of the package.

SQW/OUT and MFP pins can be used to output a square-wave signal with a programmable frequency (1 Hz, 4 kHz, 8 kHz and 32 kHz) or toggled via the control bit, OUT. Additionally, the MFP pin from MCP7940N is asserted when the alarm is triggered.

On power-up, the SQW/OUT and MFP pins have a different default state polarity.

Device	Pin No.	Pin Name	Power-Up State
DS1307	7	SQW/OUT	Low
MCP7940N	7	MFP	High

Note: SQW/OUT is enabled when DS1307 is powered from VCC or VBAT. MFP is disabled when MCP7940N is powered from the VBAT backup supply.

The MFP pin functionality is controlled by the Control register like SQW/OUT on DS1307.

TABLE 5: DS1307 AND MCP7940N CONTROL REGISTER

Device	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
DS1307	07h	OUT	0	0	SQWE	0	0	RS1	RS0	01h
MCP7940N	07h	OUT	SQWE	ALM1	ALM0	EXTOSC	RS2	RS1	RS0	80h

Note: Set the ALM1, ALM0, RS2 and EXTOSC to '0', to match with the DS1307 functionality.

The Control register is mapped at the same address, 07h, for MCP7940N and DS1307. Below is a description of each bit from the Control register:

- Bit 7 is the OUT bit: sets the logic level on the MFP when not using this as a square-wave output (MFP = 1 if OUT = 1 and MFP = 0 if OUT = 0)
- Bit 6 is the SQWE bit (bit 4 on DS1307): setting this bit enables the divided output from the crystal oscillator
- Bit 5:4 are ALM1:ALM0 bits: determine which alarms are active
- Bit 3 is the EXTOSC bit: setting this bit will allow an external 32.768 kHz signal to drive the RTCC registers, eliminating the need for an external crystal
- Bit 2:0 are RS2:RS0 bits: sets the internal divider for the 32.768 kHz oscillator to be driven to the MFP (1 Hz, 4 kHz, 8 kHz and 32 kHz for RS2 = 0, 64 Hz for RS2 = 1)

When migrating from DS1307 to MCP7940N, the Control register can be set, as shown in Example 1.

EXAMPLE 1:

```
DS1307_Control_Register = DS1307_SQWE | SQW_OUT_1Hz; // Control Register = 0x10
                                                    // (DS1307_SQWE = 0x10), (SQW_OUT_1Hz = 0x00)
MCP7940N_Control register = MCP7940N_SQWE | MFP_1Hz; // Control Register = 0x40
                                                    // (MCP7940N_SQWE = 0x40, MFP_1Hz = 0x00)

// SQWE bit = 1: enable square-wave function on MFP pin
// RS2:RS0 bits = 0: the frequency for the square-wave signal is 1 Hz
```

For more information, please refer to the MCP7940N Data Sheet (DS25010).

STARTING THE OSCILLATOR

The oscillator in both the RTCC's are enabled by a control bit, but the polarity varies between the devices. The enable is bit 7 in the Seconds register (0x00).

Device	Bit Name	State	Reset State
DS1307	CH	1 = disable oscillator 0 = enable oscillator	1
MCP7940N	ST	1 = enable oscillator 0 = disable oscillator	0

ACCESSING THE RTCC AND SRAM REGISTERS

The Date and Time registers are mapped on MCP7940N the same as DS1307 (from 00h to 07h address) with several differences that will be described below.

The SECONDS, MINUTES, HOUR, DATE and YEAR registers are mapped identically on the MCP7940N and DS1307.

The DAY register on MCP7940N contains the BCD day and additional bits for configuration and status (not present in the DS1307). The VBATEN bit (bit 3) is used to enable/disable the battery backup. The VBAT bit (bit 4) is set by hardware when the VCC falls and is cleared by firmware. The OSCON bit (bit 5) is set and cleared by hardware, indicating if the oscillator is currently running or not. This is a read-only bit.

The MONTH register has an additional bit, LP (bit 5), which indicates if the current year is a leap one. This is a read-only bit.

Care should be taken when the Date and Time registers are read or written. A number of the unimplemented "don't care" bits on DS1307, which read as '0', are used on MCP7940N as control and status bits (they are highlighted in Table 6).

EXAMPLE 2: READ THE DAY FROM MCP7940N

DAY_REGISTER & 0x07 = Day // Mask off control and status bits

EXAMPLE 3: READ THE MONTH FROM MCP7940N

(MONTH_REGISTER & 0x10) * 10 +
(MONTH_REGISTER & 0x0F) = Month

TABLE 6: DATE AND TIME REGISTER MAP

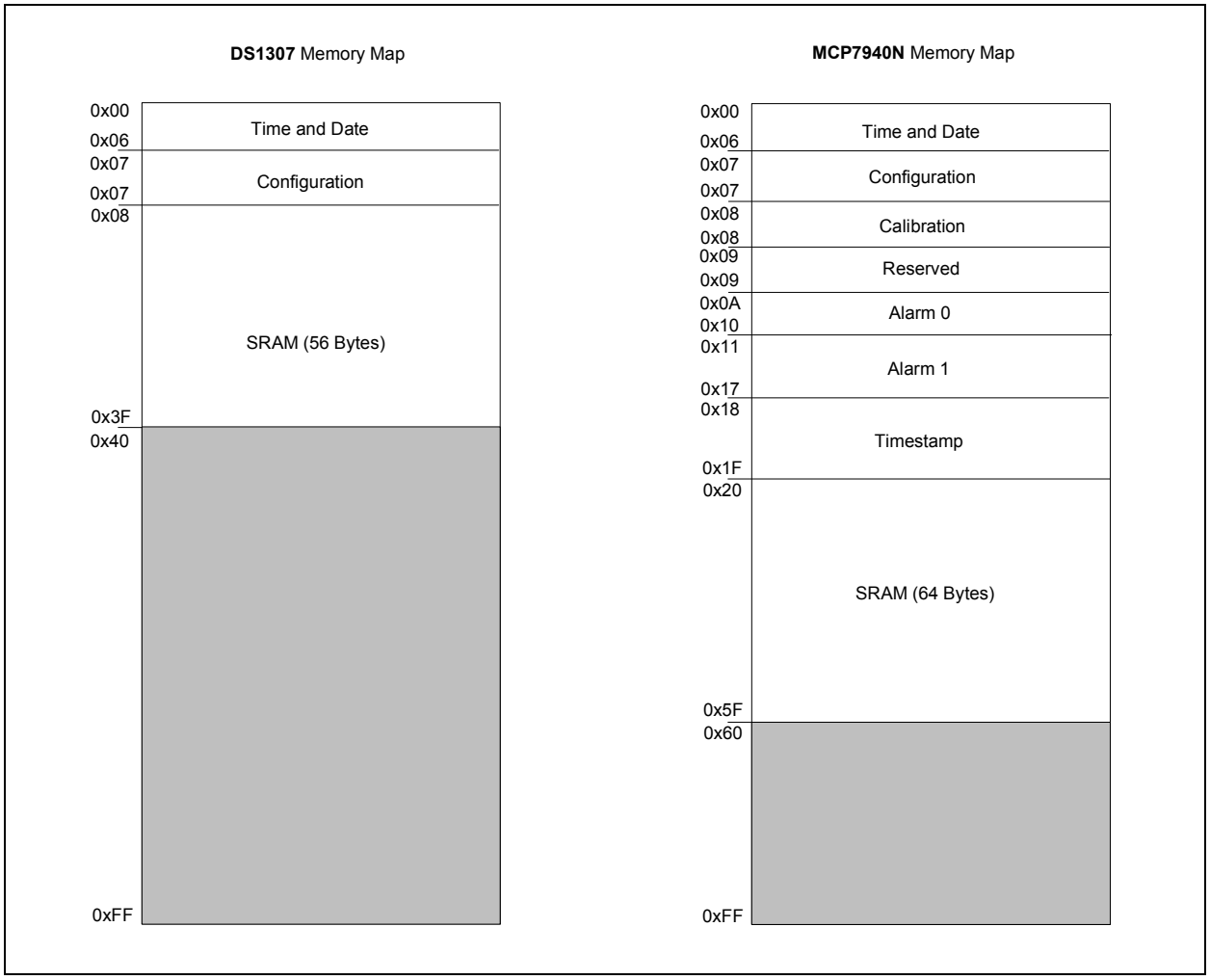
Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range	Reset State
Time Registers											
00h	ST	10 Seconds			Seconds				Seconds	00-59	00h
01h		10 Minutes			Minutes				Minutes	00-59	00h
02h		12/24	10 Hour AM/PM	10 Hour	Hour				Hours	1-12 + AM/PM 00-23	00h
03h			OSCON(Note)	VBAT(Note)	VBATEN	Day			Day	1-7	01h
04h			10 Date		Date				Date	01-31	01h
05h			LP(Note)	10 Month	Month				Month	01-12	01h
06h	10 Year				Year				Year	00-99	01h

Note: The OSCON, VBAT and LP bits are read-only.

Note: The shaded areas are not implemented and read as '0'.

Differences between the DS1307 and MCP7940N memory maps are shown in Figure 6.

FIGURE 6: DS1307 AND MCP7940N MEMORY MAP



On DS1307, the 56 bytes of RAM are located in address locations from 08h to 3Fh. These memory locations are used on MCP7940N by the calibration alarms and time-stamp registers.

On MCP7940N, the 64 bytes of RAM are located in address locations 20h to 5Fh.

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