MCP3021

Low-Power 10-Bit Analog-to-Digital Converter with I²C Interface

Features

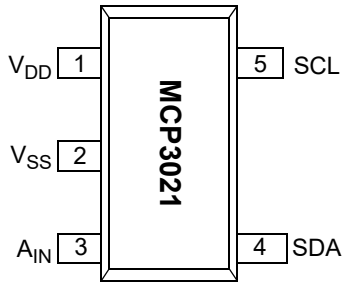
- 10-bit Resolution
- ±1 LSB Differential Nonlinearity (DNL) Maximum
- ±1 LSB Integral Nonlinearity (INL) Maximum
- 250 µA Max Conversion Current
- 5 nA Typical Standby Current, 1 µA maximum
- I²C Compatible Serial Interface
  - 100 kHz I²C Standard mode
  - 400 kHz I²C Fast mode
- Up to Eight Devices Connected on a Single 2-Wire Bus
- 22.3 ksps in I²C Fast mode
- Single-Ended Analog Input Channel
- On-Chip Sample and Hold
- On-Chip Conversion Clock
- Single-Supply Specified Operation: 2.7V to 5.5V
- AEC-Q100 Qualified, Grade 1
- Extended Temperature Range: -40°C to +125°C
- Package: 5-Lead SOT-23

Applications

- Automotive
- Data Logging
- Multi-Zone Monitoring
- Handheld Portable Applications
- Battery-Powered Test Equipment
- Remote or Isolated Data Acquisition

Package Types (top view)

5-Lead SOT-23



General Description

MCP3021 is a successive approximation Analog-to-Digital Converter (ADC) with 10 bits of resolution. It provides one single-ended input with very low power consumption. Using advanced CMOS technology, MCP3021 provides a low maximum conversion current of 250 µA and a standby current of 1 µA.

The low current consumption and compact SOT-23 package make this device ideal for battery-powered and remote data acquisition applications.

MCP3021 communicates over a 2-wire I²C compatible interface. Standard (100 kHz) and Fast (400 kHz) I²C modes are available. An on-chip conversion clock enables independent timing for the I²C and conversion clocks. Up to eight MCP3021 devices can interconnect on a single 2-wire bus.

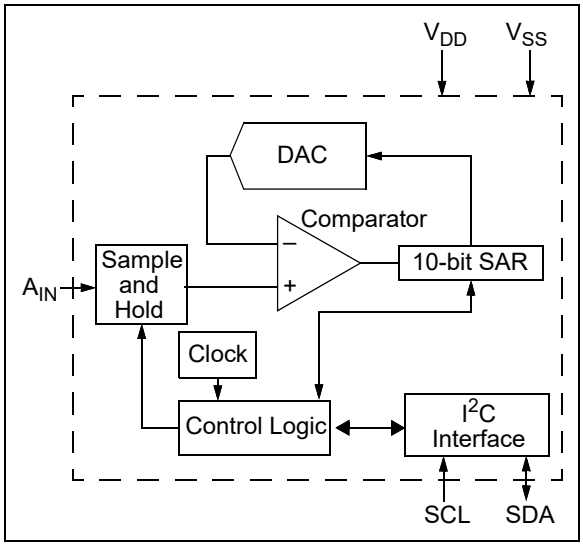
MCP3021 runs on a single-supply voltage operating over a broad range of 2.7V to 5.5V. The device offers excellent linearity: ±1 LSB DNL and INL, maximum.

MCP3021 is AEC-Q100 qualified for automotive applications and operates over the extended temperature range of -40°C to +125°C.

Related Devices

- MCP3221 – Low-Power 12-Bit Analog-to-Digital Converter with I²C Interface

Functional Block Diagram



1.0 ELECTRICAL SPECIFICATIONS

1.1 Absolute Maximum Ratings(†)

V_{DD} . . . . . +7.0V
Analog input pin (A_{IN}) relative to V_{SS} . . . . . -0.6V to V_{DD} +0.6V
SDA and SCL pins relative to V_{SS} . . . . . -0.6V to V_{DD} +1.0V
Storage Temperature (T_{STG}) . . . . . -65°C to +150°C
Ambient Temperature (T_A) with power applied. . . . . -65°C to +125°C
Maximum Junction Temperature (T_J) . . . . . +150°C
ESD protection on all pins (HBM). . . . . ≥ 4 kV

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Electrical Characteristics

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Operating Conditions: Unless otherwise indicated, all parameters apply at V_{DD} = 5.0V, V_{SS} = GND, R_{PU} = 2 kΩ (**Note 1**), T_A = -40°C to +125°C, I^2C Fast Mode Timing: f_{SCL} = 400 kHz.

Parameter	Symbol	Min.	Typical	Max.	Units	Conditions
DC Accuracy						
Resolution	—		10		bits	
Integral Nonlinearity	INL	—	±0.25	±1	LSB	
Differential Nonlinearity	DNL	—	±0.25	±1	LSB	No missing codes
Offset Error	—	—	±0.75	±3	LSB	
Gain Error	—	—	-1	±3	LSB	
Dynamic Performance						
Total Harmonic Distortion	THD	—	-70	—	dB	V_{IN} = 0.1V to 4.9V at f = 1 kHz
Signal-to-Noise and Distortion	SINAD	—	60	—	dB	V_{IN} = 0.1V to 4.9V at f = 1 kHz
Spurious Free Dynamic Range	SFDR	—	74	—	dB	V_{IN} = 0.1V to 4.9V at f = 1 kHz
Analog Input						
Input Voltage Range	—	V_{SS} – 0.3	—	V_{DD} + 0.3	V	2.7V ≤ V_{DD} ≤ 5.5V
Leakage Current	—	-1	—	+1	µA	
Power Requirements						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Conversion Current	I_{DD}	—	175	250	µA	
Standby Current	I_{DDS}	—	0.005	1	µA	-40°C ≤ T_A ≤ +85°C SDA/SCL = V_{DD}, **Note 3**
		—	0.9	—	µA	+85°C ≤ T_A ≤ +125°C SDA/SCL = V_{DD}, **Note 3**
Active Bus Current	I_{DDA}	—	—	120	µA	SDA/SCL = V_{SS} to V_{DD} at f_{SCL} = 400 kHz

Note 1: Pull-up resistor on SDA and SCL lines.
2: This parameter is periodically sampled and not 100% tested.
3: Refer to Figure 2-36 and Figure 2-37 for more details.
4: t_{ACQ} and t_{CONV} are dependent on internal oscillator timing. See Figure 5-5 and Figure 5-6 in regards to SCL.
5: Sample time is the period between conversions after the address byte is sent to the converter. Refer to Figure 5-6.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Operating Conditions: Unless otherwise indicated, all parameters apply at V_{DD} = 5.0V, V_{SS} = GND, R_{PU} = 2 kΩ (**Note 1**), T_A = -40°C to +125°C, I^2C Fast Mode Timing: f_{SCL} = 400 kHz.						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
SDA/SCL (open-drain output)						
Data Coding Format	—	Straight Binary			—	
High-Level Input Voltage	V_{IH}	0.7 x V_{DD}	—	—	V	
Low-Level Input Voltage	V_{IL}	—	—	0.3 x V_{DD}	V	
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA, R_{PU} = 1.53 kΩ
Hysteresis of Schmitt Trigger Inputs	V_{HYST}	—	0.05 x V_{DD}	—	V	f_{SCL} = 400 kHz only
Input Leakage Current	I_{LI}	-1	—	+1	µA	V_{IN} = V_{SS} to V_{DD}
Output Leakage Current	I_{LO}	-1	—	+1	µA	V_{OUT} = V_{SS} to V_{DD}
Pin Capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	—	10	pF	T_A = +25°C, f = 1 MHz, **Note 2**
Bus Capacitance	C_B	—	—	400	pF	SDA drive low, 0.4V
Conversion Rate						
Conversion Time	t_{CONV}	—	8.96	—	µs	**Note 4**
Analog Input Acquisition Time	t_{ACQ}	—	1.12	—	µs	**Note 4**
Sample Rate	f_{SAMP}	—	—	22.3	ksps	f_{SCL} = 400kHz, **Note 5**

Note 1: Pull-up resistor on SDA and SCL lines.
2: This parameter is periodically sampled and not 100% tested.
3: Refer to Figure 2-36 and Figure 2-37 for more details.
4: t_{ACQ} and t_{CONV} are dependent on internal oscillator timing. See Figure 5-5 and Figure 5-6 in regards to SCL.
5: Sample time is the period between conversions after the address byte is sent to the converter. Refer to Figure 5-6.

TABLE 1-2: TEMPERATURE SPECIFICATIONS

Operating Conditions: Unless otherwise indicated, all parameters apply at V_{DD} = 5.0V, V_{SS} = GND.						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_{OP}	-40	—	+125	°C	
Storage Temperature Range	T_{STG}	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance,	θ_{JA}	—	256	—	°C/W	

TABLE 1-3: TIMING SPECIFICATIONS

Operating Conditions: Unless otherwise indicated, all parameters apply at V_{DD} = 2.7V to 5.5V, V_{SS} = GND, T_A = -40°C to +125°C.						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
I²C Standard Mode						
Clock Frequency	f_{SCL}	0	—	100	kHz	
Clock High Time	t_{HIGH}	4000	—	—	ns	
Clock Low Time	t_{LOW}	4700	—	—	ns	
SDA and SCL Rise Time	t_R	—	—	1000	ns	From V_{IL} to V_{IH}, **Note 1**
SDA and SCL Fall Time	t_F	—	—	300	ns	From V_{IL} to V_{IH}, **Note 1**
START Condition Hold Time	$t_{HD:STA}$	4000	—	—	ns	
START Condition Setup Time	$t_{SU:STA}$	4700	—	—	ns	
Data Input Setup Time	$t_{SU:DAT}$	250	—	—	ns	
STOP Condition Setup Time	$t_{SU:STO}$	4000	—	—	ns	
STOP Condition Hold time	$t_{HD:STD}$	4000	—	—	ns	
Output Valid from Clock	t_{AA}	—	—	3500	ns	
Bus Free Time	t_{BUF}	4700	—	—	ns	**Note 2**
Input Filter Spike Suppression	t_{SP}	—	—	50	ns	SDA and SCL pins, **Note 1**
I²C Fast Mode						
Clock Frequency	f_{SCL}	0	—	400	kHz	
Clock High Time	t_{HIGH}	600	—	—	ns	
Clock Low Time	t_{LOW}	1300	—	—	ns	
SDA and SCL Rise Time	t_R	20 + 0.1 x C_B	—	300	ns	From V_{IL} to V_{IH}, **Note 1**
SDA and SCL Fall Time	t_F	20 + 0.1 x C_B	—	300	ns	From V_{IL} to V_{IH}, **Note 1**
START Condition Hold Time	$t_{HD:STA}$	600	—	—	ns	
START Condition Setup Time	$t_{SU:STA}$	600	—	—	ns	
Data Input Hold Time	$t_{HD:DAT}$	0	—	0.9	ms	
Data Input Setup Time	$t_{SU:DAT}$	100	—	—	ns	
STOP Condition Setup Time	$t_{SU:STO}$	600	—	—	ns	
STOP Condition Hold Time	$t_{HD:STD}$	600	—	—	ns	
Output Valid from Clock	t_{AA}	—	—	900	ns	
Bus Free Time	t_{BUF}	1300	—	—	ns	**Note 2**
Input Filter Spike Suppression	t_{SP}	—	—	50	ns	SDA and SCL pins, **Note 1**

Note 1: This parameter is periodically sampled and not 100% tested.

2: Time period during which the bus must be free before a new I²C transmission can start.

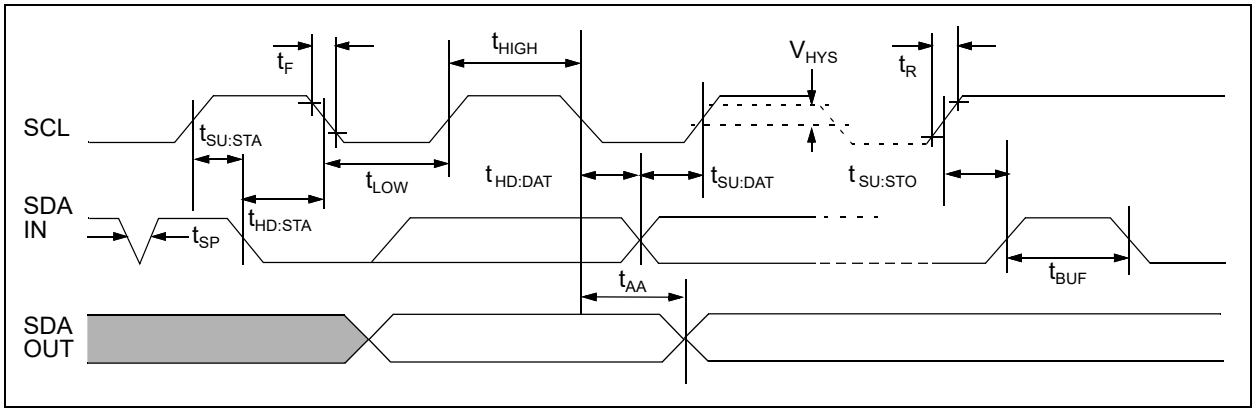


FIGURE 1-1: *I²C Standard and Fast Mode Bus Timing Data.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (for example, outside specified power supply range) and therefore outside the warranted range.

2.1 Performance Graphs

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (f_{SCL} = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

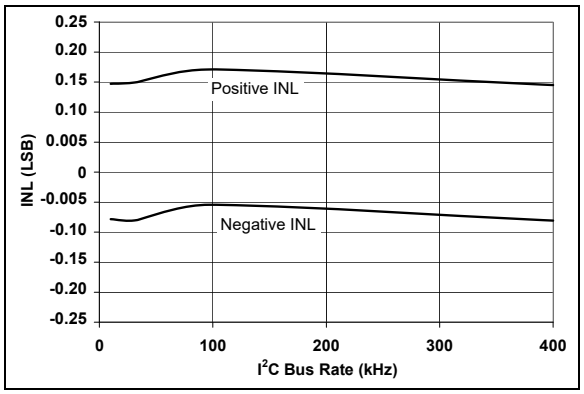


FIGURE 2-1: *INL vs. Clock Rate.*

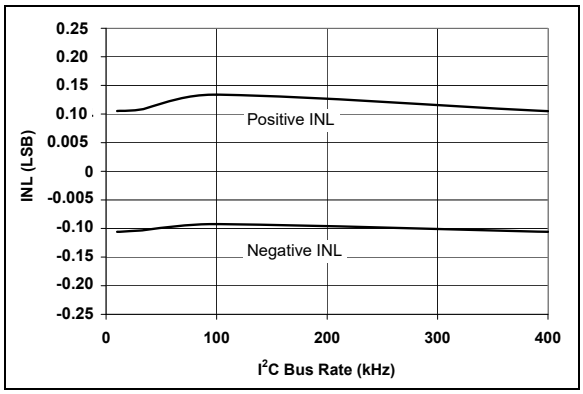


FIGURE 2-4: *INL vs. Clock Rate, V_{DD} = 2.7V.*

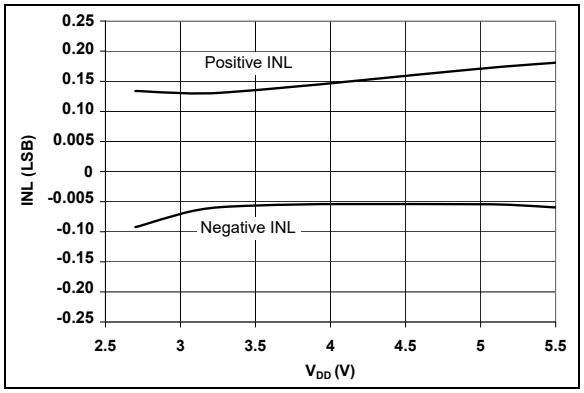


FIGURE 2-2: *INL vs. V_{DD}. I^2C Standard Mode (f_{SCL} = 100 kHz).*

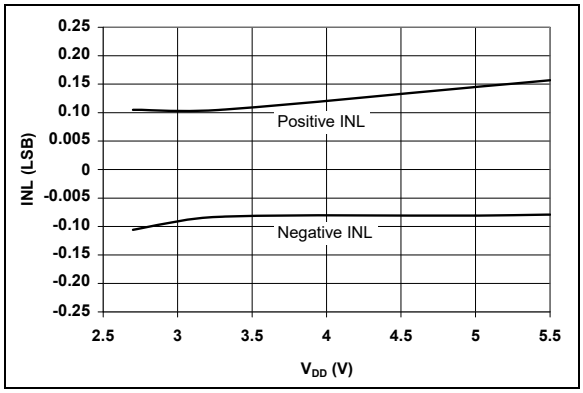


FIGURE 2-5: *INL vs. V_{DD}. I^2C Fast Mode (f_{SCL} = 400 kHz).*

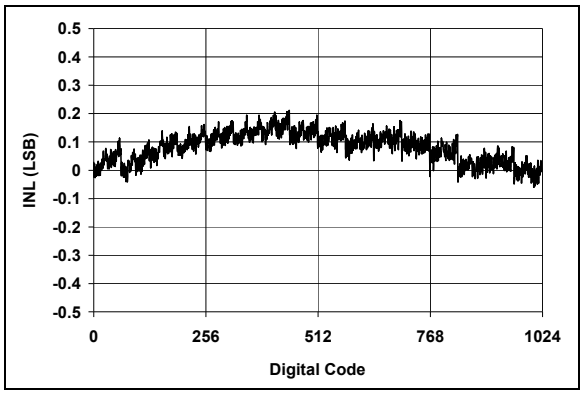


FIGURE 2-3: *INL vs. Code. Representative Part.*

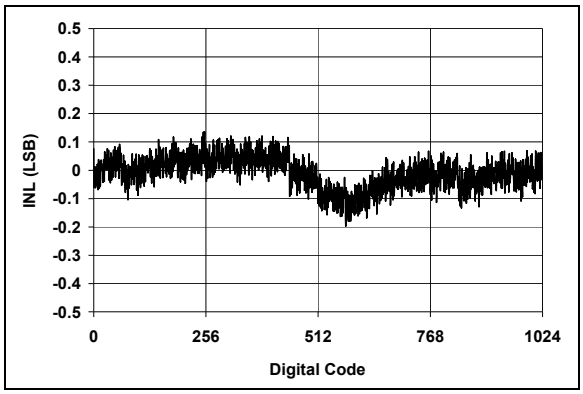


FIGURE 2-6: *INL vs. Code. Representative Part, V_{DD} = 2.7V.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (f_{SCL} = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

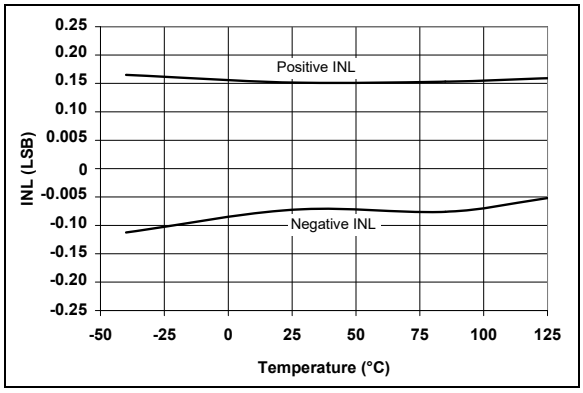


FIGURE 2-7: *INL vs. Temperature.*

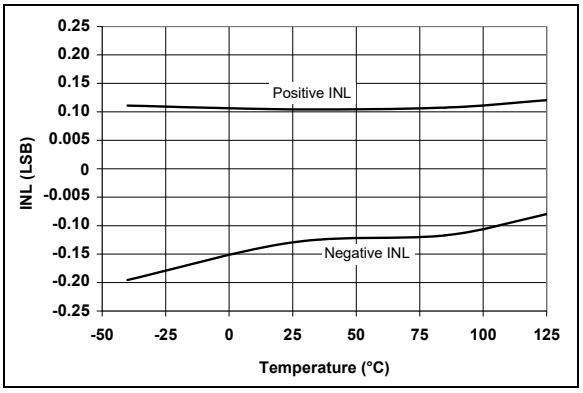


FIGURE 2-10: *INL vs. Temperature, V_{DD} = 2.7V.*

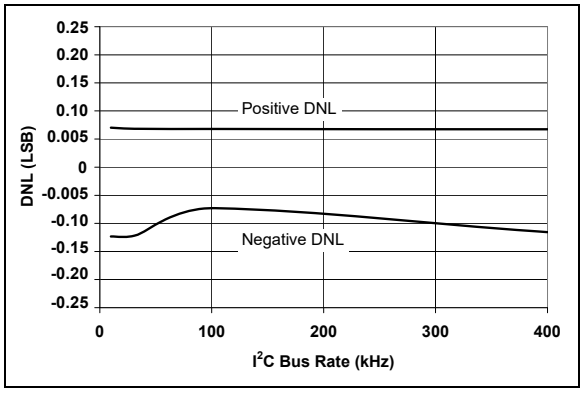


FIGURE 2-8: *DNL vs. Clock Rate.*

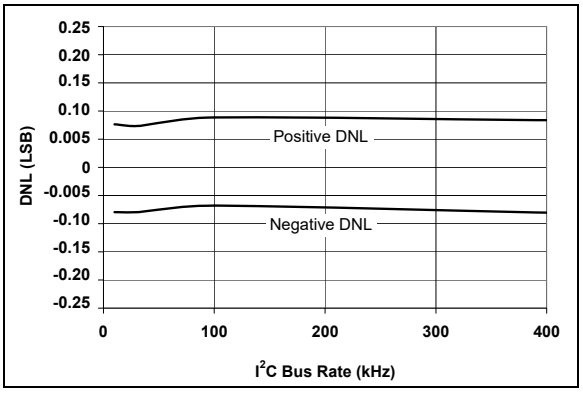


FIGURE 2-11: *DNL vs. Clock Rate, V_{DD} = 2.7V.*

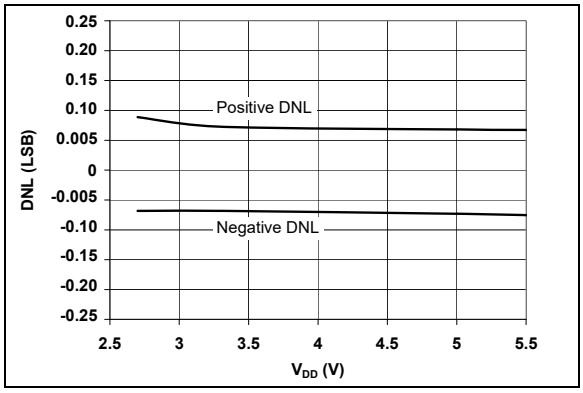


FIGURE 2-9: *DNL vs. V_{DD}. I^2C Standard Mode (f_{SCL} = 100 kHz).*

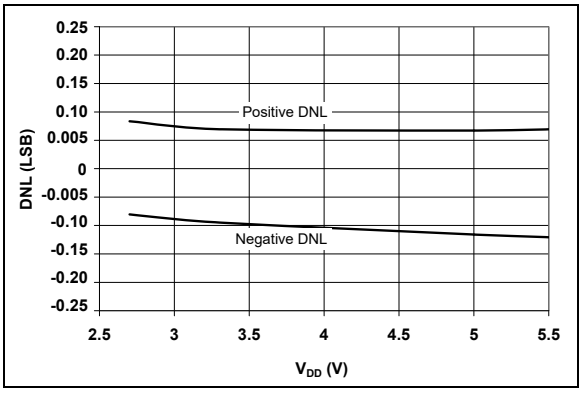


FIGURE 2-12: *DNL vs. V_{DD}. I^2C Fast Mode (f_{SCL} = 400 kHz).*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (f_{SCL} = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

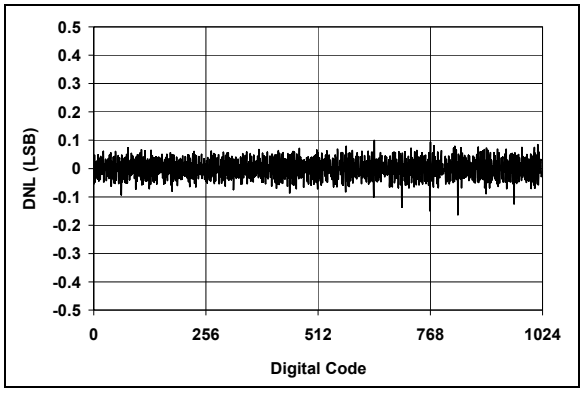


FIGURE 2-13: *DNL vs. Code. Representative Part.*

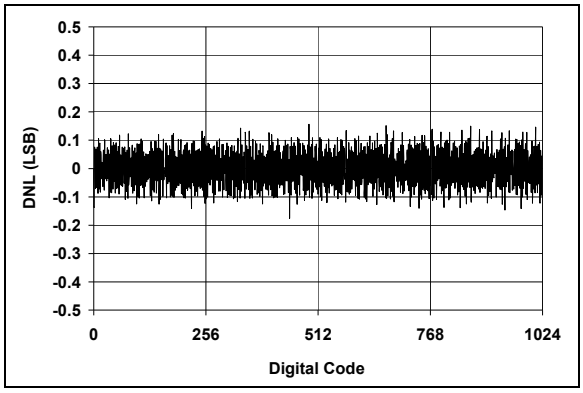


FIGURE 2-16: *DNL vs. Code. Representative Part, V_{DD} = 2.7V.*

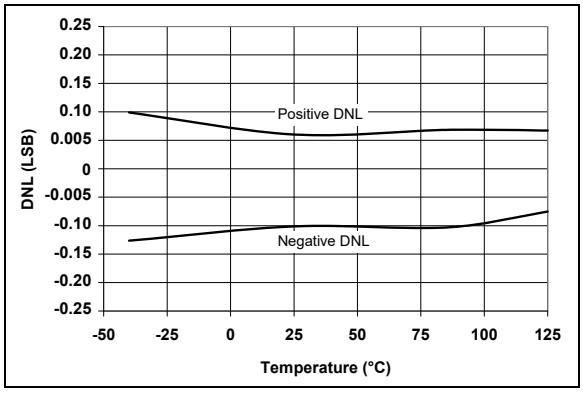


FIGURE 2-14: *DNL vs. Temperature.*

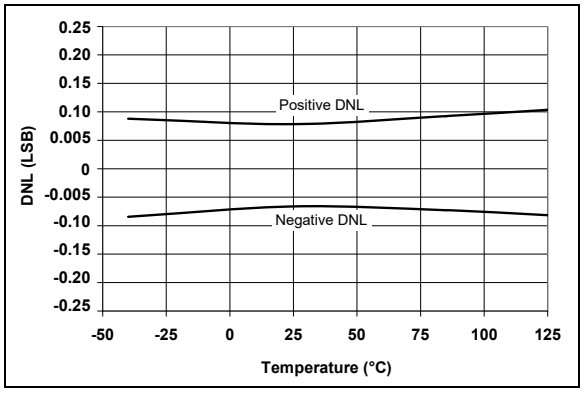


FIGURE 2-17: *DNL vs. Temperature, V_{DD} = 2.7V.*

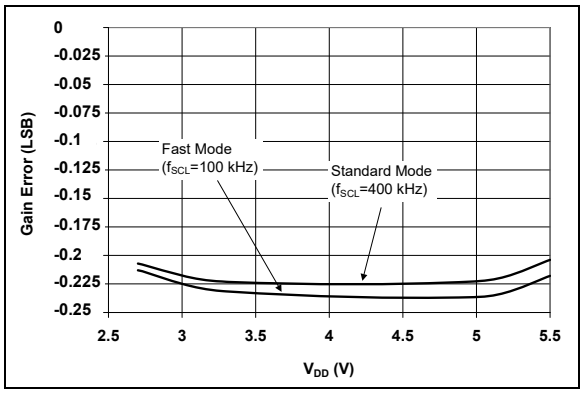


FIGURE 2-15: *Gain Error vs. V_{DD}.*

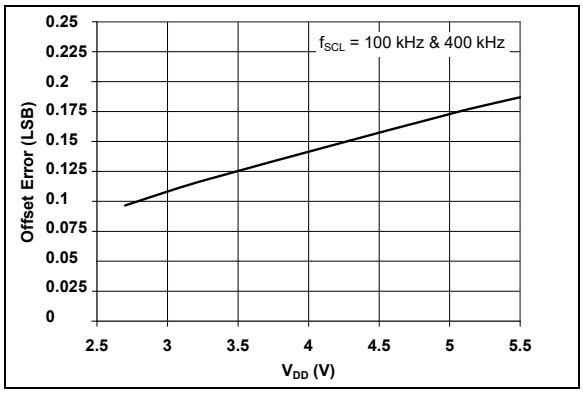


FIGURE 2-18: *Offset Error vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (f_{SCL} = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

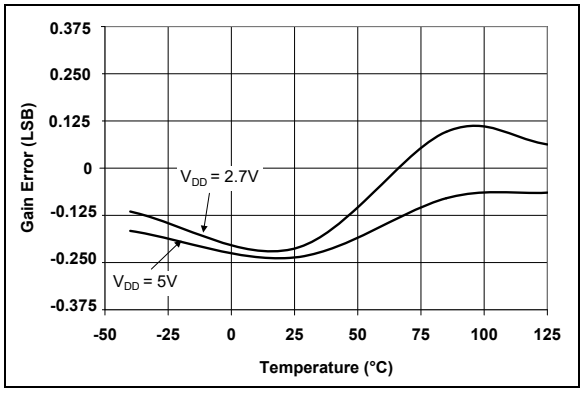


FIGURE 2-19: *Gain Error vs. Temperature.*

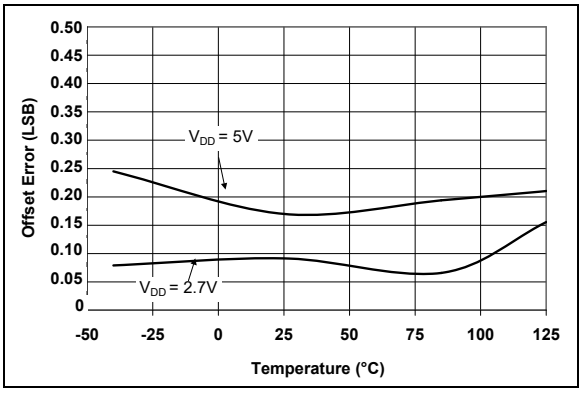


FIGURE 2-22: *Offset Error vs. Temperature.*

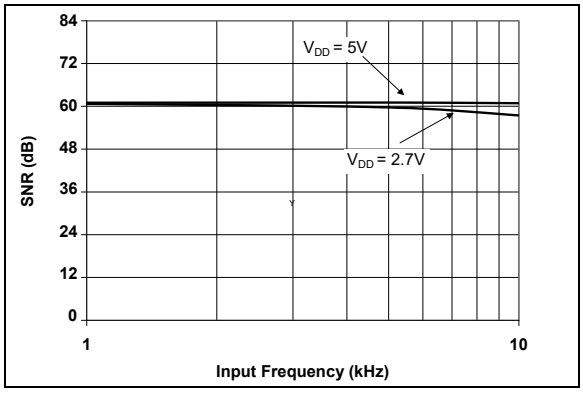


FIGURE 2-20: *SNR vs. Input Frequency.*

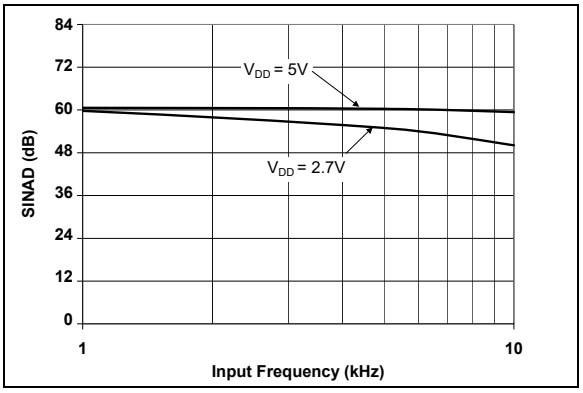


FIGURE 2-23: *SINAD vs. Input Frequency.*

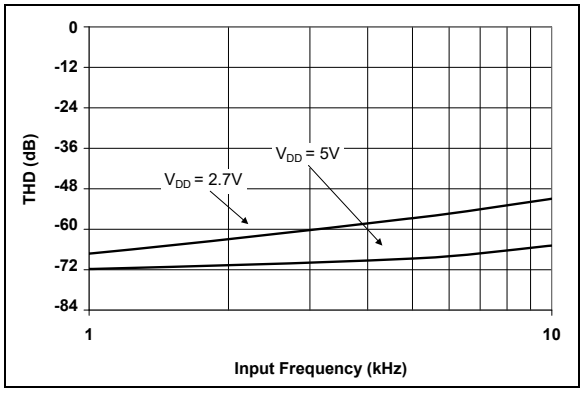


FIGURE 2-21: *THD vs. Input Frequency.*

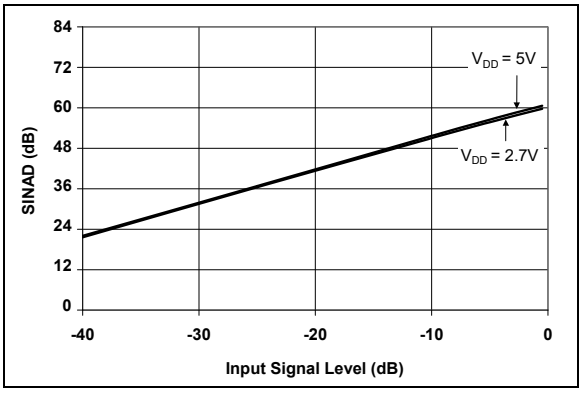


FIGURE 2-24: *SINAD vs. Input Signal Level.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (f_{SCL} = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

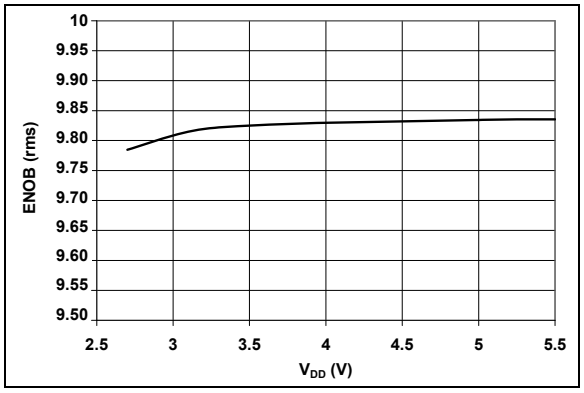


FIGURE 2-25: *ENOB vs. V_{DD}.*

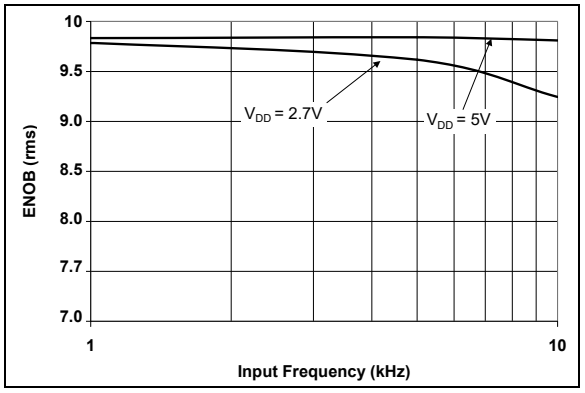


FIGURE 2-28: *ENOB vs. Input Frequency.*

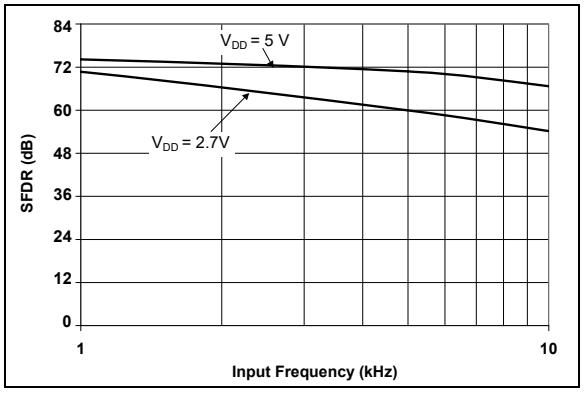


FIGURE 2-26: *SFDR vs. Input Frequency.*

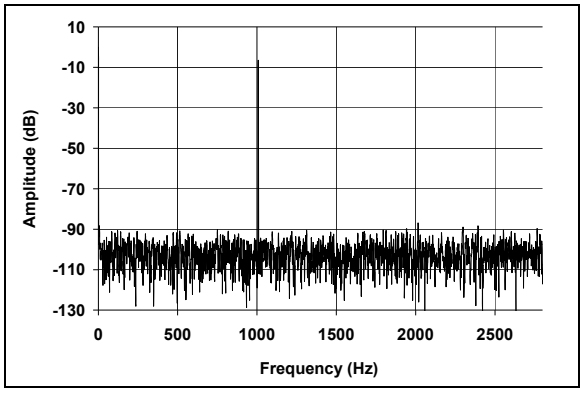


FIGURE 2-29: *Spectrum Using I^2C Standard Mode. Representative Part, 1 kHz Input Frequency.*

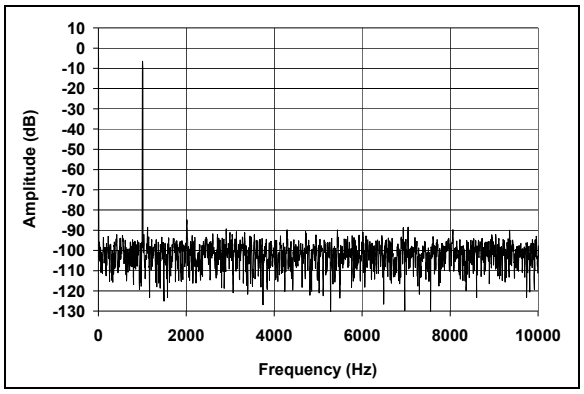


FIGURE 2-27: *Spectrum Using I^2C Fast Mode. Representative Part, 1 kHz Input Frequency.*

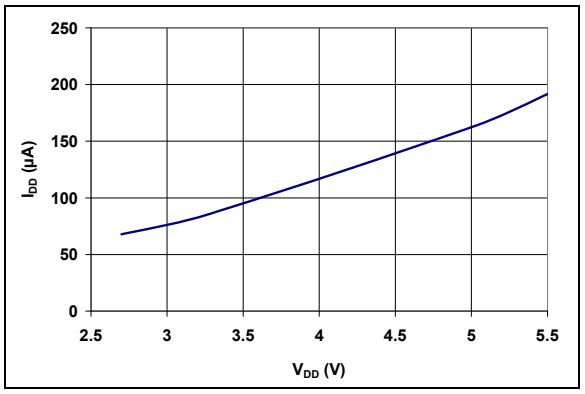


FIGURE 2-30: *I_{DD} (Conversion) vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (f_{SCL} = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

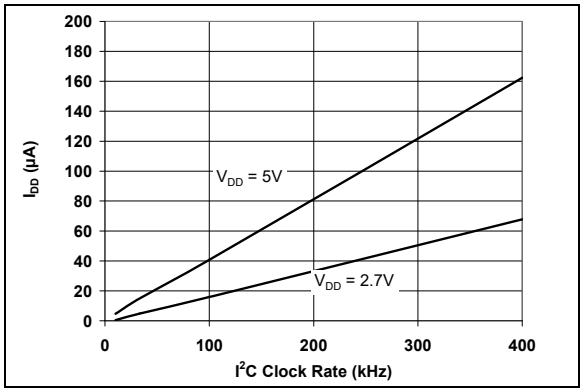


FIGURE 2-31: *I_{DD} (Conversion) vs. Clock Rate.*

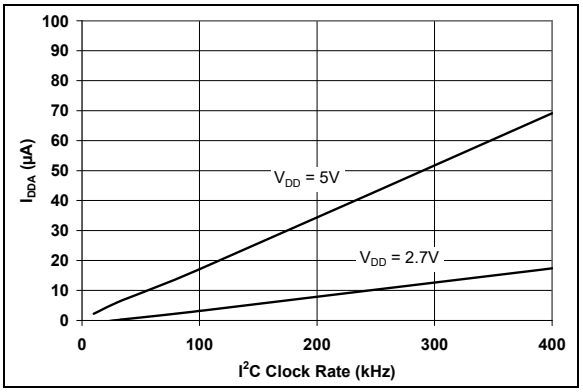


FIGURE 2-34: *I_{DDA} (Active Bus) vs. Clock Rate.*

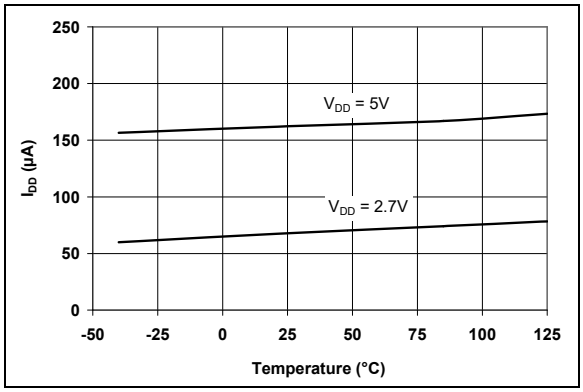


FIGURE 2-32: *I_{DD} (Conversion) vs. Temperature.*

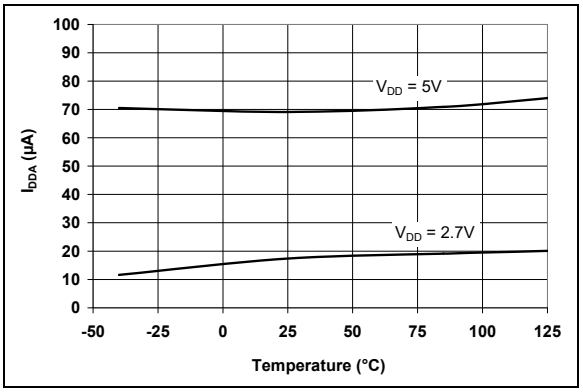


FIGURE 2-35: *I_{DDA} (Active Bus) vs. Temperature.*

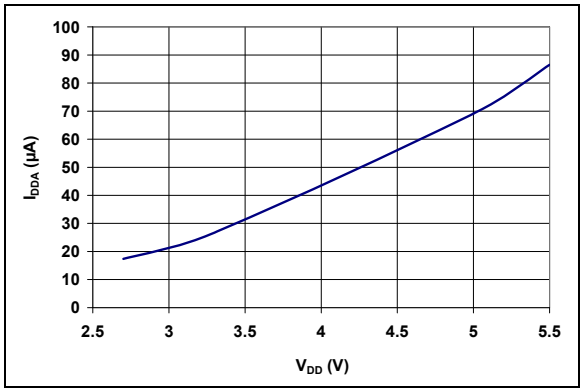


FIGURE 2-33: *I_{DDA} (Active Bus) vs. V_{DD}.*

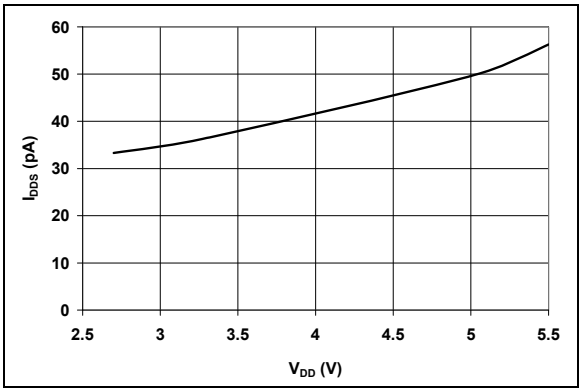


FIGURE 2-36: *I_{DDS} (Standby) vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (f_{SCL} = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

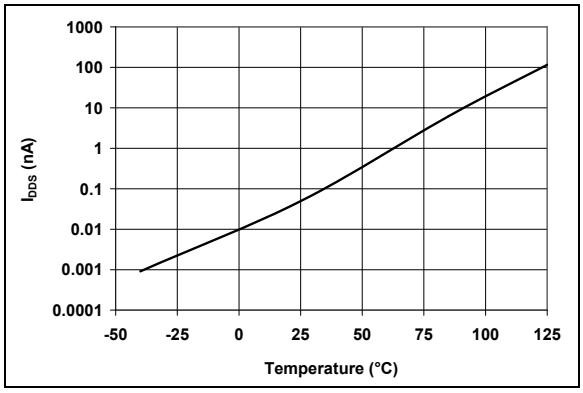


FIGURE 2-37: *I_{DDS} (Standby) vs. Temperature.*

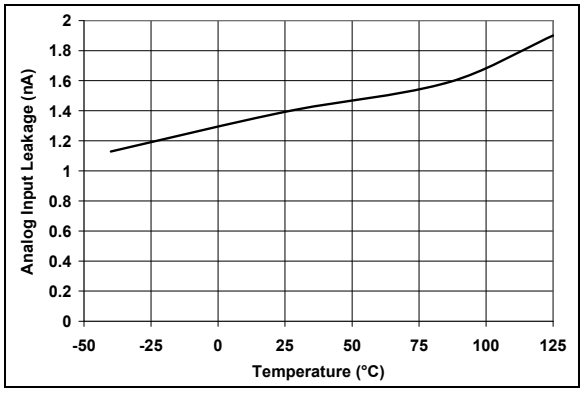


FIGURE 2-38: *Analog Input Leakage vs. Temperature.*

2.2 Test Circuits

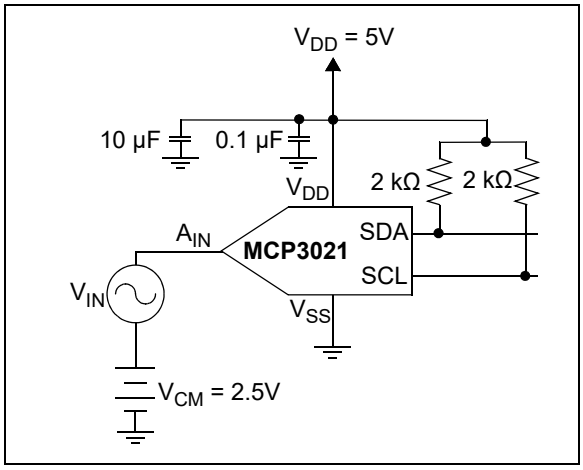


FIGURE 2-39: *Typical Test Configuration.*

3.0 PIN DESCRIPTION

Table 3-1 lists the function of the MCP3021 pins.

TABLE 3-1: MCP3021 PIN DESCRIPTIONS

Pin	Symbol	Description
1	V_{DD}	+2.7V to +5.5V Power Supply
2	V_{SS}	Ground
3	A_{IN}	Analog Input
4	SDA	Serial Data In/Out
5	SCL	Serial Clock In

3.1 V_{DD} and V_{SS}

The V_{DD} pin, with respect to V_{SS}, provides MCP3021 with power and also a voltage reference for the conversion process. Refer to **Section 6.4, "Device Power and Layout Considerations"** for tips on power and grounding.

3.2 Analog Input (A_{IN})

The A_{IN} pin is the input for the sample and hold circuitry of the Successive Approximation Register (SAR) converter. Ensure proper care when driving this pin. Refer to **Section 6.1, "Driving the Analog Input"** for more information. For proper conversions, the voltage on the A_{IN} pin can vary from V_{SS} to V_{DD}.

3.3 Serial Data (SDA)

SDA is a bidirectional pin that transfers addresses and data in and out of MCP3021. Being an open-drain terminal, the SDA bus requires a pull-up resistor connected to V_{DD} (typically 10 kΩ for f_{SCL} = 100 kHz and 2 kΩ for f_{SCL} = 400 kHz). Refer to **Section 6.2, "Connecting to the I2C Bus"** for more information.

For normal data transfer, the SDA pin is allowed to change only when the SCL pin is low. Changes when the SCL pin is high are reserved for indicating START and STOP conditions. Refer to **Section 5.1, "I2C Bus Characteristics"** for more information.

3.4 Serial Clock (SCL)

SCL is an input pin that synchronizes data transfers to and from MCP3021 on the SDA pin. As an open-drain terminal, the SCL bus requires a pull-up resistor connected to V_{DD} (typically 10 kΩ for f_{SCL} = 100 kHz and 2 kΩ for f_{SCL} = 400 kHz). Refer to **Section 6.2, "Connecting to the I2C Bus"** for more information.

For normal data transfer, the SDA pin is allowed to change only when the SCL pin is low. Changes when the SCL pin is high are reserved for indicating START and STOP conditions. Refer to **Section 6.1, "Driving the Analog Input"** for more information.

4.0 MCP3021 DEVICE OPERATION

4.1 General Description

MCP3021 employs a classic SAR architecture with an internal sample and hold capacitor to store the analog input during conversion. When acquisition time ends, the input switch of the converter opens and MCP3021 uses the collected charge on the internal sample and hold capacitor to produce a serial 10-bit digital output code. Acquisition time and conversion are self-timed using an internal clock. After each conversion, results are stored in a 10-bit register that can be read at any time.

Communication with MCP3021 is done over a 2-wire I^2C interface. Maximum sample rates of 22.3 ksps are possible when the device is in a continuous-conversion mode and uses a SCL clock rate (f_{SCL}) of 400 kHz.

4.2 Digital Output Code

The digital output code produced by MCP3021 is a function of the input signal and power supply voltage, V_{DD}. As V_{DD} level decreases, LSB size decreases accordingly. Equation 4-1 shows the theoretical LSB size.

EQUATION 4-1:

$$\text{LSB Size} = \frac{V_{DD}}{1024}$$

Where:

$LSB\ Size$ = Size of the Least Significant Bit (V)

V_{DD} = Power Supply Voltage (V)

The output code of MCP3021 is transmitted serially with the MSB first. The format of the code is straight binary.

4.3 Conversion Time (t_{CONV})

Conversion time is the duration needed to obtain the digital result after the analog input is disconnected from the holding capacitor.

For MCP3021, the conversion time is typically 8.96 µs. This period depends only on the internal oscillator and is not influenced of SCL.

4.4 Acquisition Time (t_{ACQ})

Acquisition time is the period needed to charge the sampling capacitor array.

For MCP3021, the acquisition time is typically 1.12 µs. This period depends only on the internal oscillator and is not influenced of SCL.

4.5 Sample Rate

Sample rate is the reciprocal of the maximum period between the acquisition of the first conversion to the acquisition of the second conversion.

Sample rate can be measured using either single or continuous conversions.

A single conversion includes the following:

- A single START bit
- A single Address byte
- Two Data bytes
- A single STOP bit

For single conversions, the sample rate is measured between consecutive START bits.

For continuous conversions, the sample rate is measured between consecutive conversions or for a total of 18 clocks (two data bytes and two Acknowledge bits). The Host device requests a continuous conversion by issuing an Acknowledge after a conversion. Refer to **Section 5.2, "Device Addressing"** for more information.

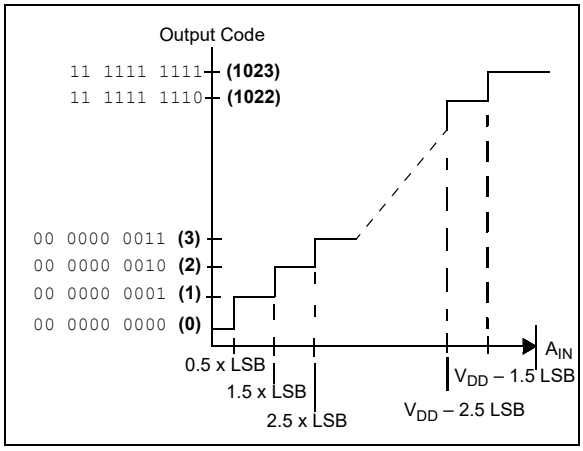


FIGURE 4-1: *Transfer Function.*

4.6 Differential Nonlinearity (DNL)

In the ideal ADC transfer function, each digital code has a uniform width, meaning the difference in analog input voltage is constant from one code transition point to the next. Differential nonlinearity (DNL) measures the deviation of any code in the transfer function from an ideal code width of 1 LSB. The DNL is calculated by subtracting the positions of consecutive code transition points after compensating for any gain and offset errors. A positive DNL indicates that a code is longer than the ideal code width, while a negative DNL means a code is shorter than the ideal width.

4.7 Integral Nonlinearity (INL)

Integral nonlinearity (INL) is the result of cumulative DNL errors and it measures the deviation of the overall transfer function from a linear response. The MCP3021 ADC uses the end-point measurement method to determine INL.

4.8 Offset Error

The offset error is the deviation of the code transition points that occurs across all output codes, effectively shifting the entire ADC transfer function. Measure this error by determining the difference between the actual position of the first code transition and its ideal position. Ideally, the first code transition occurs at 0.5 LSB above V_{SS}.

4.9 Gain Error

The gain error is the deviation from the ideal slope of the ADC transfer function. Before determining the gain error, first measure the offset error and subtract it from the conversion result. Then calculate the gain error by determining the difference between the actual position of the last code transition and its ideal position. Ideally, the last code transition occurs at 1.5 LSB below Full Scale or V_{DD}.

4.10 Conversion Current (I_{DD})

The conversion current, I_{DD}, is the amount of current consumed by MCP3021 averaged over the time needed to perform a 10-bit conversion.

4.11 Active Bus Current (I_{DDA})

The active bus current, I_{DDA}, is the amount of current consumed by MCP3021 averaged over the time needed to monitor the I^2C bus. This is the current consumed by the device while it is not addressed.

4.12 Standby Current (I_{DDS})

The standby current, I_{DDS}, is the amount of current consumed by MCP3021 averaged over the time when the SCL and SDA lines are inactive (no conversions occur and no data are outputted).

4.13 I^2C Timing

MCP3021 uses the following two I^2C timing modes as defined per I^2C specifications:

- Standard Mode — the SCL frequency is 100 kHz: f_{SCL} = 100 kHz.
- Fast Mode — the SCL frequency is 400 kHz: f_{SCL} = 400 kHz.

5.0 SERIAL COMMUNICATIONS

5.1 I²C Bus Characteristics

The following bus protocols are defined:

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock (SCL) line is high. Any changes in the data line while the SCL line is high are interpreted as a START or STOP condition.

Accordingly, the following bus conditions are defined (refer to Figure 5-1).

5.1.1 BUS NOT BUSY (A)

Both data and clock lines remain high.

5.1.2 START DATA TRANSFER (B)

A high-to-low transition on the data (SDA) line while SCL is high determines a START condition.

Note: All commands must begin with a START condition.

5.1.3 STOP DATA TRANSFER (C)

A low-to-high transition on the SDA line while SCL is high determines a STOP condition.

Note: All commands must end with a STOP condition.

5.1.4 DATA VALID (D)

Valid data is transmitted on the SDA line when, after a START condition, the data line is stable for the duration of the SCL high period.

The data on the line must change only during the SCL low period. There is one clock pulse per bit of data.

Every data transfer begins with a START condition and terminates with a STOP condition. The Host device determines the number of data bytes transferred between the START and STOP conditions. This number is unlimited.

5.1.5 ACKNOWLEDGE

Every receiving device, when addressed, generates an Acknowledge (ACK) bit after receiving each byte. The Host device must generate an extra clock pulse that is associated with this ACK bit.

The acknowledging device has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable and low during the high period of the ACK clock pulse. Consider setup and hold times. During reads, the Host device must signal an end of data to the Client device by not generating an ACK bit when the last byte is clocked out of the client device. In this case, the Client device (MCP3021) releases the bus to allow the Host device to generate the STOP condition.

MCP3021 supports a bidirectional, 2-wire bus and data transmission protocol. The device that sends data onto the bus is called the transmitter and the device that receives the data is called the receiver. A Host device controls the bus. It produces the serial clock (SCL), manages bus access and generates START and STOP conditions. MCP3021 functions as a Client device. While both Host and Client devices can operate as transmitter or receiver, only the Host device determines what mode to activate.

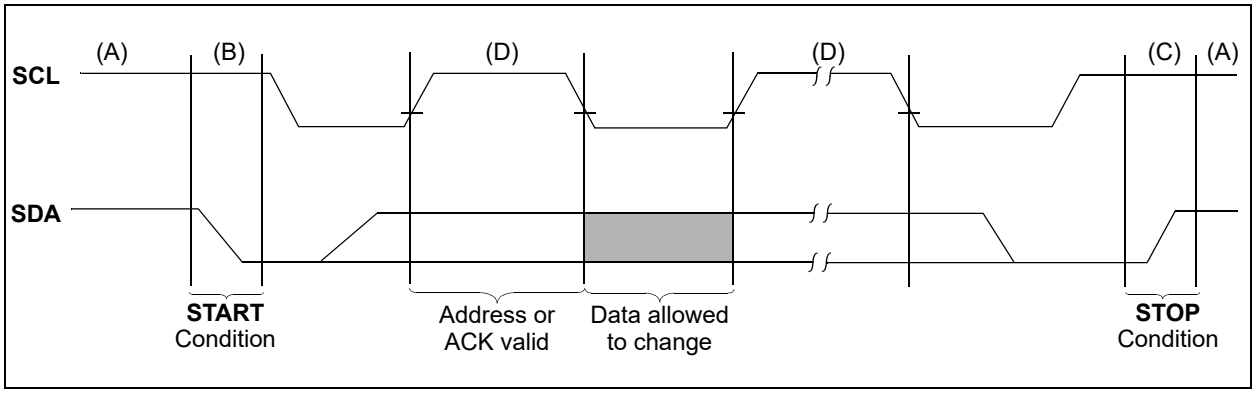


FIGURE 5-1: *Data Transfer Sequence on the Serial Bus.*

5.2 Device Addressing

The address byte is the first byte received after the START condition from the Host device. The first part of the address byte consists of a 4-bit device code. For MCP3021, this code is set to 1001.

The device code is followed by three address bits: A2, A1 and A0. The default address bits are 101.

Note: Contact the Microchip factory for additional address bit options.

The address bits allow up to eight MCP3021 devices on the same bus and they specify the target device.

The 8th and last bit of the address byte is called the Read/Write (R/$\overline{W}$) bit. It determines the operation type requested by the Host device:

- To read conversion data, the R/$\overline{W}$ bit is set to 1.
- To write to a registry, the R/$\overline{W}$ bit is set to 0.

However, MCP3021 has no writable registers. Thus, if the R/$\overline{W}$ address bit received by MCP3021 is set to 1, it triggers a conversion.

MCP3021 is a Client device that is compatible with the 2-wire I^2C serial interface protocol. Figure 6-2 shows a hardware connection diagram. The microcontroller unit (MCU) on the Host device initiates communication and sends a START condition followed by the address byte.

After MCP3021 completes the conversion(s), the MCU must send a STOP condition to end communication.

When receiving R/$\overline{W}$ = 0, MCP3021 returns an ACK and then releases the bus. This behavior can be used to poll the device. For more information, refer to **Section 6.3, "Device Polling"**.

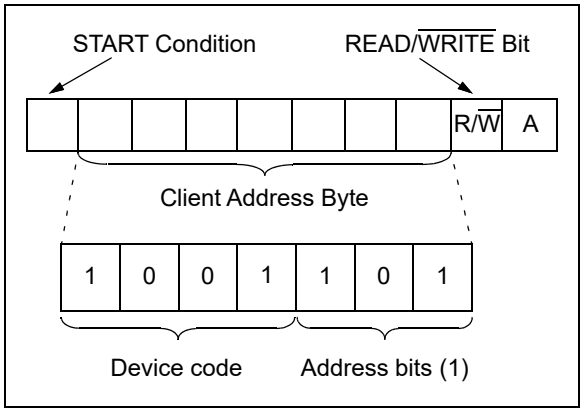


FIGURE 5-2: *Device Addressing.*

5.3 Executing a Conversion

This section describes the details of communicating with MCP3021. These include the initiation of sample and hold acquisition, the reading the conversion data and the execution of multiple conversions.

5.3.1 INITIATE SAMPLE AND HOLD ACQUISITION

The acquisition and conversion of the input signal begins with the falling edge of the R/$\overline{W}$ bit, part of the address byte. At this point, the internal clock initiates the sample, hold and conversion cycle, all of them being internal to the ADC.

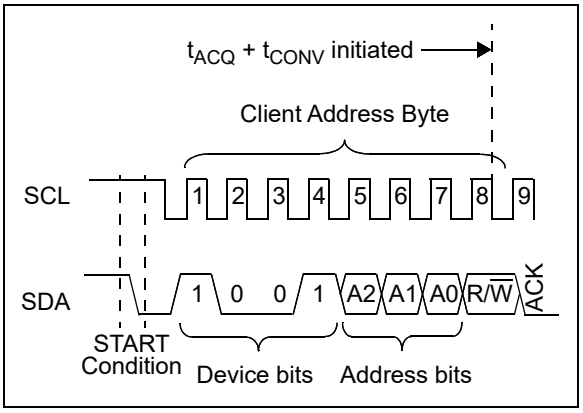


FIGURE 5-3: *Conversion Initiation, Address Byte.*

The input signal is initially sampled with the first SCL falling edge following the transmission of a logic-high R/$\overline{W}$ bit. Additionally, with the SCL rising edge, the ADC transmits an ACK = 0 bit. The Host device releases the data bus during this clock pulse to allow MCP3021 to pull the line low (see Figure 5-3).

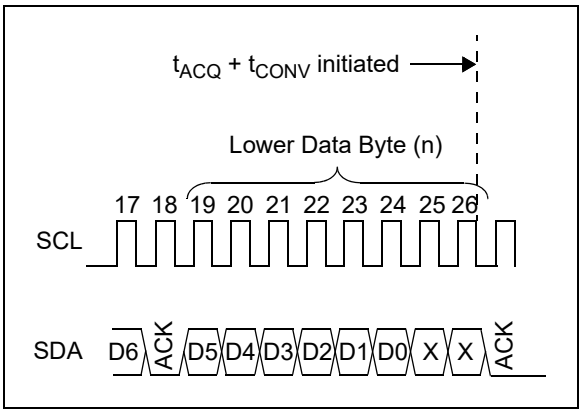


FIGURE 5-4: *Conversion Initiation, Continuous Conversions.*

5.3.2 READ CONVERSION DATA

After the MCP3021 acknowledges the address byte, the device transmits four 0 bits, followed by the upper four data bits of the conversion. The Host device responds to this byte with an ACK = Low. With the following six clock pulses, the MCP3021 transmits the lower six data bits from the conversion. The last two bits are “don’t cares”, and do not contain valid data. The master sends an ACK = high, indicating to the MCP3021 that no more data is requested. The Master can send a Stop bit to end the transmission.

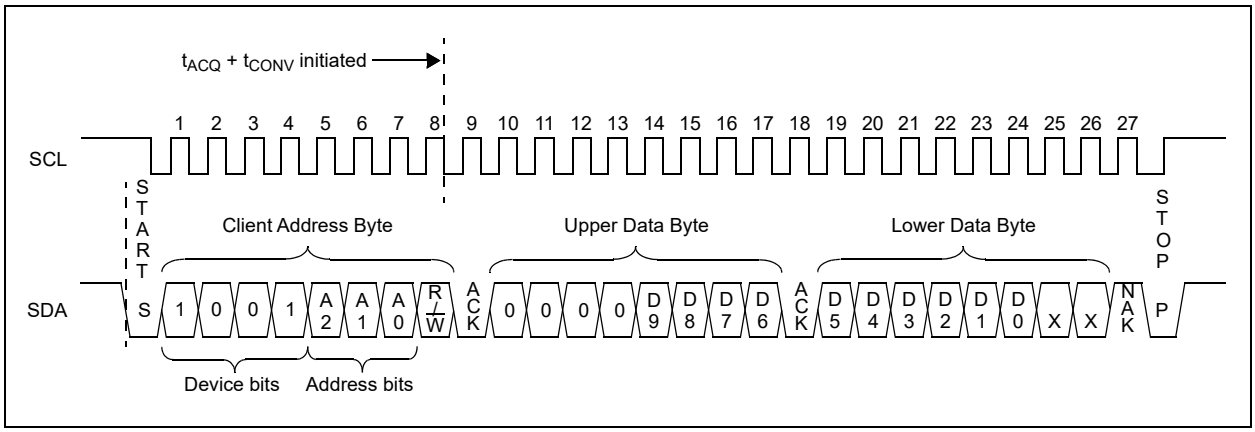


FIGURE 5-5: *Executing a Conversion.*

5.3.3 CONSECUTIVE CONVERSIONS

For consecutive conversions, sampling starts on the falling edge of the LSB of the conversion result. The LSB is two bytes in length. Figure 5-6 shows the timing diagram.

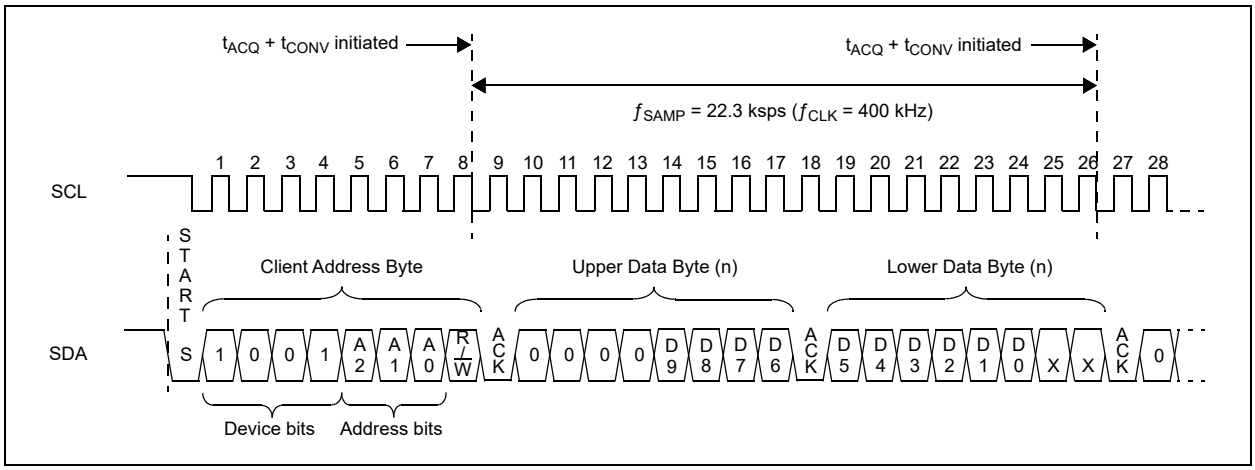


FIGURE 5-6: *Continuous Conversion.*

6.0 APPLICATION INFORMATION

6.1 Driving the Analog Input

MCP3021 has a single-ended analog input, A_{IN}. For proper conversion results, ensure the voltage at the A_{IN} pin remains between V_{SS} and V_{DD}. If the converter has no offset error, gain error, INL or DNL errors and the voltage level of A_{IN} is ≤ V_{SS} + 0.5 x LSB, the output code is `000h`. If the voltage at A_{IN} is ≥ V_{DD} – 1.5 x LSB, then the output code is instead `1FFh`.

The analog input model in Figure 6-1 shows how the source impedance (R_S) adds to the impedance of the internal sampling switch (R_{SS}), directly affecting the time required to charge capacitor C_{SAMPLE}. Thus, a larger source impedance increases the offset, gain and INL errors of the conversion. Ideally, $R_S \approx 0\Omega$. This is done using an operational amplifier with a closed-loop output impedance of tens of ohms, such as MCP6022.

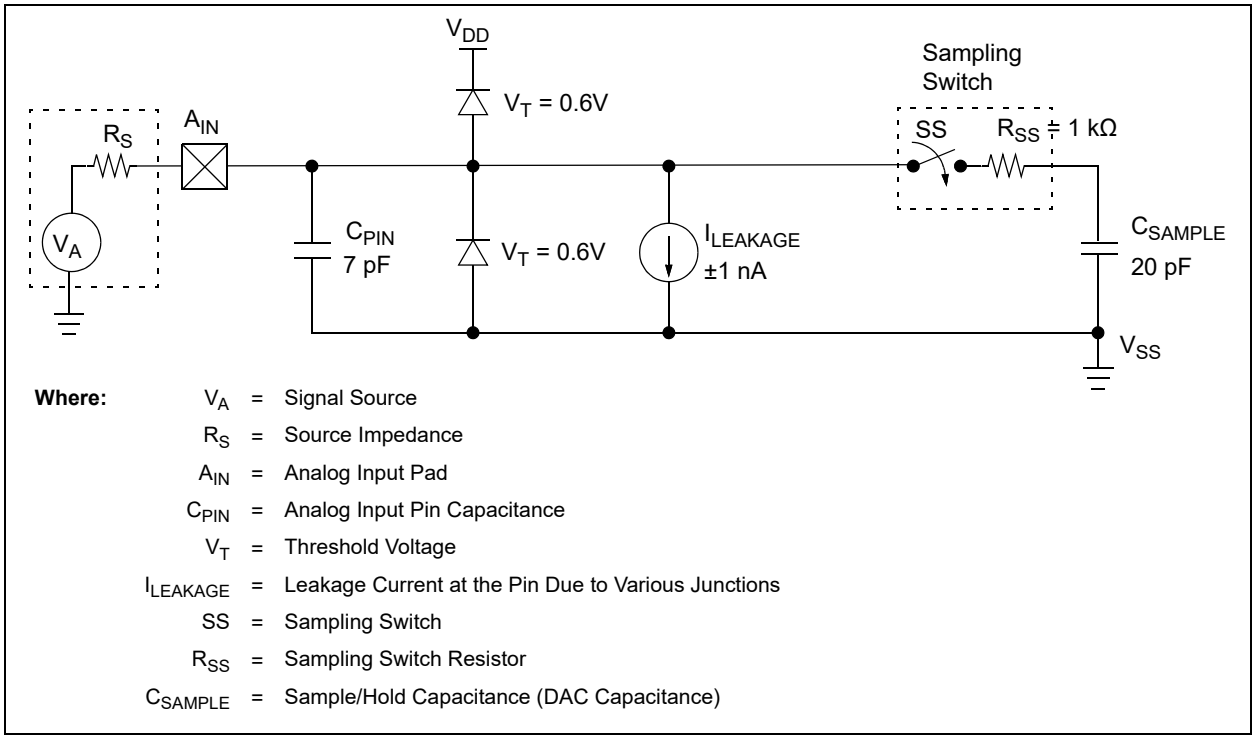


FIGURE 6-1: *Analog Input Model, A_{IN}.*

6.2 Connecting to the I²C Bus

The I²C bus is an open collector bus, requiring pull-up resistors (R_{PU}) connected to the SDA and SCL lines. Figure 6-2 shows this configuration.

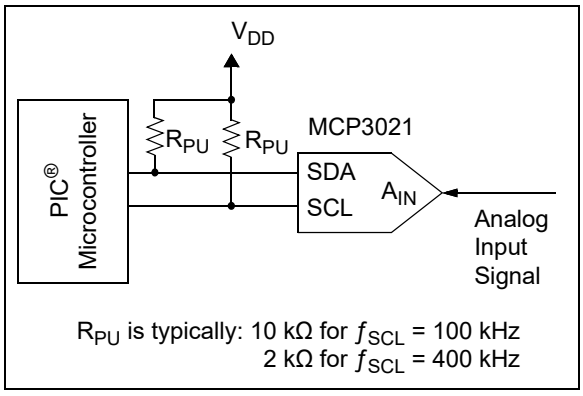


FIGURE 6-2: *Pull-up Resistors on I²C Bus.*

The number of devices connected to the bus is limited only by the maximum bus capacitance of 400 pF. Figure 6-3 shows a possible configuration with multiple devices connected to the same I²C bus.

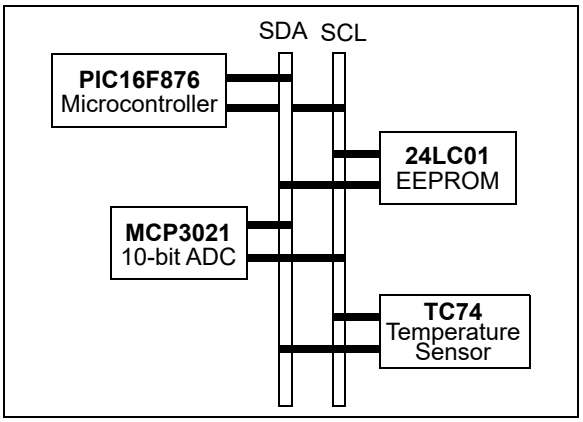


FIGURE 6-3: *Multiple Devices on I²C Bus.*

6.3 Device Polling

Sometimes, it is necessary to test for the presence of MCP3021 on the I^2C bus without doing a conversion. This is described in Figure 6-4, where the R/$\overline{W}$ bit in the address byte is set to 0. MCP3021 acknowledges by pulling the SDA line low during the ACK clock and then releases the I^2C bus. The Host device can issue a STOP or a repeated START condition to continue I^2C communication.

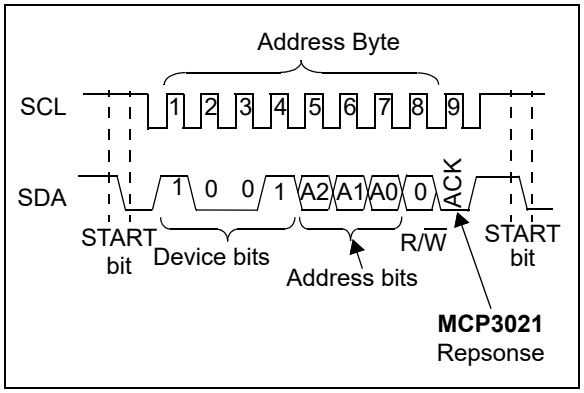


FIGURE 6-4: *Device Polling.*

6.4 Device Power and Layout Considerations

6.4.1 POWERING MCP3021

V_{DD} supplies MCP3021 with power and a reference voltage. Microchip recommends connecting a 0.1 µF bypass capacitor to V_{DD} in parallel with a 10 µF capacitor to attenuate higher frequency noise present in certain systems. Figure 6-5 shows this configuration.

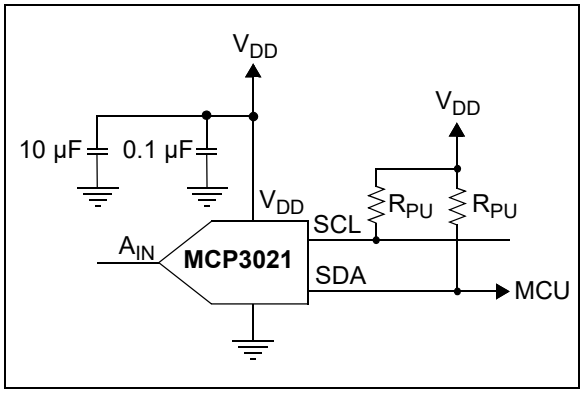


FIGURE 6-5: *Powering MCP3021.*

Note: When MCP3021 must be powered down during applications (after power-up), Microchip highly recommends to bring down V_{DD} to V_{SS} level. This ensures a Full Reset of the device for the next power-up cycle.

6.5 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor from V_{DD} to ground must be used always with this device and placed as close as possible to the device pin. A bypass capacitor value of 0.1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board, with no traces running underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high-frequency signals (such as clock lines) as far as possible from analog traces.

The MCP3021 must be connected entirely to the analog ground place as well as the analog power trace. The pull-up resistors can be placed close to the microcontroller and tied to the digital power or V_{CC}.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a Star configuration can also reduce noise by eliminating current return paths and associated errors (Figure 6-6).

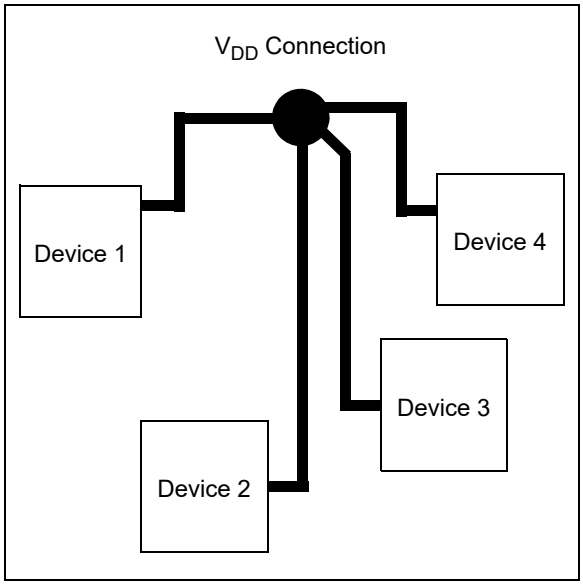


FIGURE 6-6: *V_{DD} Traces Arranged in a Star Configuration to Reduce Errors Caused by Current Return Paths.*

For more information on layout tips when using MCP3021 or other ADC devices, refer to the Microchip Technology Application Note AN688, "*Layout Tips for 12-Bit A/D Converter Application*" (DS00688).

6.5.1 USING A REFERENCE FOR THE SUPPLY VOLTAGE

MCP3021 uses V_{DD} as power and also as a reference voltage. In certain applications, it is necessary to use a stable reference to achieve the required accuracy. Figure 6-7 shows an example configuration using MCP1541 as a 4.096V, 2% voltage reference.

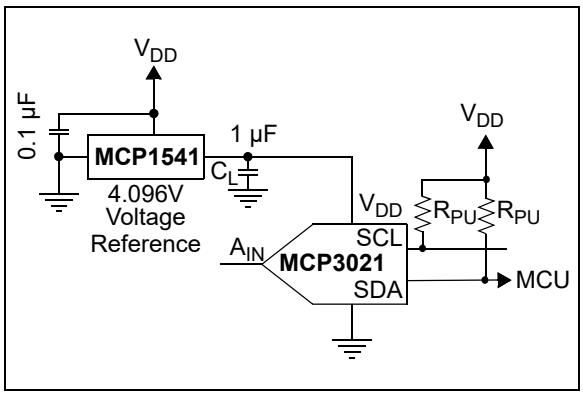


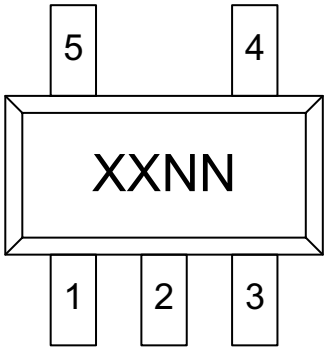
FIGURE 6-7: *Stable Power and Reference Configuration.*

7.0 PACKAGE INFORMATION

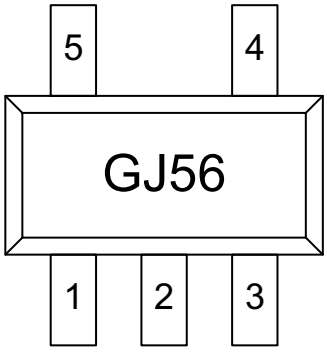
7.1 Package Marking Information

MCP3021

5-Lead SOT-23



Example:



Part Number	Address Option	Package Marking XX SOT-23
MCP3021A0T-E/OT	000	GP
MCP3021A1T-E/OT	001	GS
MCP3021A2T-E/OT	010	GK
MCP3021A3T-E/OT	011	GL
MCP3021A4T-E/OT	100	GM
MCP3021A5T-E/OT	101	GJ(*)
MCP3021A6T-E/OT	110	GQ
MCP3021A7T-E/OT	111	GR

* Default option. Contact Microchip Factory for other address options.

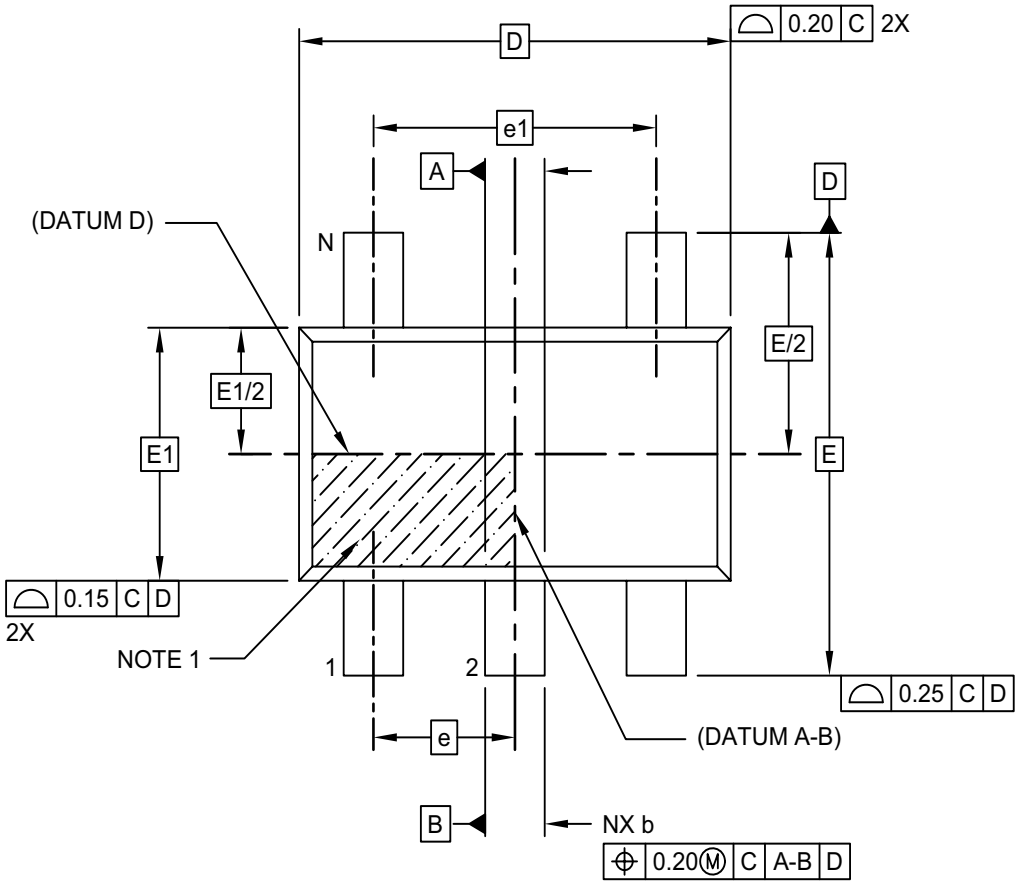
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

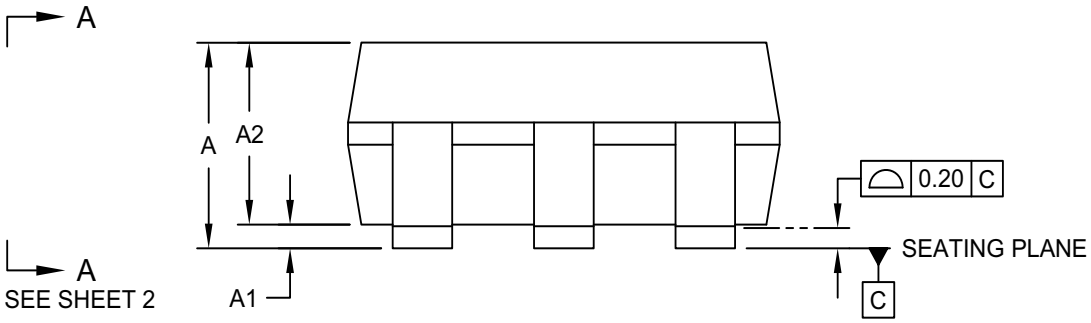
7.2 Package Drawings

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

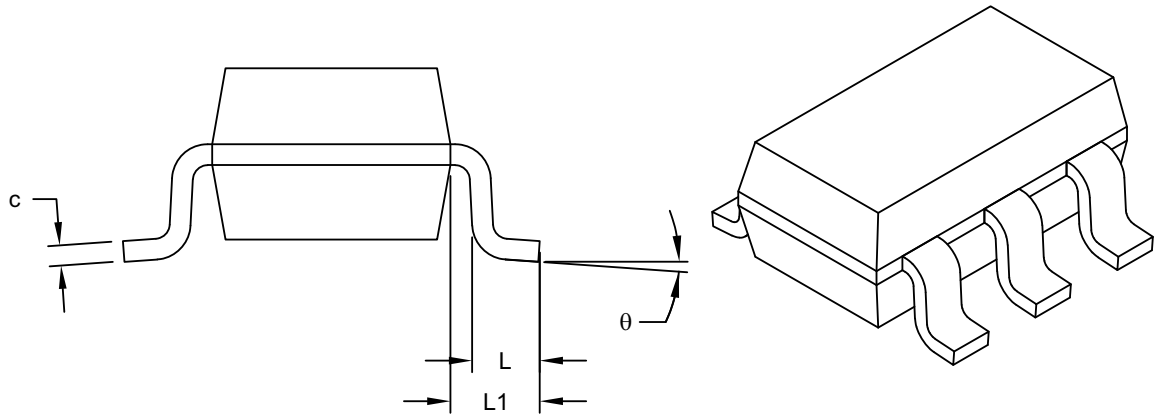


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

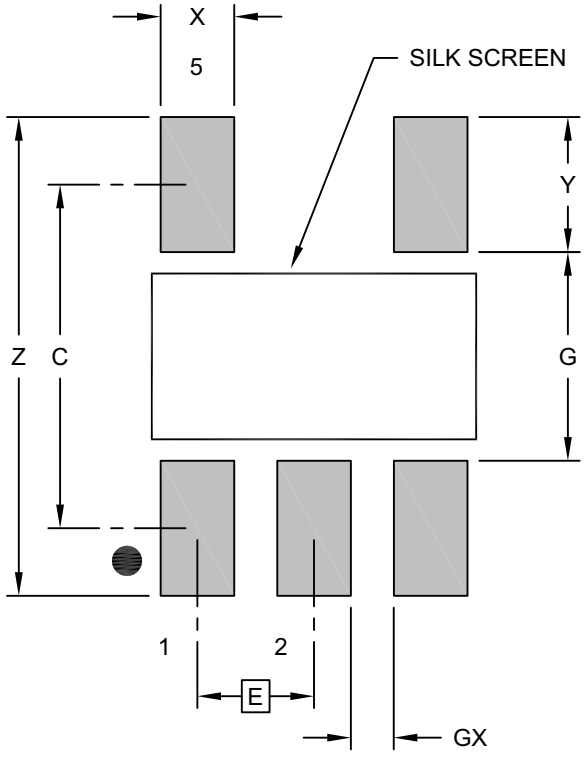
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev H

APPENDIX A: REVISION HISTORY

Revision D (April 2025)

Following is the list of changes for this revision:

- Added AEC-Q100 Qualification to **Features** and **General Description**.
- Added **Related Devices**.
- Updated the temperature range from industrial (-40°C to +85°C) to extended (-40°C to +125°C) in **Section 1.0, "Electrical Specifications"**.
- Updated Table 1-1, "DC Electrical Specifications" notes.
- Updated **Product Identification System**.
- Added **Product Identification System (Automotive)**.
- Changed terminology:
  - Master device → Host device
  - Slave device → Client device
- Updated **Section 7.1, "Package Marking Information"**.
- Updated package drawings in **Section 7.2, "Package Drawings"**.
- Several minor improvements to text formatting, parameter symbols and figures.
- Updated ***Trademark***, ***Legal Notice*** and ***Microchip Devices Code Protection Feature*** information. For details, refer to the **Microchip Information** page.
- Removed **Worldwide Sales and Service** page.

Revision C (January 2017)

Following is the list of changes for this revision:

- Added a note to **Section 6.4.1, "Powering MCP3021"**.
- Updated Figure 6-5.
- Fixed the format in **Section 7.1, "Package Marking Information"** reflect the correct package marking as “1 2 3 4” instead of “1 10 10 10”.

Revision B (January 2013)

Following is the list of changes for this revision:

- Added a note to each package outline drawing.

Revision A (June 2003)

Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X[2]	-X	/XX	XXX
Device	Address	Tape and Reel	Temperature Range	Package	Class

Device: MCP3021 = 10-Bit ADC with I^2C Interface

Address Option:

XX		Address Bits A2	A1	A0
A0	=	0	0	0
A1	=	0	0	1
A2	=	0	1	0
A3	=	0	1	1
A4	=	1	0	0
A5[1]	=	1	0	1
A6	=	1	1	0
A7	=	1	1	1

Tape and Reel Option: T = Tape and Reel[2]

Temperature Range: I = -40°C to +85°C (Industrial)
E = -40°C to +125°C (Extended)

Package: OT = 5-Lead Plastic Small Outline Transistor, SOT-23

Class: Blank = Non-automotive
VAO = Automotive

Note 1: Default Option. Contact Microchip factory for other address options.
2: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a) MCP3021A0T-E/OT = 10-Bit ADC I^2C Interface, Address A0, Tape and Reel, Extended Temperature, 5-Lead SOT-23

b) MCP3021A1T-E/OT = 10-Bit ADC I^2C Interface, Address A1, Tape and Reel, Extended Temperature, 5-Lead SOT-23

c) MCP3021A2T-E/OT = 10-Bit ADC I^2C Interface, Address A2, Tape and Reel, Extended Temperature, 5-Lead SOT-23

d) MCP3021A3T-E/OT = 10-Bit ADC I^2C Interface, Address A3, Tape and Reel, Extended Temperature, 5-Lead SOT-23

e) MCP3021A4T-E/OT = 10-Bit ADC I^2C Interface, Address A4, Tape and Reel, Extended Temperature, 5-Lead SOT-23

f) MCP3021A5T-E/OT = 10-Bit ADC I^2C Interface, Address A5, Tape and Reel, Extended Temperature, 5-Lead SOT-23

g) MCP3021A5T-I/OT = 10-Bit ADC I^2C Interface, Address A5, Tape and Reel, Industrial Temperature, 5-Lead SOT-23

h) MCP3021A6T-E/OT = 10-Bit ADC I^2C Interface, Address A6, Tape and Reel, Extended Temperature, 5-Lead SOT-23

i) MCP3021A7T-E/OT = 10-Bit ADC I^2C Interface, Address A7, Tape and Reel, Extended Temperature, 5-Lead SOT-23

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X(2)	-X	/XX	XXX
Device	Address	Tape and Reel	Temperature Range	Package	Class

Device: MCP3021 = 10-Bit ADC with I^2C Interface

Address Option:

XX		A2	A1	A0
A0	=	0	0	0
A1	=	0	0	1
A2	=	0	1	0
A3	=	0	1	1
A4	=	1	0	0
A5(1)	=	1	0	1
A6	=	1	1	0
A7	=	1	1	1

Tape and Reel Option: T = Tape and Reel(2)

Temperature Range: I = -40°C to +85°C (Industrial)
E = -40°C to +125°C (Extended)

Package: OT = 5-Lead Plastic Small Outline Transistor, SOT-23

Class: Blank = Non-automotive
VAO = Automotive

Note 1: Default Option. Contact Microchip factory for other address options.

2: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a) MCP3021A0T-E/OTVAO = 10-Bit ADC I^2C Interface, Address A0, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

b) MCP3021A1T-E/OTVAO = 10-Bit ADC I^2C Interface, Address A1, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

c) MCP3021A2T-E/OTVAO = 10-Bit ADC I^2C Interface, Address A2, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

d) MCP3021A3T-E/OTVAO = 10-Bit ADC I^2C Interface, Address A3, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

e) MCP3021A4T-E/OTVAO = 10-Bit ADC I^2C Interface, Address A4, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

f) MCP3021A5T-E/OTVAO = 10-Bit ADC I^2C Interface, Address A5, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

g) MCP3021A6T-E/OTVAO = 10-Bit ADC I^2C Interface, Address A6, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

h) MCP3021A7T-E/OTVAO = 10-Bit ADC I^2C Interface, Address A7, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

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