KSZ8081/KSZ8091

KSZ8081/KSZ8091 Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the KSZ8081/KSZ8091 family of devices, which includes the following:

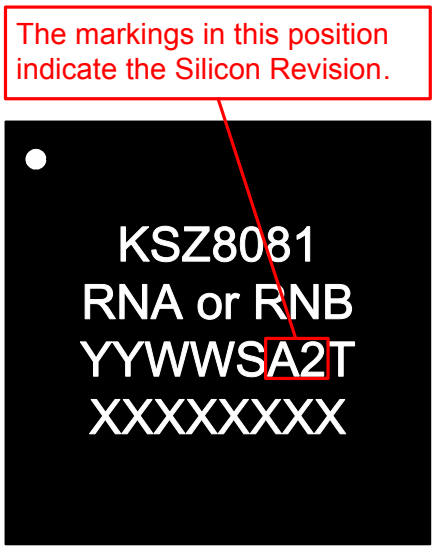
- KSZ8081RNB
- KSZ8081RNA
- KSZ8091RNB
- KSZ8091RNA
- KSZ8081RND
- KSZ8091RND
- KSZ8091MLX
- KSZ8091MNX

The silicon errata discussed in this document are for silicon with silicon revisions as listed in Table 1. The silicon revision can be determined by the device's top marking as indicated in Figure 1, or by reading device register 3h bits [3:0] (0x0 for silicon revisions A and A2, 0x1 for silicon revision A3). A summary of KSZ8081/KSZ8091 silicon errata is provided in Table 2.

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
KSZ8081RNB, KSZ8081RNA, KSZ8091RNB, KSZ8091RNA KSZ8081RND, KSZ8091RND, KSZ8091MLX, KSZ8091MNX	A, A2

FIGURE 1: TOP MARKING SILICON REVISION INDICATION



Note: The purpose of Figure 1 is to detail the top markings of an example part and highlight the location of the silicon revision. Other top marking values may differ (lot codes, location of manufacture, etc.).

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	Random RMII transmitter errors can occur in RMII 25 MHz clock mode	A, A2
2.	Link drop/packet loss in 100BASE-TX Energy Efficient Ethernet (EEE) Mode	A, A2

Silicon Errata Issues

Module 1: Random RMII transmitter errors can occur in RMII 25 MHz clock mode

DESCRIPTION

RMII Transmit errors can occur internal to the PHY on a minority of A and A2 devices. This is due to the internal data clock edges being aligned with the external 25 MHz RMII clock. When these two clocks are aligned, the data is not sampled properly into the transmit buffer.

This silicon issue affects the following device part numbers:

- KSZ8081RNA
- KSZ8081RNB
- KSZ8081RND
- KSZ8091RNA
- KSZ8091RNB
- KSZ8091RND

Silicon revision A3 locks the 25/50 MHz clock phase at the RMII transmit FIFO to correct this issue.

END USER IMPLICATIONS

When the failure occurs, transmit traffic errors will occur on the line interface.

Work Arounds

Microchip recommends that all customers use revision A3 to avoid this issue. For existing designs that cannot change, there are three possible work arounds. In priority order, these are:

Software work around 1:

1. Set register 0h to 0x6100 to enable local digital loopback after power up.
2. Send packets from the processor (MAC) and verify if all packets are looped back without error.
3. If any error occurs during loopback, toggle register 0h bit [11] from “0” to “1” and back to “0” to configure the PHY to power-down and then power-up. Repeat step 2.
4. If no error occurs during loopback, set register 0h to the default or desired value. The device can now be used for normal operation.

Software work around 2:

1. Set register 0h to 0x6100 to enable local digital loopback after power up.
2. Send packets from the processor (MAC) and verify if all packets are looped back without error.
3. If any error occurs during loopback, set the internal REFCLK register 19h bits [15:12] from their default value of 0x7 to 0x15 (+0.6 ns) or 0x00 (-0.6 ns) to adjust the REFCLK pad skew. Repeat step 2.
4. If no error occurs during loopback, set register 0h to the default or desired value. The device can now be used for normal operation.

Software work around 3:

1. Set register 0h to 0x6100 to enable local digital loopback after power up.
2. Send packets from the processor (MAC) and verify if all packets are looped back without error.
3. If any error occurs during loopback, set register 11h bit [15] to “1” to enable I/O drive current strength adjustment. Set the drive current strength via register 11h bits [14:13] (00=8 mA, 01=4 mA, 10=14 mA, 11=10 mA). Repeat step 2.
4. If no error occurs during loopback, set register 0h to the default or desired value. The device can now be

used for normal operation.

PLAN

This erratum has been corrected in silicon revision A3.

Module 2: Link drop/packet loss in 100BASE-TX Energy Efficient Ethernet (EEE) Mode

DESCRIPTION

In 100BASE-TX EEE mode, the link partner may drop link or loss packet when the local MAC/PHY (device) starts to transmit the “Wake” signal immediately following the “Sleep”/“Refresh” signal to exit Low-Power Idle mode and return to Active mode.

Many EEE PHY link partners require a short “Quiet” (Tq) duration after receiving the “Sleep”/“Refresh” signal. Without this short Tq wait time, that is not specified in the IEEE 802.3az Standard, link drop or packet loss can occur.

FIGURE 2: OVERVIEW OF EEE LPI OPERATION

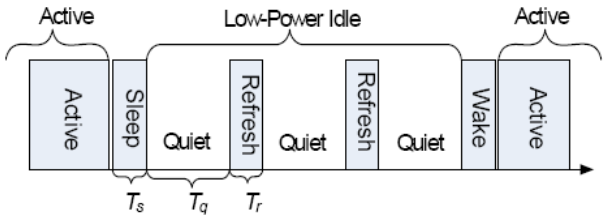


Figure 78–3—Overview of EEE LPI operation

This silicon issue affects the following device part numbers:

- KSZ8091RNA
- KSZ8091RNB
- KSZ8091RND
- KSZ8091MNX
- KSZ8091MLX

END USER IMPLICATIONS

100BASE-TX EEE Mode does not work properly. Link drops and packet losses can occur randomly.

Work Arounds

None. Do not enable 100BASE-TX EEE Mode.

PLAN

This anomaly will not be fixed in a future revision of the device.

APPENDIX A: DOCUMENT REVISION HISTORY

TABLE A-1: CUSTOMER REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000708B (02-24-17)	Table 1	Added the following part numbers: • KSZ8081RND • KSZ8091RND • KSZ8091MLX • KSZ8091MNX
	Module 1: Random RMII transmitter errors can occur in RMII 25 MHz clock mode	Updated module to include which part numbers are affected.
	Module 2: Link drop/packet loss in 100BASE-TX Energy Efficient Ethernet (EEE) Mode	Added Module
DS80000708A (08-22-16)	All	Initial release

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