AN3621

LAN9252 to LAN9253 and LAN9254 Migration Guide

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INTRODUCTION

The AN3621 LAN9252 to LAN9253 and LAN9254 Migration Guide is intended for customers migrating an existing LAN9252 board design to either LAN9253 or LAN9254 design. This application note details pin differences between the LAN9252 and LAN9253 as well as configuration strap differences between the LAN9252 and LAN9253/LAN9254. This document also contains comparative register data on the devices.

SECTIONS

This document covers the following topics:

REFERENCES

Refer to the following documents when using this application note. See your Microchip representative for availability:

- *LAN9252 2/3-Port EtherCAT® Slave Controller with Integrated Ethernet PHYs Data Sheet*
- *LAN9253 2/3-Port EtherCAT® Slave Controller with Integrated Ethernet PHYs Data Sheet*
- *LAN9254 2/3-Port EtherCAT® Slave Controller with Integrated Ethernet PHYs and Demultiplexed HBI/32 DIGIOs Data Sheet*

PIN DIFFERENCES BETWEEN LAN9252 AND LAN9253

This section provides the pin differences between LAN9252 and LAN9253 devices. Please refer to Table 1.

TABLE 1: PIN COMPARISON BETWEEN LAN9252 AND LAN9253

Pin	LAN9252	LAN9253
8	FXLOSEN	CLK_25/CLK_25_EN/XTAL_MODE
9	FXSDA/FXLOSA/FXSDENA	ERRLED/PME/100FD_B/LEDPOL4
10	FXSDB/FXLOSB/FXSDENB	WAIT_ACK/PME/LATCH0//EE_EMUL_SPI3
12	D2/AD2/SOF/SIO2	D2/AD2/SOF/SIO2/EE_EMUL_SPI0
21	D12/AD12/DIGIO6/GPI6/GPO6/MII_TXD1	D12/AD12/DIGIO6/GPI6/GPO6/MII_TXD1/100FD_B
22	D11/AD11/DIGIO5/GPI5/GPO5/MII_TXD0	D11/AD11/DIGIO5/GPI5/GPO5/MII_TXD0/100FD_A
25	A1/ALELO/OE_EXT/MII_CLK25	A1/ALELO/OE_EXT/MII_CLK25//EE_EMUL_SPI2
29	A2/ALEHI/DIGIO10/GPI10/GPO10/LINKACTLED2/ MII_LINKPOL	A2/ALEHI/DIGIO10/GPI10/GPO10/LINKACTLED2/ EE_EMUL_ALELO_POL/MII_LINKPOL/LEDPOL2
34	SYNC0/LATCH0	SYNC0/LATCH0/PME
35	D3/AD3/WD_TRIG/SIO3	D3/AD3/WD_TRIG/SIO3/EE_EMUL_SPI1
42	EESDA/TMS	EESDA/TMS/EE_EMUL1
43	EESCL/TCK	EESCL/TCK/EE_EMUL2
44	IRQ	IRQ/LATCH1
45	RUNLED/E2PSIZE	RUNLED/STATE_RUNLED/E2PSIZE/EE_EMUL0/LED-POL3
46	LINKACTLED1/TDI/CHIP_MODE1	LINKACTLED1/TDI/CHIP_MODE1/LEDPOL1
48	LINKACTLED0/TDO/CHIP_MODE0	LINKACTLED0/TDO/CHIP_MODE0/100FD_A/LEDPOL0

Note: LAN9254 is an 80-pin device. Please visit the LAN9254 device data sheet for detailed information on the device's pinout.

CONFIGURATION STRAP DIFFERENCES

This section shows the configuration straps for LAN9253. Table 2 outlines the only hardware configuration straps that are different than LAN9252. A user needs to configure these straps depending on the application.

TABLE 2: DIFFERENCES IN LAN9253 STRAP CONFIGURATION

Pin	Strap Name	Description
EE_EMUL2, EE_EMUL1	eeprom_emulation_strap	**EEPROM Emulation Strap** This configures the ESC to redirect EEPROM reads and writes to the microcontroller.
EE_EMUL2, EE_EMUL1, EE_EMUL0	ee_emul_pdi_sel_strap[2:0]	**EEPROM Emulation PDI Select Strap** This configures the default PDI selection during EEPROM Emulation mode.
EE_EMUL_ALELO_POL	ee_emul_alelo_pol_strap	**EEPROM Emulation ALELO Polarity Strap** During EEPROM Emulation mode, if the default PDI selection is set to HBI Multiplexed 1 Phase, this strap is used to set bit 2 – HBI ALE polarity of the PDI Configuration register (0x0150) – HBI modes until the EEPROM configuration data have been loaded.

TABLE 2: DIFFERENCES IN LAN9253 STRAP CONFIGURATION (CONTINUED)

Pin	Strap Name	Description
EE_EMUL_SPI3, EE_EMUL_SPI2, EE_EMUL_SPI1, EE_EMUL_SPI0	ee_emul_spi[3], ee_emul_spi[2], ee_emul_spi[1:0]	**EEPROM Emulation SPI Straps** During EEPROM Emulation mode, if the default PDI selection is set to Beckhoff-compatible SPI mode, these straps are used to set the value of PDI Configuration register (0x0150) – Beckhoff SPI mode until the EEPROM configuration data have been loaded. ee_emul_spi[3] configures bit 5 – Data Out sample ee_emul_spi[2] configures bit 4 – SCS# polarity ee_emul_spi[1:0] configure bits 1:0 – SPI mode
100FD_A 100FD_B	100FD_strap_A 100FD_strap_B	**100 Mbps/Full-Duplex Strap** These straps configure the default of the ANEG Disable PHY A/B and AMDIX Disable PHY A/B fields in the Hardware Configuration register (HW_CFG), which in turn sets the corresponding internal PHY to fixed 100 Mbps, full-duplex operation by default.
LEDPOL4 LEDPOL3 LEDPOL2 LEDPOL1 LEDPOL0	led_pol_strap[4:0]	**LED Polarity Strap** This configures the default of the LED Polarity field in the Hardware Configuration register (HW_CFG) for each of the LEDs. 0 = The LED is set as active-high since it is assumed that an LED to ground is used as the pull-down. 1 = The LED is set as active-low since it is assumed that an LED to VDD is used as the pull-up. Bit 0 is for LINKACTLED0 Bit 1 is for LINKACTLED1 Bit 2 is for LINKACTLED2 Bit 3 is for RUNLED/STATE_RUNLED Bit 4 is for ERRLED
CLK_25_EN	clk_25_en_strap	**Crystal Clock Output Enable Strap** This strap enables the CLK_25 pin as an output. 0 = disabled 1 = enabled
CLK_25_EN	xtal_input_mode_strap	**Crystal Clock Input Mode Strap** This strap selects between the operation of a crystal oscillator amplifier or a Schmitt trigger input. 0 = Oscillator mode 1 = Schmitt Input mode

SYSTEM CONTROL AND STATUS REGISTERS

The LAN9253 and LAN9254 devices provide EtherCAT® Direct Mapped mode. Table 3 details the direct mapped addresses for the system control and status registers.

TABLE 3: DIRECT MAP ADDRESSES FOR SYSTEM CONTROL AND STATUS REGISTERS

Address	EtherCAT® Direct Mapped Mode	Register Name
050h	3050h	Chip ID and Revision (ID_REV)
054h	3054h	Interrupt Configuration register (IRQ_CFG)
058h	3058h	Interrupt Status register (INT_STS)
05Ch	305Ch	Interrupt Enable register (INT_EN)
064h	3064h	Byte Order Test register (BYTE_TEST)
074h	3074h	Hardware Configuration register (HW_CFG)
084h	3084h	Power Management Control register (PMT_CTRL)
08Ch	308Ch	General Purpose Timer Configuration register (GPT_CFG)
090h	3090h	General Purpose Timer Count register (GPT_CNT)
09Ch	309Ch	Free Running 25 MHz Counter register (FREE_RUN)
1F8h	31F8h	Reset Control register (RESET_CTL)

REGISTER DIFFERENCES

This section shows the differences between the LAN9252 and LAN9253/LAN9254 registers. See Table 4 to Table 9.

TABLE 4: HARDWARE CONFIGURATION REGISTER (HW_CFG)

Bit	Description	
	LAN9252	LAN9253/LAN9254
26	RESERVED	**AMDIX Disable PHY B** When set, this bit disables the Auto-MDIX function and selects a non-crossed over configuration.
25	RESERVED	**AMDIX Disable PHY A** When set, this bit disables the Auto-MDIX function and selects a non-crossed over configuration.
24	RESERVED	**ANEG Disable PHY B** When set, this bit: • Sets the default mode of operation to fixed 100 Mbps, Full-Duplex • Modifies the MI Link Detection and Configuration operation (if enabled) to check for and enforce a fixed 100 Mbps Full-Duplex link • Modifies the Enhanced Link Detection operation (if enabled) to reset the PHY in case of errors instead of restarting auto-negotiation
23	RESERVED	**ANEG Disable PHY A** When set, this bit: • Sets the default mode of operation to fixed 100 Mbps, Full-Duplex. • Modifies the MI Link Detection and Configuration operation (if enabled) to check for and enforce a fixed 100 Mbps Full-Duplex link • Modifies the Enhanced Link Detection operation (if enabled) to reset the PHY in case of errors instead of restarting auto-negotiation

TABLE 4: HARDWARE CONFIGURATION REGISTER (HW_CFG) (CONTINUED)

Bit	Description	
	LAN9252	LAN9253/LAN9254
4:0	RESERVED	**LED Polarity** When cleared to 0, the associated LED pin is active-low. When set to 1, the associated LED pin is active-high. Bit 0 = LINKACTLED0 Bit 1 = LINKACTLED1 Bit 2 = LINKACTLED2 Bit 3 = RUNLED/STATE_RUNLED Bit 4 = ERRLED

TABLE 5: POWER MANAGEMENT CONTROL REGISTER (PMT_CTRL)

Bit	Description	
	LAN9252	LAN9253/LAN9254
9:7	RESERVED	**PME Pin Map (PME_PIN_SEL)** This field is used to map the PME signal to one of the various device pins. 000 = None 001 = ERRLED 010 = WAIT_ACK 011 = SYNC0/LATCH0 100 =SYNC1/LATCH1 101 = Reserved 110 = Reserved 111 = Reserved
6	RESERVED	**PME Buffer Type (PME_TYPE)** When this bit is cleared, the PME output pin functions as an open-drain buffer for a wired-or configuration. When set, the PME output pin is a push-pull driver. 0 = PME pin open-drain output 1 = PME pin push-pull driver
3	RESERVED	**PME Indication (PME_IND)** The PME signal can be configured as a pulsed output or a static signal, which is asserted upon detection of a wake-up event. When set, the PME signal will pulse active for 50 ms upon detection of a wake-up event. When cleared, the PME signal is driven continuously upon detection of a wake-up event. 0 = PME driven continuously on detection of event 1 = PME 50 ms pulse on detection of event The PME signal can be deactivated by clearing the above status bit(s) or by clearing the appropriate enable(s).
2	RESERVED	**PME Polarity (PME_POL)** This bit controls the polarity of the PME signal. When set, the PME output is an active-high signal. When cleared, it is active-low. 0 = PME active-low 1 = PME active-high

TABLE 5: POWER MANAGEMENT CONTROL REGISTER (PMT_CTRL) (CONTINUED)

Bit	Description	
	LAN9252	LAN9253/LAN9254
1	RESERVED	**PME Enable (PME_EN)** When set, this bit enables the external PME signal pin. When cleared, the external PME signal is disabled. 0 = PME pin disabled 1 = PME pin enabled

TABLE 6: ERR LED OVERRIDE REGISTER

Bit	Description
	LAN9253/LAN9254
7:5	RESERVED
4	**ERR Override** 0 = Override disabled 1 = Override enabled
3:0	**ERR LED Code** 0h = Off 1h-Ch = Flash 1x-12x Dh = Blinking Eh = Flickering Fh = On

Note 1: LAN9252 does not offer the ERR LED feature.

TABLE 7: PDI CONTROL REGISTER

Bit	Description	
	LAN9252	**LAN9253/LAN9254**
7:0	**Process Data Interface** 04h = Digital I/O 80h = SPI 88h = HBI Multiplexed 1 Phase 8-bit 89h = HBI Multiplexed 1 Phase 16-bit 8Ah = HBI Multiplexed 2 Phase 8-bit 8Bh = HBI Multiplexed 2 Phase 16-bit 8Ch = HBI Indexed 8-bit 8Dh = HBI Indexed 16-bit Others = RESERVED	**Process Data Interface (PDI_SELECT)** 04h = Digital I/O 05h = Beckhoff SPI 80h = SPI (LAN9252 Compatibility mode) 82h = SPI (EtherCAT® Direct Mapped mode) 88h = HBI Multiplexed 1 Phase 8-bit 89h = HBI Multiplexed 1 Phase 16-bit 8Ah = HBI Multiplexed 2 Phase 8-bit 8Bh = HBI Multiplexed 2 Phase 16-bit 8Ch = HBI Indexed 8-bit 8Dh = HBI Indexed 16-bit 90h = HBI Multiplexed 1 Phase 8-bit (EtherCAT Direct Mapped mode) 91h = HBI Multiplexed 1 Phase 16-bit (EtherCAT Direct Mapped mode) 92h = HBI Multiplexed 2 Phase 8-bit (EtherCAT Direct Mapped mode) 93h = HBI Multiplexed 2 Phase 16-bit (EtherCAT Direct Mapped mode) 94h = HBI Indexed 8-bit (EtherCAT Direct Mapped mode) 95h = HBI Indexed 16-bit (EtherCAT Direct Mapped mode) 8Eh: HBI Demultiplexed 8-bit 8Fh: HBI Demultiplexed 16-bit 96h: HBI Demultiplexed 8-bit (EtherCAT Direct Mapped Mode) 97h: HBI Demultiplexed 16-bit (EtherCAT Direct Mapped Mode) Others = RESERVED

TABLE 8: EXTENDED PDI CONFIGURATION REGISTER: DIGITAL I/O MODE

Bit	Description		
	LAN9252	LAN9253	LAN9254
15:8	RESERVED	RESERVED	**I/O Direction** 0 = Input 1 = Output

TABLE 9: PDI CONFIGURATION REGISTER: BECKHOFF SPI MODE

Bit	Description
	LAN9253/LAN9254
7:6	RESERVED
5	**Data Out Sample Mode** 0 = Normal sample (SPI_DO and SPI_DI are sampled at the same SPI_CLK edge) 1 = Late sample SPI_DO and SPI_DI are sampled at different SPI_CLK edges)
4	**SCS# Polarity** 0 = Active-low 1 = Active-high
3:2	RESERVED
1:0	**SPI Mode** 00 = SPI mode 0 01 = SPI mode 1 10 = SPI mode 2 11 = SPI mode 3

Note 1: LAN9252 does not offer the Beckhoff SPI mode feature.

100BASE-FX FIBER SUPPORT

LAN9252 supports 100BASE-FX via an external fiber transceiver. Pins 8, 9, and 10 in LAN9252 device are used for fiber port support. However, the LAN9253 and LAN9254 devices do not support the fiber port. These pins in LAN9253 and LAN9254 devices are strap configuration pins. Therefore, users need to connect these pins appropriately. The data sheet provides detailed information about the hardware strap configurations on these pins.

MOVING DESIGN FROM LAN9252 TO LAN9253 AND LAN9254

When moving from the LAN9252 to LAN9253 and LAN9254, the system design is mostly the same. Table 10 outlines new features and their implementation requirements for the LAN9253 and LAN9254 devices. Note that the table is not intended to replace the device data sheets. Refer to the data sheets for detailed description and implementation of these features.

TABLE 10: TRANSFERRING DESIGN FROM LAN9252 TO LAN9253/LAN9254

Item Number	Features	LAN9252	Implementation in LAN9253/LAN9254
1	EtherCAT Direct Mapped mode	Not supported	The EtherCAT Direct Mapped mode reduces overhead by mapping the EtherCAT CSR and Process Data RAM into the host memory space at the cost of slower bus access and timing requirements. The EtherCAT mode is configured via the Process Data Interface (PDI_SELECT) field in the PDI Control register. The device data sheets detail the implementation guidelines.
2	Crystal clock output pin	Not supported	The crystal clock may be output onto the dedicated CLK_25 pin for use as the reference clock to another device. This pin is enabled when the CLK_25_EN is high. In clock daisy chaining configuration with the CLK_25 of the previous devices as the input clock source, this pin should be set to Schmitt Trigger Input mode via the XTAL_MODE strap input.
3	EEPROM emulation	Not supported	These devices support EEPROM emulation to reduce EtherCAT system's cost and form factor. In this mode, the ESI file is saved on the attached MCU's non-volatile memory (NVRAM). The MCU performs the read and write to its NVRAM. In EEPROM Emulation mode, the ESC issues an interrupt to the microcontroller if an EEPROM command is pending, and it automatically sets the busy bit 0x0502[15]. While the busy bit is set, the microcontroller can read out the command and the EEPROM address. For a write access, write data are present in the data register. For a read command, read data have to be stored in the data register by the microcontroller. Once the microcontroller has finished reading/writing the EEPROM Data register, it acknowledges the command by writing to the EEPROM Command Register bits. The microcontroller has to write the command value it has executed into the EEPROM Command register. Errors can be indicated using two of the error bits. After acknowledging the command, the EEPROM busy bit 0x0502[15] is automatically cleared, and the interrupt is released. Select appropriate configuration straps as shown in Table 2.
4	ERROR LED	Not supported	The ERROR LED (ERRLED) is enabled by an enable bit in the ASIC Configuration register. Please visit the data sheet for the register definitions. The ERRLED pin on the LAN9252 functioned as the Fiber mode signal detect as well as the Port A FX-SD Enable. For copper twisted-pair operation, this pin would either be tied to or pulled down to ground. Since the ERRLED pin is enabled via an EEPROM bit, a special situation arises in the event of an EEPROM loading error. In this case, the ERRLED pin is forced enabled but only if the polarity (bit 4 of the LED Polarity field in the Hardware Configuration register (HW_CFG) indicates the ERRLED is active-low (implying that a high strap was loaded). The ERRLED Polarity field is controlled by the LEDPOL[4:0] configuration straps.

TABLE 10: TRANSFERRING DESIGN FROM LAN9252 TO LAN9253/LAN9254 (CONTINUED)

Item Number	Features	LAN9252	Implementation in LAN9253/LAN9254
5	BI-color state LED	Not supported	EtherCAT Technology Group (ETG) has allowed to use bi-color LED which includes red and green LEDs. In this arrangement, red is for error and green is for the RUN LED. Since the RUN part of the STATE LED must be turned off while the ERR part is active, the RUNLED and ERRLED pins cannot be simply combined to drive the bi-color LED. Instead, the RUNLED pin can be changed to a STATE_RUNLED pin, which is turned off while the ERRLED pin is on. STATE_RUNLED is selected via the STATE_RUNLED Mode Select bit of the ASIC Configuration register. The ASIC Configuration register is initialized from the contents of the EEPROM. Two, three and four pin bi-color LEDs are supported. A two-pin bi-color LED is supported by placing a pull-up or pull-down (depending on the signal polarity in use) on each side of the LED. A three-pin bi-color LED is supported by placing a series resistor to power or to ground (depending on the signal polarity in use). The choice between common anode or common cathode also depends on the signal polarity in use. For both two and three pin options, the polarity of STATE_RUN and ERR LEDs must be the same (or the use of an inverting transistor is required). A four-pin bi-color LED offers the most flexibility as each signal can have a different polarity if desired.
6	Beckhoff SPI	Not supported	The Beckhoff SPI interface is used as an alternate SPI interface. The value in the PDI Configuration register reflects the value from EEPROM. The value in the PDI Configuration register is used to configure the SPI. The value in the Extended PDI Configuration register is used if GPIOs are enabled (SPI w/GPIO). The PDI Configuration register and Extended PDI Configuration register are initialized from the contents of the EEPROM.
7	HBI Interface - Direct Mapped mode	Not supported	EtherCAT Direct Mapped mode requires additional pins. However, with some modifications, EtherCAT Direct Mapped mode can be used for PCBs designed for the LAN9252. WAIT_ACK: The WAIT_ACK pin on the LAN9252 functions as the Fiber mode signal detect as well as the Port B FXSD Enable. For copper twisted-pair operation, this pin would either be tied to or pulled down to ground. WAIT_ACK is disabled by default to avoid a short. Without the WAIT_ACK connected to the host processor, the host bus cycles must assume worst-case cycle timing. BE1/BE0: When in 16-bit data width mode, the byte enables are required to select which byte or bytes are written or read from the EtherCAT core. In Multiplexed mode, these pins on the LAN9252 are unused and not driven. The BE1/BE0 pins have internal pull-downs such that if left undriven, they would assume an Active state, This allows 16-bit only access to the device. Caution is required to not overwrite the adjacent byte when only BYTE access is desired.
8	HBI Demultiplexed mode	Not supported	This implementation provides a demultiplexed address and data bus with the address and endianness select inputs directly provided by the host. Two back-to-back 16-bit data cycles or 4 back-to-back 8-bit data cycles are required within the same 32-bit DWORD. Table 7 shows the PDI control registers to select HBI Demultiplexed registers.
9	Fiber port connection	Pin 8,9, and10	Not supported. These pins in LAN9253 and LAN9254 devices are strap configuration pins. Therefore, users need to connect these pins appropriately. The data sheet provides detailed information about the hardware strap configurations on these pins.

TABLE 10: TRANSFERRING DESIGN FROM LAN9252 TO LAN9253/LAN9254 (CONTINUED)

Item Number	Features	LAN9252	Implementation in LAN9253/LAN9254
10	Fiber port connection	Pin 9	Not supported. These pins in LAN9253 and LAN9254 devices are strap configuration pins. Therefore, users need to connect these pins appropriately. The data sheet provides detailed information about the hardware strap configurations on these pins. If ERROR LED function is used on this pin, please refer to ERROR LED feature #4 in this table.
11	Fiber port connection	Pin 10	LAN9253 and LAN9254 do not support fiber. If WAIT_ACK function is used a test pin can be added on this pin.

NOTES:

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003621A (09-09-20)	Initial release.	

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