

LF Antenna Driver ATA5279C – Thermal Considerations and PCB Design Suggestions

ATA5279C

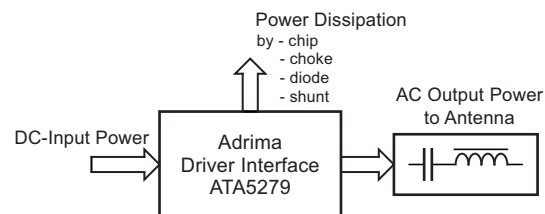
General

To minimize EMC radiation the Atmel® ATA5279C is designed to drive antennas with a sinusoidal waveform. For the same reason the switching edges of the integrated boost transistor are degenerated. The EMC benefit thus results in higher power dissipation and a corresponding increase in the on-chip temperature.

Power Balancing at the Driver Interface

The total power loss on the chip primarily results from the activated driver stage in addition to the internal boost transistor. In the worst case the highest power dissipation occurs when the supply voltage ($V_S = 8V$) is low and a high antenna impedance is driven by the maximum antenna current (1Ap).

Figure 1. Power Balancing of the Driver Interface



In spite of the power dissipation the thermal load can be controlled for typical automotive PEG applications because the device is activated on demand and operates for a short time only.

In addition, a temperature sensor monitoring protects the device from becoming damaged in the event of an unusual operation scenario.

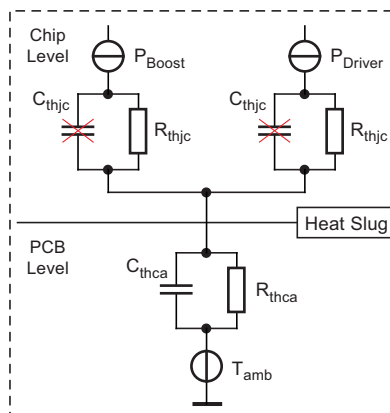
Nevertheless, the design of hardware and software has to ensure that a thermal shutdown during normal operation never occurs. But in case of an abnormality as well, a cyclic over-temperature shutdown should be avoided to ensure the device achieve maximum longevity.

Thus, the designer wants to know in advance the resulting chip temperature with respect to his specific application conditions. This is important for estimating the margin to thermal shutdown when sending the specific LF protocol.

1. Thermal Model of the Device Mounted on PCB

Even though the Atmel® ATA5279C is a device for short-term power operation, it has to take in account both the local peak temperature on the silicon area as well the average temperature of the case. A thermal model has been created for the purpose of calculating or simulating on-chip thermal behavior.

Figure 1-1. Simplified Thermal Model



The power dissipation sources P_{Boost} and P_{Driver} are located on different chip areas. Each source is connected to an individual thermal resistance R_{thjc} with identical value to derive the heat down to the slug level. For the sake of simplicity the thermal capacity C_{thjc} can be ignored because the resulting time constant (4ms) has only a minor impact compared to that of the device package. The combined power dissipation $P_{Boost} + P_{Driver}$ passes R_{thca} and is then absorbed by the PCB. Thus, the final heat slug temperature is determined by the total power dissipation multiplied by the thermal resistance R_{thca} and the operation duty cycle n_{duty} plus the ambient temperature T_{amb} .

How to simulate or calculate the chip temperature according to the thermal model of [Figure 1-1](#) is described in a section below.

1.1 Power Dissipation on Chip Depending on Operating Conditions

Power dissipation values shown in the tables below are determined by simulation under various operating conditions based on chip design parameters. The tables demonstrate the dissipation for operating the high-power driver stages of the device. For the selected driver stage AxP it has to be taken into account that power loss is also generated even when sending LF "0" data or remaining in idle mode. This is due to the cross current of the driver stage. The dissipation results from the driver voltage V_{DS} multiplied by the driver cross current $I_{AxP,CC}$. However, if sending LF "0" data, V_{DS} is defined by regulation, whereas in idle mode V_{DS} is fixed to $V_S = 12V$, the result is $I_{AxP,CC} = 68mA$ or about 0.8W.

Table 1-1. Boost Power Dissipation at $V_S = 12V$

Boost Dissipation [W] at $V_S = 12V$ Carrier On, RC Snubber ⁽¹⁾			
Antenna Current [mA _p]	Antenna Impedance [Ω]		
	12.5	15	17
500	0.26	0.36	0.46
600	0.46	0.66	0.86
700	0.77	1.14	1.53
800	1.25	1.89	2.55
900	1.97	3.01	4.70
1000	2.99	5.01	4.44

Note: 1. Additional RC snubber circuitry through a diode for EMC suppression leads to increased power dissipation

Table 1-2. Boost Power Dissipation at $V_S = 9V$

Boost Dissipation [W] at $V_S = 8.25V$ Carrier On, RC Snubber ⁽¹⁾			
Antenna Current [mA _p]	Antenna Impedance [Ω]		
	12.5	15	17
500	0.45	0.65	0.84
600	0.85	1.24	1.64
700	1.50	2.26	3.08
800	2.55	4.04	6.20
900	4.33	6.28	6.65
1000	5.98	6.36	6.54

Note: 1. Additional RC snubber circuitry through a diode for EMC suppression leads to increased power dissipation

Table 1-3. Driver Power Dissipation

Boost Dissipation [W] at Carrier ON			
Antenna Current [mA _p]	Antenna Impedance [Ω]		
	12.5	15	17
500	1.79	1.82	1.89
600	2.23	2.35	2.45
700	2.78	2.94	3.08
800	3.37	3.59	3.76
900	4.01	4.29	4.51
1000	4.71	5.05	5.32

Table 1-4. Driver Power Dissipation Sending LF “0” Data

Boost Dissipation [W] at Carrier Off Sending LF “0” Data			
Antenna Current [mA _p] Sent Before	Antenna Impedance [Ω]		
	12.5	15	17
500	1.46	1.63	1.77
600	1.66	1.86	2.03
700	1.86	2.09	2.28
800	2.05	2.33	2.54
900	2.25	2.56	2.80
1000	2.45	2.79	3.06

Graphical Performance of power dissipation given by [Table 1-1 on page 2](#) to [Table 1-4](#):

Figure 1-2. Boost Dissipation at Continuous Carrier, $V_S = 12V$

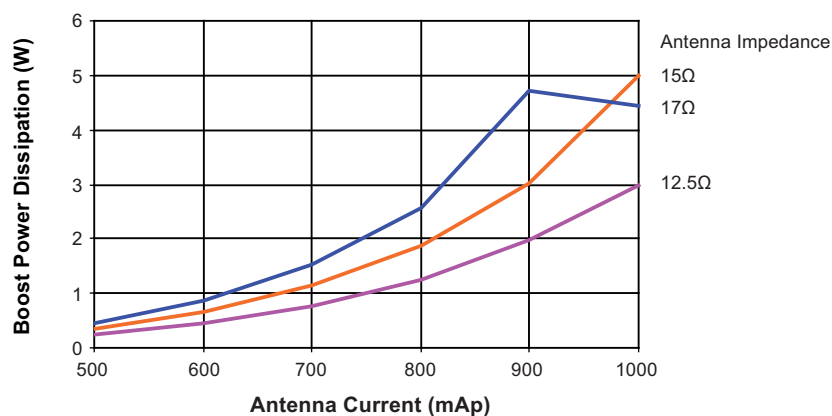


Figure 1-3. Boost Dissipation at Continuous Carrier, $V_S = 8.25V$

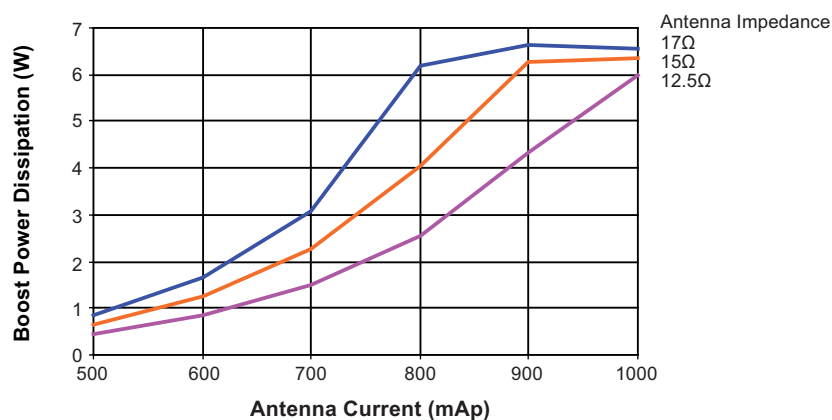


Figure 1-4. Driver Dissipation at Continuous Carrier

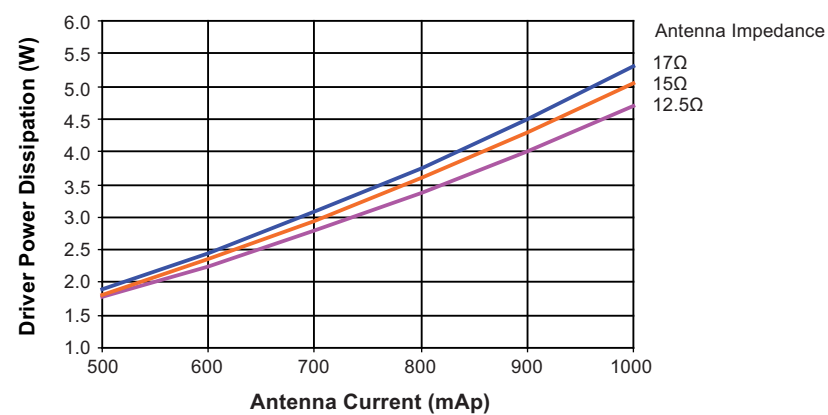
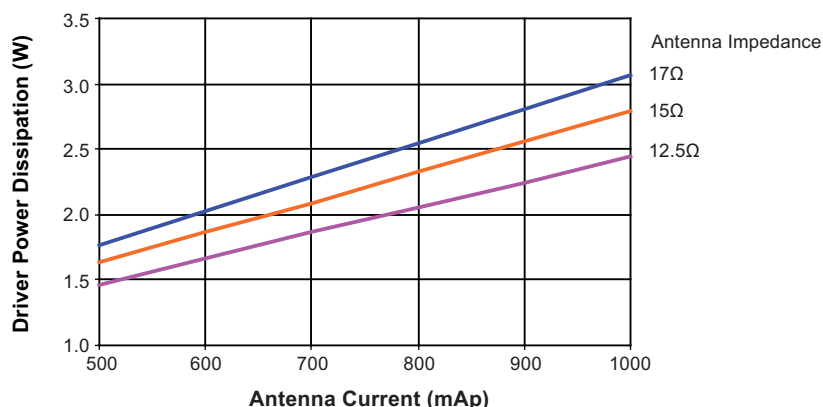


Figure 1-5. Driver Dissipation Sending LF “0” Data



Note: The power limitation and reduction of the boost converter power dissipation in [Figure 1-2 on page 4](#) is caused by reaching the overvoltage switch-off threshold due to high antenna impedance (17Ω). However, at low voltage operation ($V_S = 8.25V$) [Figure 1-3 on page 4](#) the boost converter reaches the current limitation if a 15Ω or 17Ω antenna is in use.

1.2 Thermal Parameters of Device and PCB

The junction-case thermal resistance of device is specified by the data sheet with $R_{thjc} = 10k/W$. Whereas, the thermal capacity C_{Thjc} can be ignored because the related time constant of about 4ms is minor compared to that of a typical PCB.

More effort is required to determine the thermal parameters for the specific PCB. [Section 4. “Appendix” on page 11](#) describes how it is measured by using the Atmel® ATAB5279 application board.

As a frame of reference, thermal parameters for this board were measured as follows:

- Thermal resistance $R_{thca} = 34K/W$
- Thermal time constant $\tau_{hca} = 12.5s$

These values can be used as a guideline reference in advance for thermal simulations. But it can be assumed that no significant lower thermal resistance will be reached based on this target board design.

2. Calculation of Temperature Rise Based on Equation

The equations of the chip temperature calculation below are derived from the simplified thermal model as shown in [Figure 1-1 on page 2](#).

$$T_{\text{Heatslug}}(t) = T_{\text{amb}} + n_{\text{duty}} \times R_{\text{thca}} \times (P_{\text{Boost}} + P_{\text{Driver}}) \times \left(1 - e^{-\frac{t}{\tau_{\text{ca}}}}\right) \quad \text{Equation 1}$$

$$T_{\text{Boost}}(t) = P_{\text{Boost}} + R_{\text{thjc}} + T_{\text{Heatslug}}(t) \quad \text{Equation 2}$$

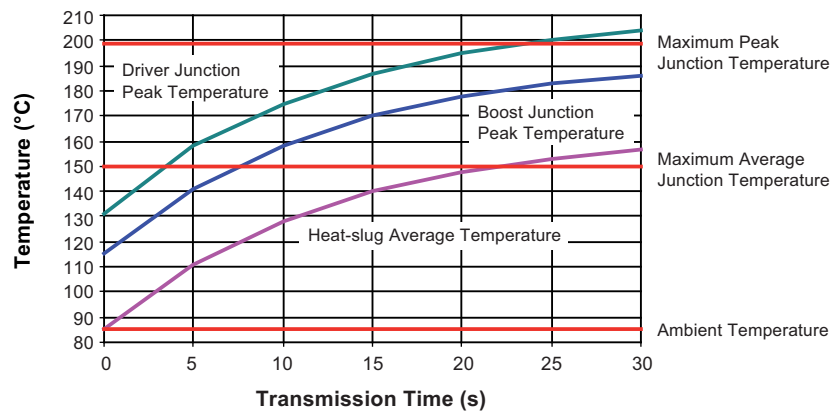
$$T_{\text{Driver}}(t) = P_{\text{Driver}} + R_{\text{thjc}} + T_{\text{Heatslug}}(t) \quad \text{Equation 3}$$

By means of equations 1-3, the local temperature rise on chip can be calculated in a separate manner for boost and driver area on-chip as well for the average heat-slug temperature. To calculate the average temperature on the heat-slug an operation duty cycle n_{duty} has to be assumed.

The example below shows the resulting temperature profile using the application board with antenna operated at 12V supply voltage and maximum antenna current of 1A_p.

P_{Boost}	= 2.99W	Power dissipation of boost transistor (from Table 1-1 on page 2)
P_{Driver}	= 4.71W	Power dissipation of driver stage (from Table 1-2 on page 3)
T_{amb}	= 85°C	Ambient temperature
R_{thjc}	= 10K/W	Thermal resistance junction case of device
R_{thca}	= 34K/W	Thermal resistance case-to-ambient (PCB)
τ_{ca}	= 12.5s	Thermal time constant of PCB ($R_{\text{thca}} \times C_{\text{thca}}$)
n_{duty}	= 0.30	Operation duty cycle
t		Time of transmission

Figure 2-1. Calculated Temperature Profile on Chip



Using a formula to calculate the temperature rise has the disadvantage that an average operation duty cycle has to be assumed. The calculation method cannot perform a real temperature profile modulated by sent LF data pattern. [Section 3. "Simulation of Temperature Rise Based on Thermal Model" on page 7](#) describes how a thermal simulation can be performed using a standard PSPICE simulation tool.

3. Simulation of Temperature Rise Based on Thermal Model

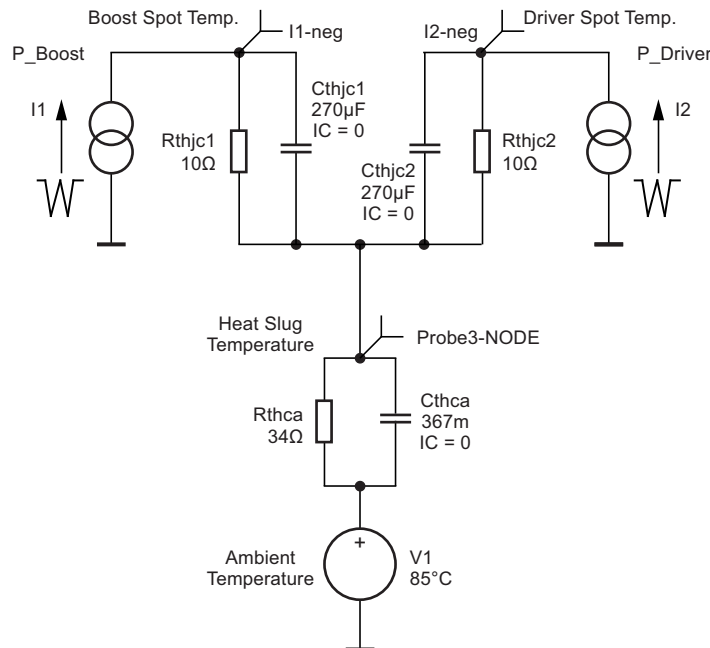
Due to the analogy between thermal and electrical behavior the temperature transients can be simulated by means of a standard PSPICE tool available on the market. In comparison to the calculation method in [Section 2. “Calculation of Temperature Rise Based on Equation” on page 6](#), it offers the advantage that the real temperature profile can be visualized depending on power dissipation of the sent LF pattern.

In analogy parameters can be transferred for simulation as follows:

Power Dissipation	P [W]	>>>	Current Source	I [A]
Ambient Temperature	9 [°C]	>>>	Voltage Source	V [V]
Thermal Resistance	R _{th} [K/W]	>>>	Resistor	R [Ω]
Thermal Capacitance	C _{th} [Ws/K]	>>>	Capacitor	C [F]

In accordance with the thermal model in [Figure 1-1 on page 2](#) and the analogy to the electrical parameters a related schematic entry for simulation is carried out in [Figure 3-1](#).

Figure 3-1. Schematic Entry for PSPIC



For the simulation example the thermal parameter and power dissipation values are taken from the calculation example in [Section 2. “Calculation of Temperature Rise Based on Equation” on page 6](#).

The thermal capacities are derived from the known time constant and thermal resistance according formula:

$$C_{thjc1} = C_{thjc2} = \frac{\tau_{thjc}}{R_{thjc}} = \frac{4ms}{10\frac{K}{W}} = 4 \times 10^{-4} \frac{Ws}{K} \gggg 400\mu F$$

$$C_{thca} = \frac{\tau_{thca}}{R_{thca}} = \frac{12.5s}{34\frac{K}{W}} = 0.367 \frac{Ws}{K} \gggg 367mF$$

For the specific application the on-chip temperature profile is modulated by the sent LF pattern. In the schematic entry in [Figure 3-1](#) the P_Boost and P-Driver power dissipation are represented by the PWL current sources I1 and I2. The modulating on/off time sequence with related power dissipation values are entered separately from the menu for the I1 and I2 sources.

Note: When sending LF “0” data, due to the cross current the driver stage generates power dissipation in any case. It is accounted for with 2.45W in the entry box in [Figure 3-3 on page 8](#) taken from [Table 1-4 on page 3](#).

Figure 3-2 and Figure 3-3 on page 8 show the entry boxes for I1/I2 current sources of the simulation example. Therefore data pattern are converted in a continuous time sequence based on which the boost and driver power dissipation are modulated in on/off mode. In the example, “Time” is entered in seconds and “Current” in watts.

Figure 3-2. Entry Box for I1 Current (Power) Sequence

	Time	Current
1	0.0021280	2.7
2	0.0021281	0
3	0.0022560	0
4	0.0022561	2.7
5	0.0023840	2.7
6	0.0023841	0
7	0.0025120	0
8	0.0025121	2.7
9	0.0026400	2.7

"Insert" inserts a row or rows
 "Delete" deletes selected rows

Ok Paste Cancel

Figure 3-3. Entry Box for I2 Current (Power) Sequence

	Time	Current
1	0.0020000	4.7
2	0.0021280	4.7
3	0.0021281	2.45
4	0.0022560	2.45
5	0.0022561	4.7
6	0.0023840	4.7
7	0.0023841	2.45
8	0.0025120	2.45
9	0.0025121	4.7

"Insert" inserts a row or rows
 "Delete" deletes selected rows

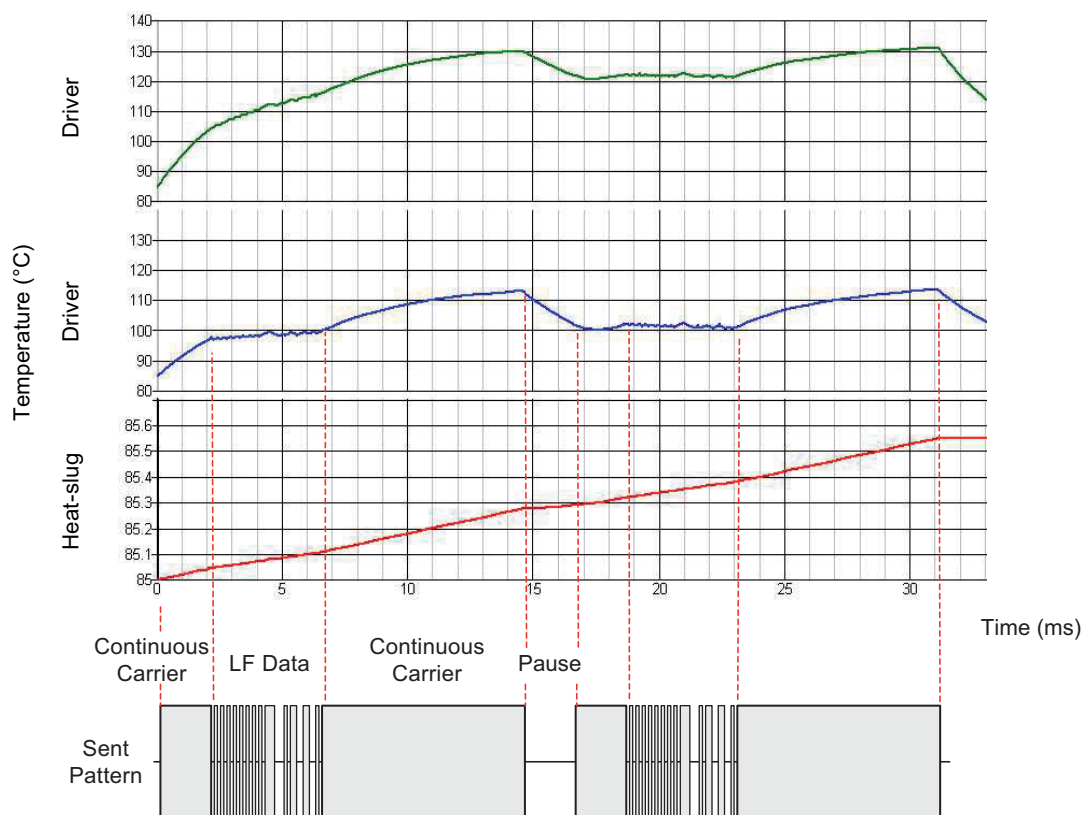
Ok Paste Cancel

This tool limits the number of time steps which can be entered to 256. So if a data pattern would be entered on bit level (bit width of 128µs), the protocol length is limited to $256 \times 128\mu s = 32.768ms$. In this example data is entered at the bit level because only 32bits are used. In order to reduce the step numbers, longer terms of changing data bits can be summarized to a time duration defining an average of power dissipation corresponding to the logical bit structure. Thus only two time steps are required to indicate the beginning and end of a power dissipation phase. To generate a continuous time sequence an Excel calculation according to the list in Figure 3-4 may be helpful.

Figure 3-4. Generation of Bit Time Sequence Using Excel Lists

Time Settings		Timing	Power Dissipation		Bit No.	
			Boost	Driver		
Start Time [s]	0,002	0,0020000	2,7	4,71	Bit 1	Byte 1
Step Time [s]	0,000128	0,0021280	2,7	4,71		
Rise Time [s]	0,0000001	0,0021281	0	2,45	Bit 2	
		0,0022560	0	2,45		
		0,0022561	2,7	4,71	Bit 3	
		0,0023840	2,7	4,71		
		0,0023841	0	2,45	Bit 4	
		0,0025120	0	2,45		
		0,0025121	2,7	4,71	Bit 5	
		0,0026400	2,7	4,71		

Figure 3-5. Temperature Profile on Chip and PCB Depending Power Dissipation and Sent Pattern



3.1 Simulation Result

The simulated profile in [Figure 3-5](#) indicates the fast local temperature rise on driver stage and boost transistor due to the low thermal capacity (time constant ($\tau_{ca} = 4\text{ms}$)). In contrast the heat-slug temperature rises much more slowly because the capacity of the PCB is larger (time constant $\tau_{ca} = 12.5\text{s}$).

Under the mentioned operating conditions in combination with the example protocol pattern, the device stays in safe operation because the maximum driver temperature is 25 degrees below the maximal allowed junction temperature of 150°C . Of course, if such a LF pattern was sent in repeat mode, the average temperature on the heat-slug would increase further. In this case, a thermal shutdown happens if the threshold level (typical 145°C) is exceeded.

Under “listed condition” in [Figure 3-6](#) and [Figure 3-7](#) the scenario depicts how long the driver could be activated in continuous mode till the thermal shutdown terminates operation.

Operating conditions:

P_{Boost}	= 2.99W	Power dissipation of boost transistor at $V_S = 12\text{V}$
P_{Driver}	= 4.71W	Power dissipation of driver stage at $V_S = 12\text{V}$, active
P_{Driver}	= 2.45W	Power dissipation of driver stage at $V_S = 12\text{V}$, send LF “0” data
T_{amb}	= 85°C	Ambient temperature
R_{thjc}	= 10K/W	Thermal resistance junction case of device
R_{thca}	= 34K/W	Thermal resistance case-to-ambient (PCB)
τ_{ca}	= 125s	Thermal time constant of PCB ($R_{\text{thca}} \times C_{\text{thca}}$)

Figure 3-6. Temperature Profile of Chip and PCB with Continuous Power Dissipation

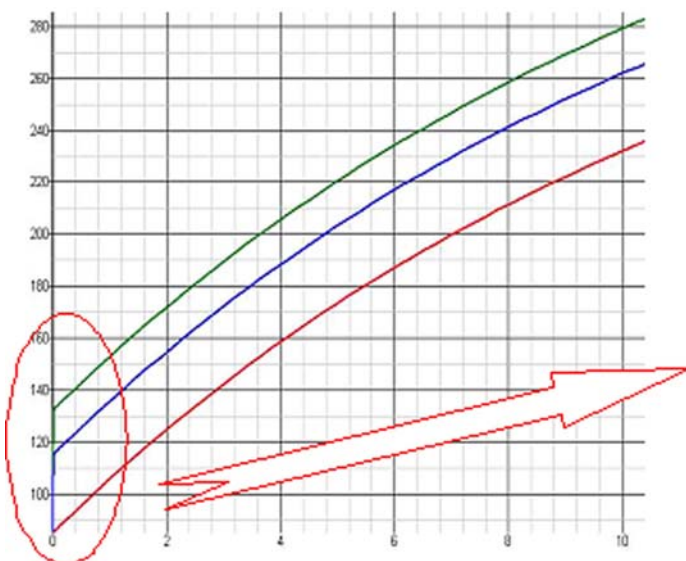
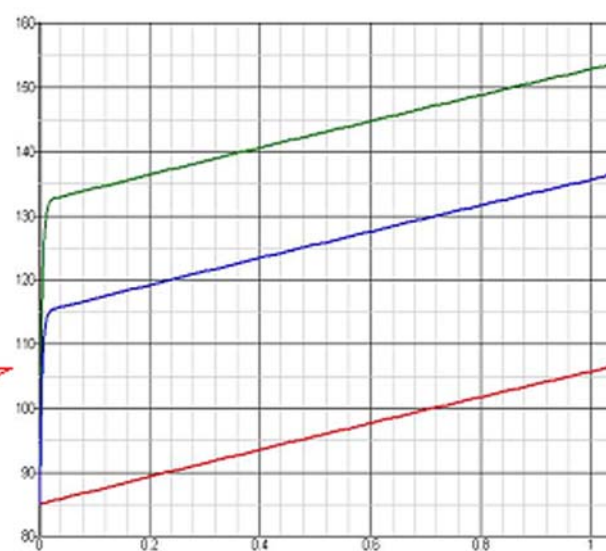


Figure 3-7. Close-up View of [Figure 3-6](#)



4. Appendix

4.1 How to Determine the Thermal Parameters of the PCB

A key aspect of the thermal resistance is the thermal connection from the heat slug underneath the package (QFN44) soldered to the assembly copper plate and the heat sink through vias to the copper plate on the rear. Therefore, it is difficult to calculate in advance the size needed for the copper plate to achieve a given thermal resistance. The copper back plate of this board establishes the electrical ground and also serves as a heat sink. Its dimension is almost equivalent to the board size (80mm×65mm). The thermal transportation through the board is achieved by 8 vias with a diameter of 0.3mm as shown in Figure 4-2.

Figure 4-1. Assembly of Application Board ATAB5279

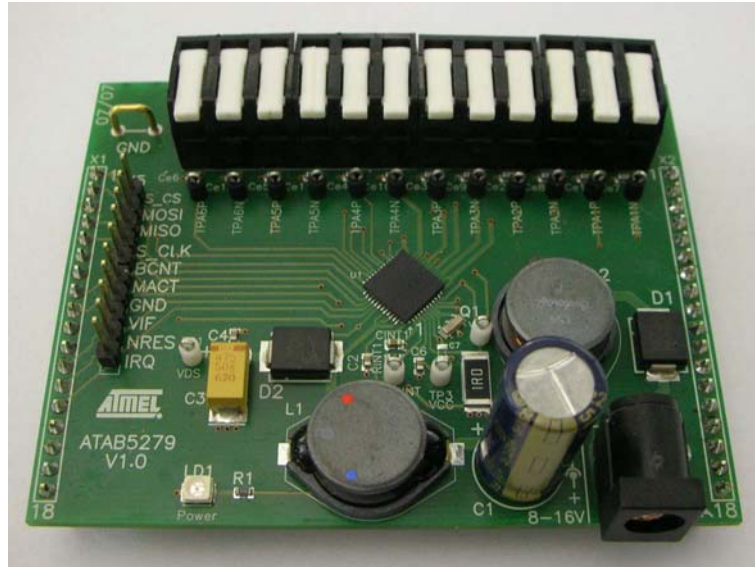
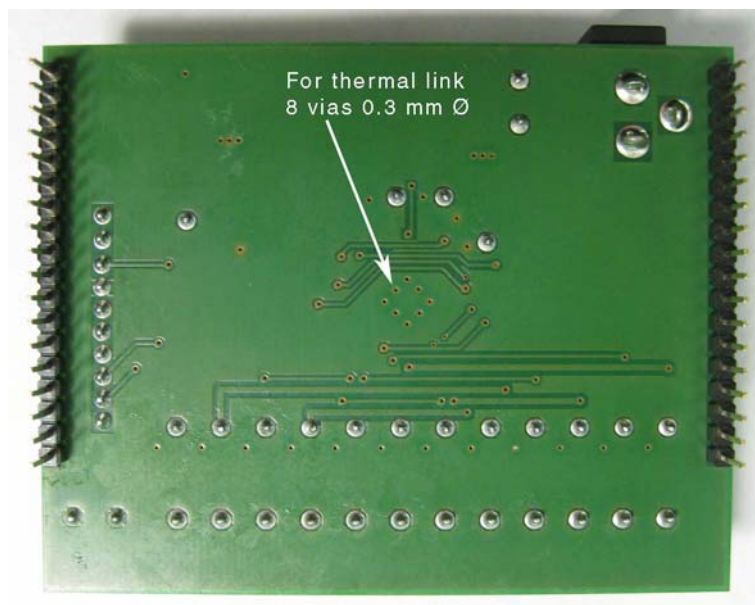


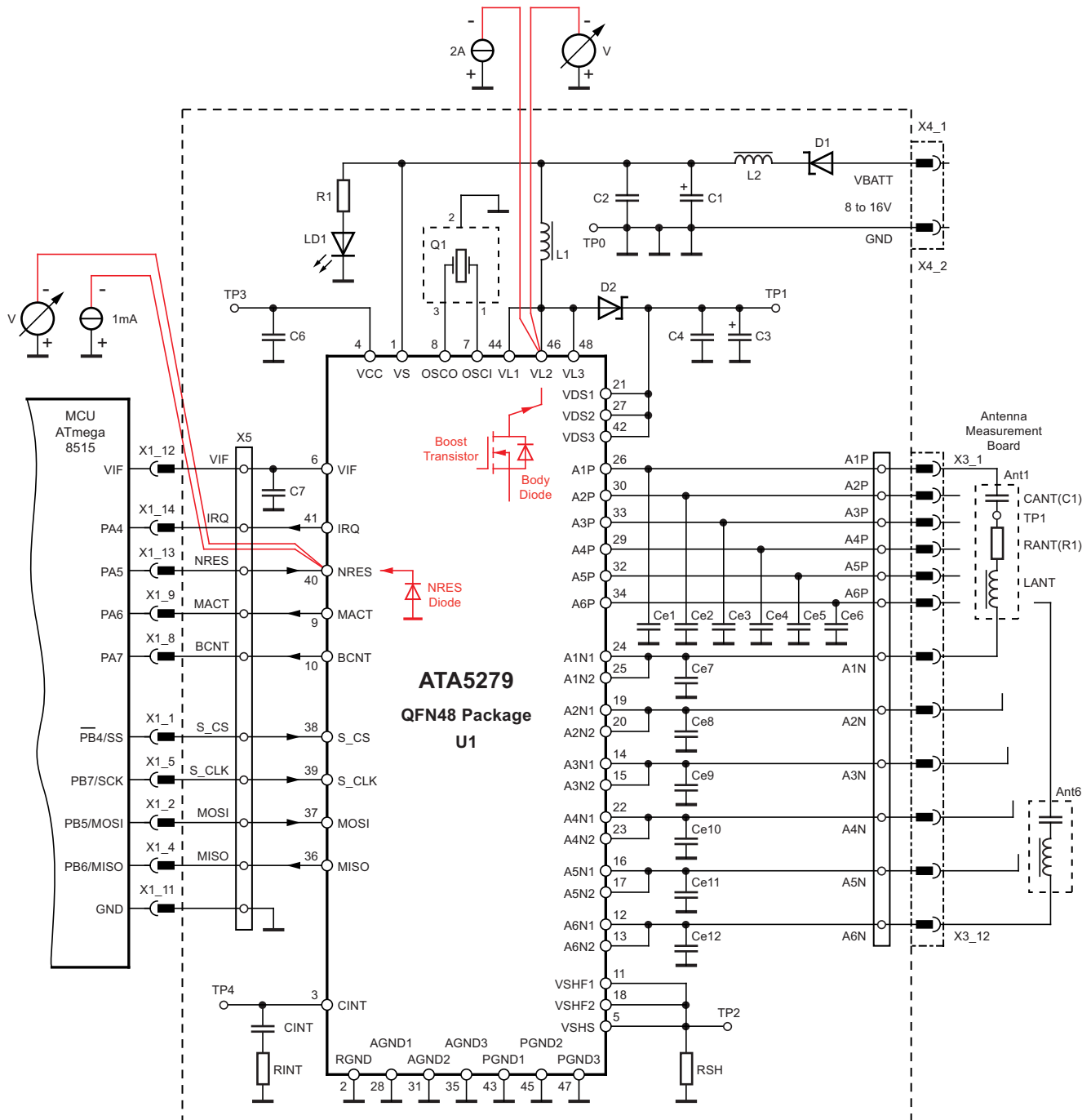
Figure 4-2. Heat Sink Ground Connection Plan of the ATAB5279



4.2 Arrangement for Measuring the Thermal Parameters on PCB

To define the thermal resistance R_{thja} of the PCB the ESD protection diode at the “NRES” pin is used for temperature detection within the chip. The diode is therefore powered by a DC constant current of 1mA and the resulting voltage drop over temperature is measured. The chip on board is heated by powering the boost transistor body diode by a constant DC current of 2A fed into the “VL” pin. The resulting voltage drop at the body diode detected at the VL pin indicates the dissipated power. The force/sense principle has to be used to obtain accurate measurements.

Figure 4-3. Thermal Resistance Measurement on the ATAB5279 Application Board



4.3 How to Determine the Thermal Resistance R_{thca} on a PCB

When heating up the chip in combination with the board using the boost transistor's body diode, the resulting on-chip temperature can be measured via V_F of the NRES diode. The board is thus operated at a constant ambient temperature of 20°C using a climate chamber.

However, it must be taken into account that the NRES diode is located at the edge of the chip close to the pin. This means the measured temperature is that of the case rather than of the chip. As a result, the thermal resistance determined here indicates the value of case to ambient (R_{thca}).

The power dissipation on the body diode is given by:

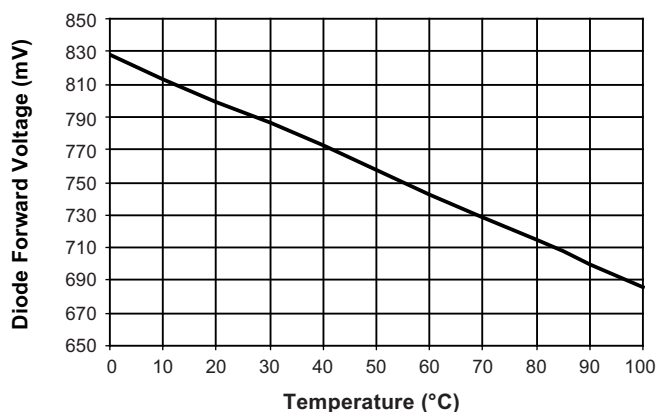
$$(1) \quad \begin{aligned} P_{DissB} &= V_{FB} \times I_{FB} & P_{DissB} & \text{Power dissipation of body diode} \\ P_{DissB} &= 965\text{mV} \times 2\text{A} = 1.93\text{W} & V_{FB} & \text{Forward voltage of body diode} \\ & & I_{FB} & \text{Forward current of body diode} \end{aligned}$$

To calibrate the NRES reference diode the board is exposed to a temperature-controlled chamber recording V_F (NRES) over temperature.

Table 4-1. Temperature Dependency of NRES Diode Forward Voltage

Temperature [°C]	V_F (NRES Diode) at 1mA [mV]
0	828
10	813
20	799
30	786
40	772
50	757
60	743
70	729
80	715
90	700
100	686

Figure 4-4. Temperature Dependency of Diode Voltage



Using the measurements in [Table 4-1 on page 13](#) the temperature coefficient of the NRES reference diode is calculated as follows:

$$(2) \quad TC(NRES) = \frac{(828 - 686)mV}{100K} = 1.42 \frac{mV}{K}$$

The resulting temperature coefficient TC(NRES) and the actual measured diode voltage are used to calculate the NRES diode temperature.

$$(3) \quad \Delta T_X = \frac{1}{TC} (V_{D0} - V_{DX})$$

$$\Delta T_X = \frac{1}{1.42 \times \frac{mV}{K}} (799 - 707)mV = 64.78K$$

ΔT_X	Actual temperature rise
T_0	Initial temperature
V_{D0}	Diode voltage at initial temperature T_0
V_{DX}	Diode voltage at actual temperature T_X

Using the on-chip power dissipation from equation (1) and the delta temperature rise equation (3) the entire thermal resistance of the board including the IC can be calculated according to equation (4).

$$(4) \quad R_{thja} = \frac{\Delta T_X}{P_{Bdiss}} = \frac{64.78K}{1.93W} = 33.56 \frac{K}{W}$$

4.4 How to Measure the Thermal Time Constant as well as PCB Capacity

Using the arrangement shown in [Figure 4-3 on page 12](#) the chip temperature increase is recorded while the body diode of the boost transistor is heated up. To this end, the DSO oscilloscope measures the forward voltage VF of the NRES diode over time and creates a set of values that can be imported into an Excel spreadsheet. [Figure 4-5](#) and [Figure 4-6](#) show these measurements over time for both chip temperature increase and decrease.

Figure 4-5. Increase of Chip Temperature

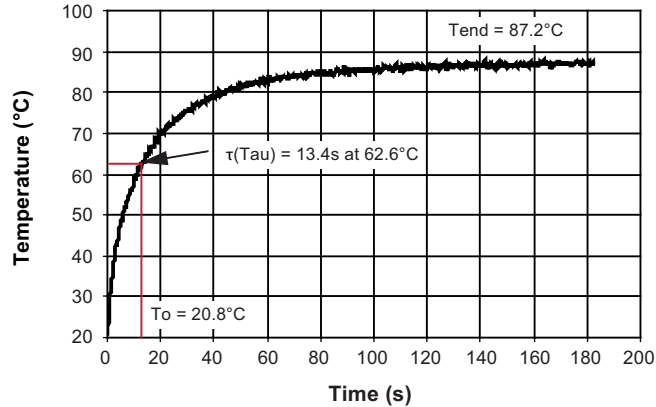
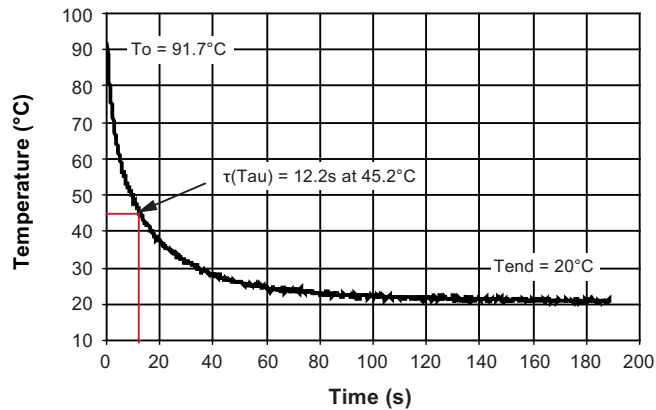


Figure 4-6. Decrease of Chip Temperature



According to the physical rules, Tau ($\tau = R_{thjca} \times C_{thjca}$) is defined to be 63% of the final value of an exponential function. Since the board and device do have different thermal capacities, the exponential function is not ideal in the first ms range. From a long-term perspective, however, this can be disregarded. In addition, the difference in the resulting τ -values (see [Figure 4-5](#) and [Figure 4-6](#)) is due to measurement inaccuracy. Theoretically it should be the same in both cases.

5. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9168D-RKE-05/15	• Put document in the latest template

