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Component Placement Checklist for the LAN8820, 56-pin QFN Package

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Component Placement Checklist for LAN8820

Information Particular for the 56-pin QFN Package

LAN8820 QFN Phy Interface:

1. Place the 49.9 Ω termination pull-up (TR0P, pin 44) as close to the LAN8820 as possible.
2. Place the 49.9 Ω termination pull-up (TR0N, pin 43) as close to the LAN8820 as possible.
3. Place the 49.9 Ω termination pull-up (TR1P, pin 47) as close to the LAN8820 as possible.
4. Place the 49.9 Ω termination pull-up (TR1N, pin 46) as close to the LAN8820 as possible.
5. Place the 49.9 Ω termination pull-up (TR2P, pin 52) as close to the LAN8820 as possible.
6. Place the 49.9 Ω termination pull-up (TR2N, pin 51) as close to the LAN8820 as possible.
7. Place the 49.9 Ω termination pull-up (TR3P, pin 55) as close to the LAN8820 as possible.
8. Place the 49.9 Ω termination pull-up (TR3N, pin 54) as close to the LAN8820 as possible.
9. All the components discussed in this section should be considered critical components. To ensure the best signal integrity and good EMI performance, these critical components should be placed on the component side of the PCB. This will ensure that these components will be referenced to a contiguous ground plane reference on Layer 2 of the design.

LAN8820 QFN Magnetics:

1. Place the 0.022 μF Center Tap termination capacitors as close to the magnetics as possible. This capacitor should be considered a critical component. To ensure the best signal integrity and good EMI performance, this critical component should be placed on the component side of the PCB. This will ensure that this component will be referenced to a contiguous ground plane reference on Layer 2 of the design.
2. Place the four 75 Ω cable side center tap termination resistors and the 1000 ρF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible. These components may be considered non-critical components. These components make up part of the high voltage barrier for the Ethernet front end. The best location for these components is typically on the solder side of the PCB. They should be placed such that none of the resultant routing crosses the differential pairs. These components have both ESD and EMI implications.

RJ45 Connector:

1. Place the RJ45 connector, the magnetics and the LAN8820 QFN as close together as possible.

2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN8820 QFN.

3. The distance from the RJ45 connector to the magnetics should be 0.50” at a minimum and 0.75” at a maximum.

4. The distance from the magnetics to the LAN8820 should be 1.0” at a minimum and 3.0” at a maximum.

5. Select and place the magnetics as to set up the best routing scheme from the LAN8820 QFN to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.

6. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.

VDD25IO Power Supply Connections:

1. Place the (4) VDD25IO decoupling capacitors for the LAN8820 QFN as close to the power pin as possible. Using an SMD_0402 package will make this task easier.

2. Decoupling capacitors, in general, are best placed on the component side of the PCB. This should allow the board designer to minimize the use of vias and provide a short, direct copper connection from the capacitor to the power pin.

+1.2V Power Supply Connections:

1. Place the (6) VDD12CORE decoupling capacitors for the LAN8820 QFN as close to the power pin as possible. Using an SMD_0402 package will make this task easier.

2. Place the (4) VDD12A decoupling capacitors for the LAN8820 QFN as close to the power pin as possible. Using an SMD_0402 package will make this task easier.

3. Place the single VDD12BIAS decoupling capacitor for the LAN8820 QFN as close to the power pin as possible. Using an SMD_0402 package will make this task easier.

4. Place the single VDD12PLL decoupling capacitors for the LAN8820 QFN as close to the power pin as possible. Using an SMD_0402 package will make this task easier.

5. Decoupling capacitors, in general, are best placed on the component side of the PCB. This should allow the board designer to minimize the use of vias and provide a short, direct copper connection from the capacitor to the power pin.

Ground Connections:

1. There are no component placement issues associated with the LAN8820 QFN ground connections. The LAN8820 has an Exposed Die Paddle ground connection on the package bottom. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

Crystal Connections:

1. Place the 25.000 MHz crystal and the associated 27 – 33 ρF capacitors as close together as possible and as close to the LAN8820 QFN (XI, pin 5 & XO, pin 6) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.).

2. The crystal and associated components should be located within 0.25” of the LAN8820.

3. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all crystal components are referenced to the same reference plane.

ETHRBIAS Resistor:

1. Place the ETHRBIAS resistor as close to pin 42 of the LAN8820 QFN as possible.

2. The RBIAS resistor should be considered a critical component. This critical component should be placed on the component side of the PCB. This will ensure that this component will be referenced to a contiguous ground plane reference on Layer 2 of the design.

Required External Pull-ups/Pull-downs:

1. Typically, there are no component placement issues associated with the LAN8820 QFN External Pull-up connections.

RGMII Interface:

1. When physically placing the LAN8820 in an RGMII application, the designer should be aware of the relative trace lengths determined by the relationship of the Phy and the MAC in the application. By placing the MAC too far away from the LAN8820, this may result in operational problems associated with excessive trace lengths.

2. The designer has some latitude in the placement of the LAN8820 with respect to the magnetics. This should allow for some adjustment on the Phy-to-MAC RGMII interface, should this be necessary. By moving the Phy farther away from the magnetics, the MII interface can be shortened.

3. SMSC recommends the final RGMII interface trace lengths to remain under 6” long.

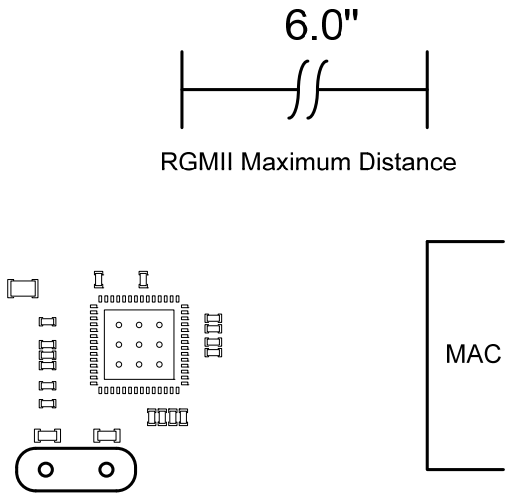

Figure No. 1

RGMII Series Terminations:

1. If the designer has elected to use impedance matching terminations in his design, these series resistors should be placed as close as possible to the source of the driving signal.

2. The RGMII Series Terminations should be considered critical components. To ensure the best signal integrity and good EMI performance, these critical components should be placed on the component side of the PCB. This will ensure that these components will be referenced to a contiguous ground plane reference on Layer 2 of the design. This will also minimize the use of vias in routing these signals.

CONFIG[3..0] Pins:

1. There are no component placement issues associated with the LAN8820 CONFIG[3..0] pins.

LED Pins:

1. There are no component placement issues associated with the LAN8820 LED pins.

Dedicated Configuration Strap Pins:

1. There are no component placement issues associated with the LAN8820 dedicated configuration strap pins.

Miscellaneous:

1. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes. Typically, this component is placed on the back of the PCB. This component has both ESD and EMI implications.

2. Bulk capacitors for each power plane can reside anywhere on the plane they serve.