

**ENT-AN0101**  
**Application Note**  
**VSC8658 100BASE-FX/1000BASE-X Over SerDes Pins**  
November 2006



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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.2

Revision 1.2 was published in April 2006. In revision 1.2 of this document, the section 2.3.1 was updated.

## 1.2 Revision 1.1

Revision 1.1 was published in March 2006. In revision 1.1 of this document, the device number was updated to VSC8658.

## 1.3 Revision 1.0

Revision 1.0 was published in April 2006. It is the first publication of this document.

## 2 Introduction

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This document will highlight the design differences needed to implement the new 100BASE-FX /1000BASE-FX over SerDes feature on the next Generation VSC8658 Octal PHY from the VSC8558 Silicon Revision B.

### 2.1 Audience

The target audiences for this document are hardware, system, and software designers as well as design managers evaluating this feature implementation.

### 2.2 References

#### 2.2.1 Vitesse Documents

- VSC8558 Datasheet
- VSC8658 Datasheet

#### 2.2.2 IEEE Standards

- IEEE 802.3 – CSMA/CD Access Method and Physical Layer Specification

### 3 Feature Differences for 100BASEFX

This section describes the hardware and software differences from the VSC8558 for a designer to implement the new 100BASE-FX feature over SerDes in the VSC8658 Octal PHY.

#### 3.1 Hardware Differences

To upgrade from supporting a 1000BASE-X device to a 100BASE-FX device for the VSC8658 Octal PHY is relatively straightforward. From a design implementation perspective whatever steps are required to implement either a 1000BASE-X GBIC or SFP will be the same design requirements for a 100BASE-FX SFP. The TX and RX Differential signals need to be connected the same manner to the TX and RX SerDes Differential signals as well as the Signal Detect/RX\_LOS signal to the SIG\_DET pin of the Octal PHY. AC Coupling capacitors are required if the common mode voltages between the device is different, although all Vitesse Octal PHYs have internal AC Coupling Capacitors integrated on its Fiber SerDes ingress, receiving pins.

#### 3.2 Register Differences

The following table describes the software changes necessary to implement the 100BASE-FX over SerDes pin feature.

**Table 1 • PHY Register 23 Updates**

| Operating Mode                                  | Register 23 bit 11 AMS Preference | Register 23 bit 10:8 Media Operating Mode |
|-------------------------------------------------|-----------------------------------|-------------------------------------------|
| CAT5 Copper Only                                | N/A                               | 000                                       |
| 1000BASE-X fiber/SFP pass-through mode only.    | N/A                               | 001                                       |
| No auto-negotiation performed in this PHY       |                                   |                                           |
| 1000BASE-X fiber/SFP only with auto negotiation | N/A                               | 010                                       |
| performed by the PHY.                           |                                   |                                           |
| 100BASE-FX fiber/SFP only                       | N/A                               | 011                                       |
| Reserved                                        | N/A                               | 100                                       |
| Auto-Media Sense with Copper CAT5 media or      | 0                                 | 101                                       |
| 1000BASE-X fiber/SFP pass-through mode.         |                                   |                                           |
| Fiber AMS preferred.                            |                                   |                                           |
| Auto-Media Sense with Copper CAT5 media or      | 1                                 | 101                                       |
| 1000BASE-X fiber/SFP pass-through mode.         |                                   |                                           |
| Copper AMS preferred.                           |                                   |                                           |

| Operating Mode                                                                                                                                 | Register 23 bit 11 AMS Preference | Register 23 bit 10:8 Media Operating Mode |
|------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-------------------------------------------|
| Auto-Media Sense with Copper CAT5 media or<br><br>1000BASE-X fiber/SFP with auto-negotiation<br><br>performed by the PHY. Fiber AMS preferred. | 0                                 | 110                                       |
| Auto-Media Sense with Copper CAT5 media or<br><br>1000BASE-X fiber/SFP with auto-negotiation performed by the PHY. Copper AMS preferred.       | 1                                 | 110                                       |
| Auto-Media Sense with Copper CAT5 media or 100BASE-FX fiber/SFP. Fiber AMS preferred.                                                          | 0                                 | 111                                       |
| Auto-Media Sense with Copper CAT5 media or 100BASE-FX fiber/SFP. Copper AMS preferred.                                                         | 1                                 | 111                                       |

### 3.3 Operational Differences

#### 3.3.1 LED Indication

For the 100BASE-FX mode, the link and activity LED indications will be performed by the following LED modes in Register 29:

Any LED that supports 100BASE-TX will now support 100BASE-FX indication, including:

- MODE0: Link/Activity
- MODE2: Link100/Activity
- MODE4: Link100/1000/Activity
- MODE6: Link10/100/Activity

If Fiber LED Disable = 0 (Register 30.15)

- MODE 7: Link100BASE-FX/1000-BASE-X/Activity
- MODE 11: 100BASE-FX/1000-BASE-X Activity

#### 3.3.2 Link Status

For Link Status Indication, the Link Status bit Register 1.2 will indicate if a link is present for 100BASE-FX.

Register 28.4:3 Speed Status, 01 will now both indicate 100BASE-TX and 100BASE-FX

#### 3.3.3 EPG (Packet Generator) and CRC Counters

EPG and CRC Counters will be supported in the 100BASE-FX mode over SerDes mode.

#### 3.3.4 Loopbacks

Near-End, Far-End and Connector Loopbacks will be supported in the 100BASE-FX over SerDes mode.

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