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## DOCUMENT DESCRIPTION

**Routing Checklist for the LAN83C185, 64-pin TQFP Package**

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# Routing Checklist for LAN83C185

### Information Particular for the 64-pin TQFP Package

## LAN83C185 TQFP Phy Interface:

1. The traces connecting the transmit outputs (TXP, pin 51) & (TXN, pin 50) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

2. The traces connecting the receive inputs (RXP, pin 55) & (RXN, pin 54) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

3. For differential traces running from the LAN controller to the magnetics, SMSC recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.

4. The AVDD power supply should be routed as a mini-plane and can be routed on an internal power plane layer.

5. The union of the 10.0Ω resistor supplying AVDD to the Transmit Channel center tap of the magnetics and the 0.022 μF capacitor, should be routed as a mini-plane.

## LAN83C185 TQFP Magnetics:

1. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.

2. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.

3. For differential traces running from the magnetics to the RJ45 connector, SMSC recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

## RJ45 Connector:

1. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause EMC problems.

2. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.

## Power Supply Connections:

1. Route the (3) VDD pins of the LAN83C185 TQFP directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the (3) VDD decoupling capacitors for the LAN83C185 TQFP power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

3. Route the (4) AVDD pins of the LAN83C185 TQFP directly into a solid, +3.3V power plane (created with a ferrite bead). The pin-to-plane trace should be as short as possible and as wide as possible.

4. In addition, route the (4) AVDD decoupling capacitors for the LAN83C185 TQFP power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

5. Route the (1) VREG pin of the LAN83C185 TQFP directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

6. In addition, route the (1) VREG decoupling capacitor for the LAN83C185 power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.

## Ground Connections:

1. The (7) digital ground pins (VSS) on the LAN83C185 TQFP should be routed directly into a solid, contiguous, internal ground plane. The pin-to-plane trace should be as short and as wide as possible.

2. The (5) analog ground pins (AVSS) on the LAN83C185 TQFP should be routed directly into the same solid, contiguous, internal ground plane. The pin-to-plane trace should be as short and as wide as possible.

3. We recommend that the Digital Ground pins (VSS) and the AVSS pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

## VDD_CORE:

1. The VDD_CORE pin (pin 14) must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it. A mini-plane is also acceptable.

## Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.

2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.

## EXRES1 Resistor:

1. The EXRES1 resistor (pin 59) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the EXRES1 resistor.

## MII Interface:

1. The MII interface on the LAN83C185 should be constructed using 68-ohm traces.

## Required External Pull-ups:

1. There are no critical routing instructions for the Required External Pull-up connections.

## Mode Pins:

1. There are no critical routing instructions for the Mode Pin connections.

## Phy Address Pins:

1. There are no critical routing instructions for the Phy Address Pin connections.

## LED Pins:

1. There are no critical routing instructions for the LED Pin connections.

## Miscellaneous:

1. SMSC recommends utilizing at least a four-layer design for boards for the LAN83C185 TQFP device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.

2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.

3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.

4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.

5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.