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A	Release		8-3-07
B	Added Phy Address / LED Polarity Diagram & Interrupt Section		9-7-07

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DOCUMENT DESCRIPTION
Schematic Checklist for the LAN83C185, 64-pin TQFP Package

 	SMSC 80 Arkay Drive Hauppauge, New York 11788	
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	SC471206	B

Schematic Checklist for LAN83C185

Information Particular for the 64-pin TQFP Package

LAN83C185 TQFP Phy Interface:

1. TXP (pin 51); This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω , 1.0% pull-up resistor to AVDD (created from +3.3V). This pin also connects to the transmit channel of the magnetics.
2. TXN (pin 50); This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω , 1.0% pull-up resistor to AVDD (created from +3.3V). This pin also connects to the transmit channel of the magnetics.
3. For Transmit Channel connection and termination details, refer to Figure 1.
4. RXP (pin 55); This pin is the receive twisted pair input positive connection to the internal phy. This pin must be AC coupled to the receive channel of the magnetics. This is accomplished by a series $6.8\text{ }\eta\text{F}$ capacitor connecting it to the magnetics. This pin also requires a 49.9Ω , 1.0% termination, AC coupled to digital ground. The capacitor used in this instance is a $0.01\text{ }\mu\text{F}$ to digital ground. The union of the resistor and the $0.01\text{ }\mu\text{F}$ capacitor must be connected to the center tap of the receive channel of the magnetics.
5. RXN (pin 54); This pin is the receive twisted pair input negative connection to the internal phy. This pin must be AC coupled to the receive channel of the magnetics. This is accomplished by a series $6.8\text{ }\eta\text{F}$ capacitor connecting it to the magnetics. This pin also requires a 49.9Ω , 1.0% termination, AC coupled to digital ground. The capacitor used in this instance is a $0.01\text{ }\mu\text{F}$ to digital ground. The union of the resistor and the $0.01\text{ }\mu\text{F}$ capacitor must be connected to the center tap of the receive channel of the magnetics.
6. Only one $0.01\text{ }\mu\text{F}$ capacitor to digital ground is required. It is shared by both 49.9Ω resistors
7. Together, the two 49.9Ω resistors form a 100Ω termination that the Ethernet receive channel requires.
8. For Receive Channel connection and termination details, refer to Figure 2.

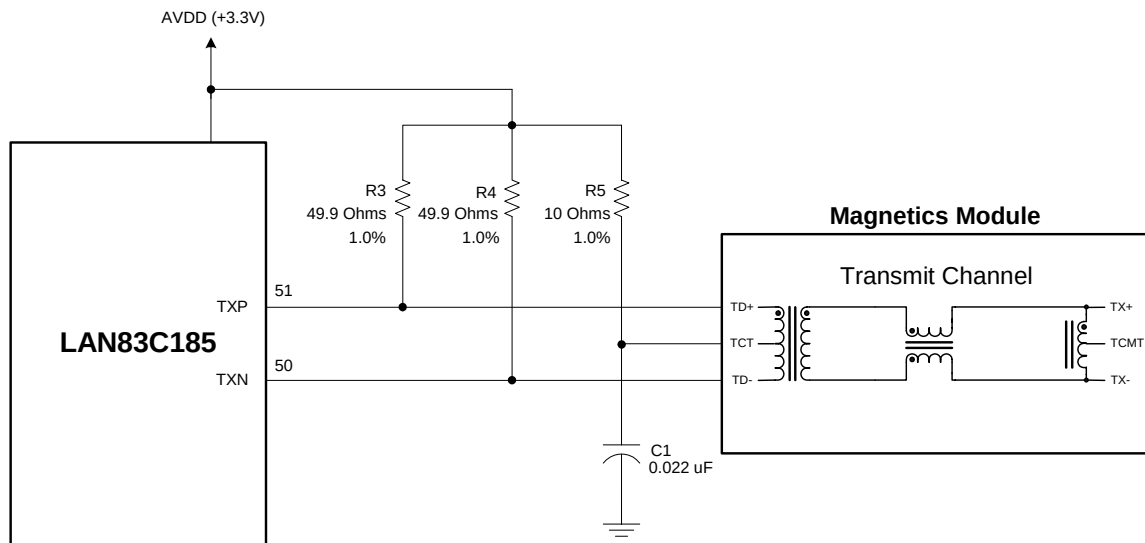


Figure 1 – Transmit Channel Connections and Terminations

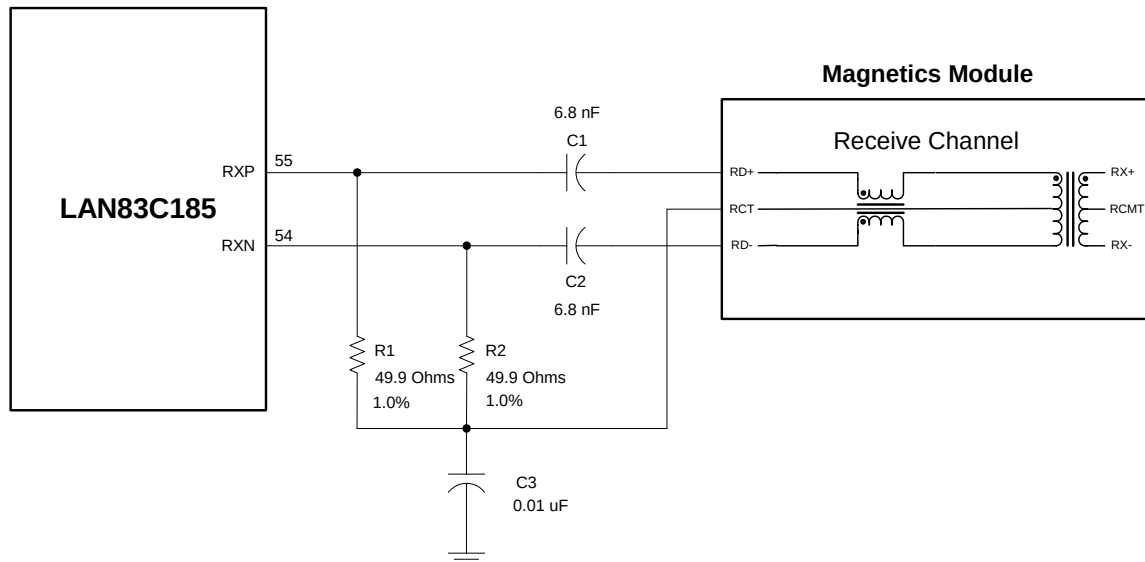


Figure 2 - Receive Channel Connections and Terminations

LAN83C185 TQFP Magnetics:

1. The center tap connection on the LAN83C185 side for the transmit channel must be connected to AVDD (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the magnetics also requires a $0.022\ \mu\text{F}$ capacitor terminated to digital ground.
2. The center tap connection on the LAN83C185 side for the receive channel must be referenced to the 100Ω termination of the receive channel. This is accomplished by connecting the receive channel center tap to the union of the (2) 49.9Ω resistors and the $0.01\ \mu\text{F}$ capacitor as described in the above section.
3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a $1000\ \mu\text{F}$, 2KV capacitor (C_{magterm}) to chassis ground.
4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a $1000\ \mu\text{F}$, 2KV capacitor (C_{magterm}) to chassis ground.
5. Only one $1000\ \mu\text{F}$, 2KV capacitor (C_{magterm}) to chassis ground is required. It is shared by both TX & RX center taps.
6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP (pin 51) of the LAN83C185 TQFP.
7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN (pin 50) of the LAN83C185 TQFP.
8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP (pin 55) of the LAN83C185 TQFP.
9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN (pin 54) of the LAN83C185 TQFP.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:
 - a) Pins 4 & 5 can be connected together with two 49.9 Ω resistors. The common connection of these resistors should be connected through a third 49.9 Ω to the 1000 pF, 2KV capacitor (C_{rjterm}).
 - b) For a lower component count, the resistors can be combined. The two 49.9 Ω resistors in parallel look like a 25 Ω resistor. The 25 Ω resistor in series with the 49.9 Ω makes the whole circuit look like a 75 Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75 Ω resistor in series with the 1000 pF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.
2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:
 - a) Pins 7 & 8 can be connected together with two 49.9 Ω resistors. The common connection of these resistors should be connected through a third 49.9 Ω to the 1000 pF, 2KV capacitor (C_{rjterm}).
 - b) For a lower component count, the resistors can be combined. The two 49.9 Ω resistors in parallel look like a 25 Ω resistor. The 25 Ω resistor in series with the 49.9 Ω makes the whole circuit look like a 75 Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75 Ω resistor in series with the 1000 pF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.
3. The RJ45 shield should be attached directly to chassis ground.

Power Supply Connections:

1. The digital supply (VDD) pins on the LAN83C185 TQFP are 8, 18 & 43. They require a connection to +3.3V.
2. Each power pin should have one .01 μ F (or smaller) capacitor to decouple the LAN83C185. The capacitor size should be SMD_0603 or smaller.
3. The analog supply (AVDD) pins on the LAN83C185 TQFP are 53, 57, 61 & 63. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
4. Each AVDD pin should have one .01 μ F (or smaller) capacitor to decouple the LAN83C185. The capacitor size should be SMD_0603 or smaller.
5. Pin 13 (VREG) is a supply voltage for the internal +1.8V regulators. This pin must be connected to +3.3V.
6. The VREG pin should have one .01 μ F (or smaller) capacitor to decouple the LAN83C185. The capacitor size should be SMD_0603 or smaller.

Ground Connections:

1. The digital ground pins (VSS) on the LAN83C185 TQFP are 7, 15, 21, 24, 28, 36 & 40. They need to be connected directly to a solid, contiguous ground plane.
2. The analog ground pins (AVSS) on the LAN83C185 TQFP are 49, 52, 58, 60 & 62. They also need to be connected directly to the same solid, contiguous ground plane.
3. We recommend that the Digital Ground pins and the AVSS pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

VDD_CORE:

1. VDD_CORE (pin 14), this pin is used to provide bypassing for the +1.8V core regulator. This pin requires a 0.01 μF decoupling capacitor. This capacitor should be located as close as possible to its pin without using vias. In addition, pin 14 requires a bulk capacitor placed as close as possible to pin 14. The bulk capacitor must have a value of at least 10 μF , and have an ESR (equivalent series resistance) of no more than 2.0 Ω . SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only. **Do Not** power other circuits or devices with this supply.

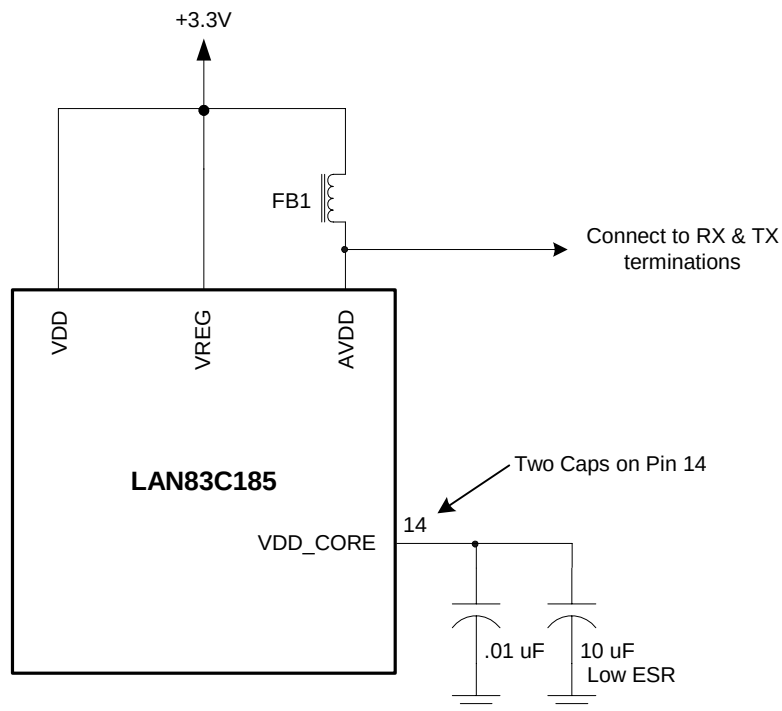


Figure 3 - LAN83C185 Power Connections

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN83C185 TQFP. For exact specifications and tolerances refer to the latest revision LAN83C185 data sheet.
2. CLKIN/XTAL1 (pin 23) on the LAN83C185 TQFP is the clock circuit input. This pin requires a 15 – 33 pF capacitor to digital ground. One side of the crystal connects to this pin.
3. XTAL2 (pin 22) on the LAN83C185 TQFP is the clock circuit output. We recommend placing a 0 Ω resistor in series with this pin to the crystal for future EMI considerations. The other side of the resistor can then connect to a matching 15 – 33 pF capacitor to ground and the other side of the crystal.
4. Since every system design is unique, the value for the series resistor and the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

EXRES1 Resistor:

1. EXRES1 (pin 59) on the LAN83C185 TQFP should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

MII Interface:

1. When utilizing either an external MII MAC interface or an MII Connector, the following table indicates the proper connections for the 18 signals.

From:	Connects To:	
	MII MAC Device	MII Connector
LAN83C185 TQFP		
RXD0 (pin 32)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 31)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 30)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 29)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 33)	RX_DV	RX_DV (contact 8)
RX_ER (pin 35)	RX_ER	RX_ER (contact 10)
RX_CLK (pin 34)	RX_CLK	RX_CLK (contact 9)
TX_ER (pin 37)	TX_ER	TX_ER (contact 11)
TXD0 (pin 41)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 42)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 44)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 45)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin 39)	TX_EN	TX_EN (contact 13)
TX_CLK (pin 38)	TX_CLK	TX_CLK (contact 12)
CRS (pin 48)	CRS	CRS (contact 19)
COL (pin 47)	COL	COL (contact 18)
MDIO (pin 26)	MDIO	MDIO (contact 2)
MDC (pin 27)	MDC	MDC (contact 3)

2. CLK_FREQ (pin 11) this defines the frequency of the input clock to the LAN83C185. A low on this pin configures the phy clock for 25 MHz operation. This input needs to be held low continuously, during and after reset. This pin must be tied low through a 56.2 Ω resistor to digital ground.
3. MII (pin 1) this defines the MII Bus operation of the LAN83C185. A low on this pin configures the LAN83C185 for normal MII Bus operation. This input needs to be held low continuously, during and after reset. This pin must be tied low through a 56.2 Ω resistor to digital ground.
4. Provisions should be made for series terminations for all outputs on the MII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN83C185 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependant and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 10.0 Ω .

Required External Pull-ups:

1. nINT (pin 46) requires an external pull-up resistor as this output is an Open Drain type.
2. When using the MII interface of the LAN83C185 TQFP with a MAC device on board, a pull-up resistor on the signal MDIO (pin 26) must be incorporated. A pull-up resistor of 1.5K Ω to +5V is required for this application.

Mode Pins:

1. The Mode pins of the LAN83C185 (MODE[2:0]) control the default configuration of the 10/100 Phy. Speed, Duplex, Auto-Negotiation & power down functionality can be configured through these pins. The value of these three pins are latched in upon power-up and reset. The values latched in are reflected in Register 0 & Register 4 of the LAN83C185. See the LAN83C185 data sheet for complete details for the operation of these pins. These three pins have weak internal pull-ups and can be left as no-connects.

Phy Address Pins:

1. The Phy address pins of the LAN83C185 (PHYAD[4:0]) determine which of the 32 addresses the LAN83C185 will respond to. The value of these five pins are latched in upon power-up and reset. The values latched in are reflected in Register 18 of the LAN83C185. See the LAN83C185 data sheet for complete details for the operation of these pins. These five pins have weak internal pull-ups and can be left as no-connects.
2. A basic Phy address of 01h is usually recommended.
3. The Phy Address pins are shared with the LED functionality and one general purpose output of the LAN83C185. The pinouts are as follows:

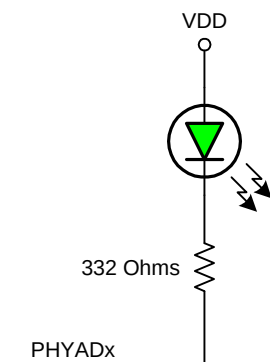
Phy Address 0 is shared with LED SPEED100 on pin 16.

Phy Address 1 is shared with LED LINKON on pin 17.

Phy Address 2 is shared with LED ACTIVITY on pin 19.

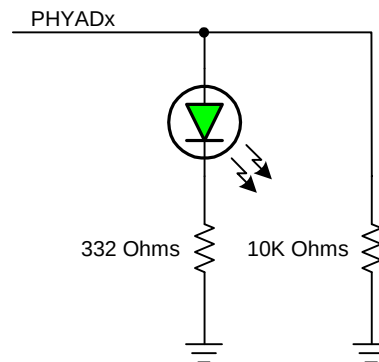
Phy Address 3 is shared with LED FDUPLEX on pin 20.

Phy Address 4 is shared with GPO1 on pin 2.



PHY Address Bit = 1

**LED Output Signal from
LAN83C185 is Active Low**



PHY Address Bit = 0

**LED Output Signal from
LAN83C185 is Active High**

Figure 4 Phy Address / LED Polarity

LED Pins:

1. The LAN83C185 provides four LED signals. These indicators will display speed, duplex, link and activity information about the current state of the Phy. The LED outputs have the ability to be either active high or active low. The polarity is determined by the Phy address latched in at reset. The LAN83C185 senses each Phy address bit and changes the polarity of the LED signal accordingly. If the address bit is set as a level one, the LED polarity will be set to an active-low. If the address bit is set as a level zero, the LED polarity will be set to an active high; see Figure 4 above. See the LAN83C185 data sheet for further details on how to strap each pin for correct Phy addressing and LED polarity outcomes.
2. The LED and one general purpose output pins are shared with the Phy Address functionality of the LAN83C185. The pinouts are as follows:

LED SPEED100 is shared with Phy Address 0 on pin 16.

LED LINKON is shared with Phy Address 1 on pin 17.

LED ACTIVITY is shared with Phy Address 2 on pin 19.

LED FDUPLEX is shared with Phy Address 3 on pin 20.

GPO1 is shared with Phy Address 4 on pin 2.

Interrupt Functionality:

1. For added flexibility, the LAN83C185 TQFP has a discrete interrupt line for embedded applications. This is advantageous as there is no interrupt facility across the standard MII Bus interface.
2. nINT (pin 46) this pin provides the interrupt signal from the LAN83C185. This signal requires an external pull-up resistor as this output is an Open Drain type.

Miscellaneous:

1. There are two No-Connect pins on the LAN83C185. It is very important that these pins remain as no-connects. These pins are 56 & 64.
2. TEST0 & TEST1 (pins 9 & 10) are used for internal test modes only. They have no end-user functionality. These two pins have weak internal pull-downs and should be left as no-connects on the device. It is very important that these two pins remain low at all times.
3. REG_EN (pin 12) this pin enables the internal +1.8V core regulator of the LAN83C185. To enable the regulator, this pin must be tied to +3.3V. To disable the regulator, this pin should be tied to ground. Normal operation will have this pin tied to +3.3V.
4. nRST (pin 25), this pin is an active-low reset input. This signal resets all logic and registers within the LAN83C185. If nRST is left unconnected the LAN83C185 will rely on its internal power-on reset circuitry.
5. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.
6. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

LAN83C185 TQFP QuickCheck Pinout Table:

Use the following table to check the LAN83C185 TQFP shape in your schematic.

LAN83C185 TQFP							
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GPO0/MII	17	LINKON/PHYAD1	33	RX_DV	49	AVSS
2	GPO1/PHYAD4	18	VDD	34	RX_CLK	50	TXN
3	GPO2	19	ACTIVITY/PHYAD2	35	RX_ER/RXD4	51	TXP
4	MODE0	20	FDUPLEX/PHYAD3	36	VSS	52	AVSS
5	MODE1	21	VSS	37	TX_ER/TXD4	53	AVDD
6	MODE2	22	XTAL2	38	TX_CLK	54	RXN
7	VSS	23	CLKIN/XTAL1	39	TX_EN	55	RXP
8	VDD	24	VSS	40	VSS	56	NC2
9	TEST0	25	nRST	41	TXD0	57	AVDD
10	TEST1	26	MDIO	42	TXD1	58	AVSS
11	CLK_FREQ	27	MDC	43	VDD	59	EXRES1
12	REG_EN	28	VSS	44	TXD2	60	AVSS
13	VREG	29	RXD3	45	TXD3	61	AVDD
14	VDD_CORE	30	RXD2	46	nINT	62	AVSS
15	VSS	31	RXD1	47	COL	63	AVDD
16	SPEED100/PHYAD0	32	RXD0	48	CRS	64	NC1

Notes:

Reference Material:

1. SMSC LAN83C185 Data Sheet; check web site for latest revision.
2. SMSC LAN83C185 EVB Schematic, Assembly No. 6316 (Kilkerrin); check web site for latest revision.
3. SMSC LAN83C185 EVB PCB, Assembly No. 6316; order PCB from web site.
4. SMSC LAN83C185 EVB PCB Bill of Materials, Assembly No. 6316; check web site for latest revision.
5. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.