

DRF Series Design Guide

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Introduction

In this Design Guide we will detail the design process involved when using the DRF Series of devices and their performance. As we move through this document it will be necessary to clearly define and explain multiple technical points so that we have a mutual understanding of the key issues and how to address them. The DRF Series is based on a Flangeless Mechanical design illustrated in Figure 1. All of these devices incorporate at least one driver die, the DRF100; all others have one or two driver die and one or two MOSFET devices.

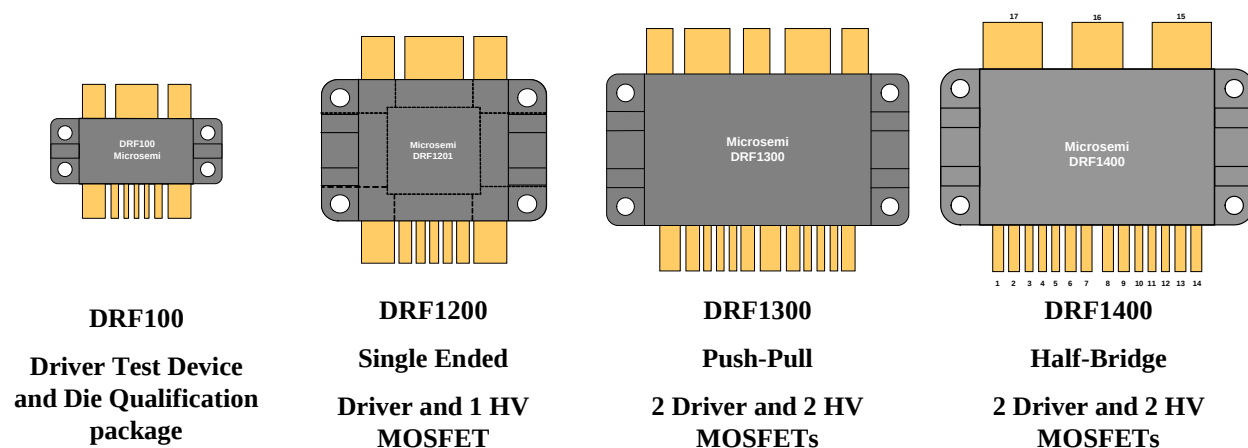


Figure 1. DRF Series Devices

The DRF100 was the platform used to develop and qualify the RF Driver IC. Understanding the design, layout and function of the DRF100 is necessary to appropriately understand the DRF family of devices. The DRF devices are capable of multiple Kilowatts at RF Frequencies of < 2MHz to > 30MHz; the DRF1200 Series 1KW; the DRF1300 Series 1-2KW; and the DRF1400 Series 2-3KW.

DRF100

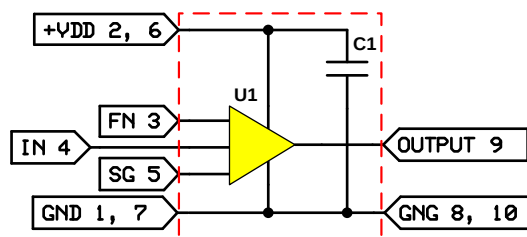


Figure 2. Simplified DRF100 Circuit Diagram

FN Invert Non-Invert	IN	Output	FUNCTION
High	High	High	Non-Inverting
High	Low	Low	Non-Inverting
Low	High	Low	Inverting
Low	Low	High	Inverting

Table 1

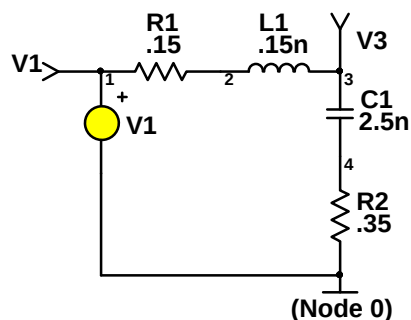
The simplified DRF100 Circuit Diagram is illustrated in Figure 2 above. By including the high speed by-pass capacitor, the contribution to the internal parasitic loop inductance of the driver output is greatly reduced. This low parasitic approach, coupled with the Schmitt Trigger input (pin 4), Kelvin Signal Ground (pin 5) and the Anti-Ring Function, provide improved stability and control. The IN pin (4) is applied to a Schmitt Trigger. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. The P channel and N channel power drivers provide the high current to the Output (pin 9). Table 1 is the truth table for the DRF100.

Electrical

MOSFET Model and Parasitics

The DRF100 is a High-Speed Power RF MOSFET driver. It is intended to drive the gate of a power RF MOSFET with $\geq 3\text{nF}$ gate capacitance to 15V at frequencies up to 30MHz. It can produce output currents $\geq 8\text{A RMS}$, while dissipating 60W. The Driver output can be configured as Inverting or Non-Inverting.

To understand the driver and its integration into a power RF package with a power MOSFET, it will be useful to review the important design considerations in that process. The Driver circuit model is illustrated in Figure 3.



R1 represents the on resistance of the internal MOSFETs in the output section of the Driver. This parameter is driven by driver performance requirements. L1 accounts for Loop Inductance in the driver output. C1 models the effective output capacitance of the driver and R2 is the ESR of C1. V1 provides the control signal.

Figure 3. Driver Circuit Model

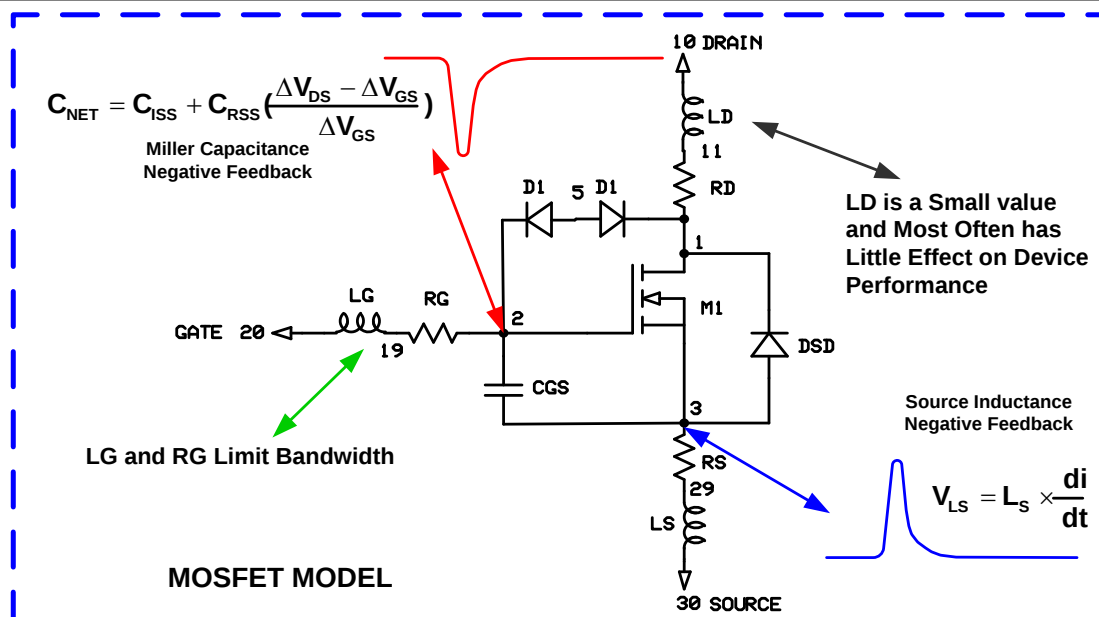


Figure 4. Negative Feedback Terms

There are two significant Negative Feedback Terms that affect MOSFET performance, the DRF100, and all the DRF devices. They are the effect of **Miller Capacitance** (C_{NET}) and **Source Lead Inductance** (V_{LS}). Figure 4 shows the location of these two Negative Feedback Terms and the equations that describe their effects on MOSFETs and the DRF Series Devices. We have little control over the C_{NET} term; however we can ensure, by design, that the Driver IC has sufficient output voltage swing and power margin to drive all the RF MOSFETs we may choose to use. In addition we have taken great care to minimize the V_{LS} and LG terms in all of the DRF Devices. LG and RG impact Bandwidth and switching speed. LD in most DRF devices is between 5 and 15nH in the Drain circuit. This has very little effect on most circuits operating below 50MHz.

Referring to Figure 4, as the current rises in the MOSFET at turn on, the Voltage at Node 3, MOSFET Source (Die) also rises. This is a negative feedback term to the Gate Drive at Node 2. The magnitude is driven by the inset equation for (V_{LS}).

At the same time, the voltage at the Drain (Die), Node 1, falls. This falling voltage produces a negative feedback term to the Gate (Die) Node. The magnitude of this “Miller Feedback” is given by the inset formula (C_{NET}). In short it presents an increase in effective input capacitance which is voltage and time dependent. The time dependency is determined by the rate of change of the drain voltage.

Miller Capacitance is a function of Silicon Die design - the bigger the die, the larger the Miller effect. The Source, Gate and Drain lead inductance are byproducts of the geometry of the package design.

As we integrate Figure 3 and Figure 4 into a Hybrid, we cross from the discrete components, as illustrated in Figure 4, to a multi-chip module design. In that process it is important to minimize all parameters that will limit performance of the hybrid.

Loop Inductance

This section discusses how package inductance and circuit stray inductance are formed, and how to minimize them.

The parasitic loop for an RF Output is schematically illustrated in Figure 5. The Source V1 is the square wave output to the RF Network and the load. The mechanical geometry forms a current loop that is very critical to Circuit Operation. The smaller the loop, the lower the stray inductance.

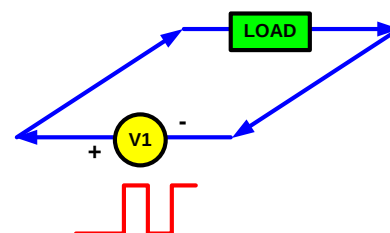


Figure 5. Current Loop in an RF Loop

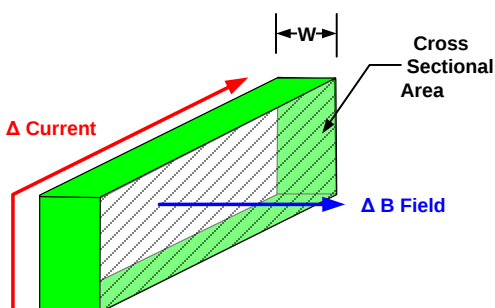


Figure 6. Loop Inductance

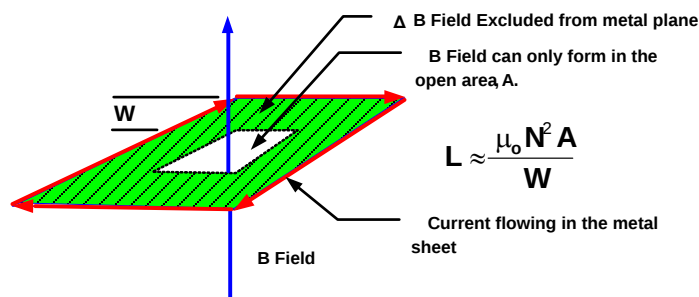


Figure 7. Loop Inductance

Figures 6 and 7 illustrate the output loop inductance of an RF Power Output Stage. From Equation 1 we see that the stray inductive term is directly proportional to the Cross Sectional Area. Therefore, if we minimize the Cross Sectional Area we will reduce the loop inductance proportionally. In addition, if we increase the width **W** we will also reduce the Loop Inductance. See the equation below.

Equation 1

$$L = \frac{\mu_0 N^2 A}{W}$$

Where:

L = Inductance, H

μ₀ = Permeability of Free Space, $1.26 \times 10^{-6} \text{ H m}^{-1}$

N² = (Number of turns)² = 1

A = Cross Sectional Area, m²

W = Width, m

Equation 2

$$L : \frac{A}{W}$$

For the RF Output Section this loop inductance is a very critical, geometry and layout-driven, parameter. The smaller the better. This lower inductance drives the ring frequency higher with lower amplitude. If the loop inductance is too large ringing on the top of the Drain voltage waveform can have severe consequences, such as HV breakdown, reduced power output, higher harmonics and loss of stability. The PCB layout must incorporate this understanding. This will be discussed in more detail later in the Hybrid section and in the Push-Pull and Half-Bridge sections.

Equation 1 shown at the left is simplified but accurate enough for our discussion. Looking at this equation, we see the only two terms that we can change are terms **A** and **W**. See Equation 2. In the process of Printed Circuit design it is essential that **A/W** is minimized in order to optimize circuit Performance.

Mechanical

The DRF family of RF Hybrid Devices incorporates one or two RF Driver Integrated Circuits and one or two RF Power MOSFETs. The DRF Series devices are designed to allow their user to focus on the Output RF elements in the design with little need to address the RF Driver. For this discussion we will start with the Flangeless Discrete Devices. Figure 8 illustrates the construction of the Legacy Devices and the New Flangeless devices. The principal physical difference between the two, is the Copper Tungsten Flange, used on legacy devices. This leads to a difference in the Thermal Impedance, Power Cycle Capability as well as Electrical and RF performance. There is also the cost differential between the two technologies.

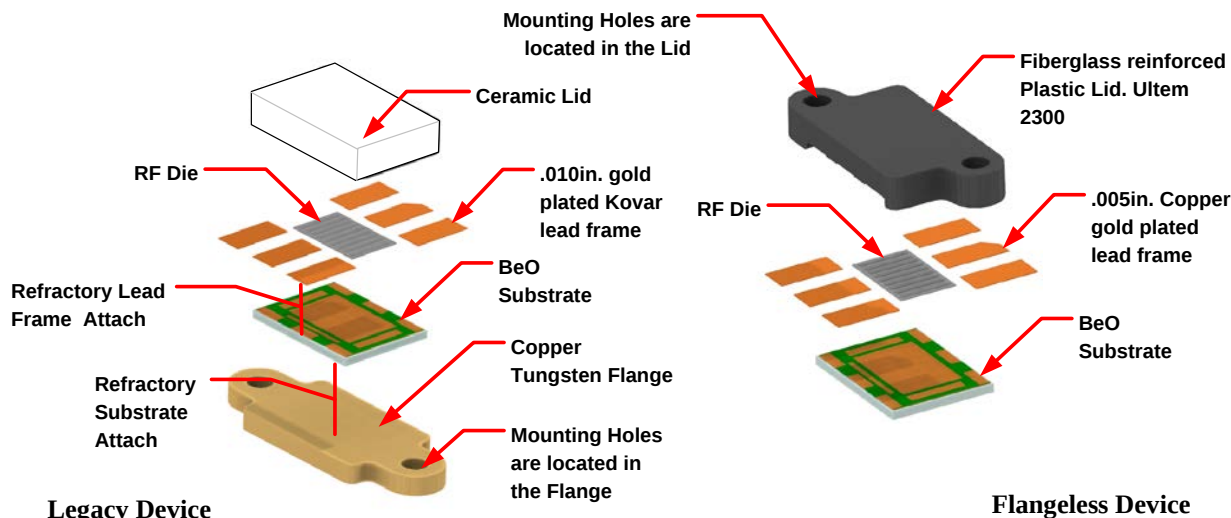


Figure 8. Legacy and New Flangeless Construction

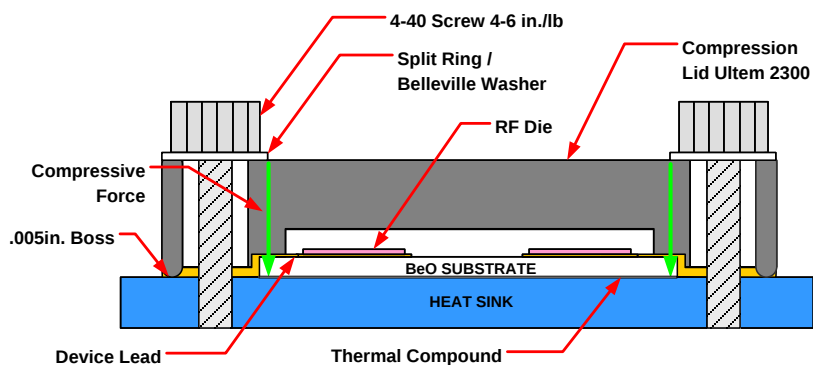


Figure 9. Flangeless Power Device

In Figure 8 we see both the Flangeless and the legacy Flanged device. There are only three obvious components that they share: the lead frame, the die and the substrate. The compression mechanics of the package design are less obvious. Referring to Figure 9, when the two 4-40 screws are tightened, the 0.005in. Bosses at the two ends of the package lid, force the package to flex.

These Bosses contact the heat sink first. As torque is applied to the mounting screws, the lid begins to flex and in so doing applies a constant pressure to the substrate, pressing it hard onto the heat sink. The two green arrows in Figure 9 illustrate this pressure. The side walls of the plastic lid have been removed in this sectioned view of the package. The side walls are thick and tall so that the pressure applied along the complete perimeter of the BeO substrate is close to the same. The lid is constructed with a fiberglass reinforced plastic, Ultem 2300, an exceedingly strong high temperature material.

Thermal

Figure 10 illustrates the VRF154 Thermal Profile and Figure 11 the MRF154, a flanged device with similar mechanical construction. The Thermal Profile illustrates one of the differences between the Flangeless and the Flanged device. They both start at 25°C and end at 175°C, however it is the point-by-point delta in these two plots as they move between limits that illustrates the different in the specific heat of the packages.

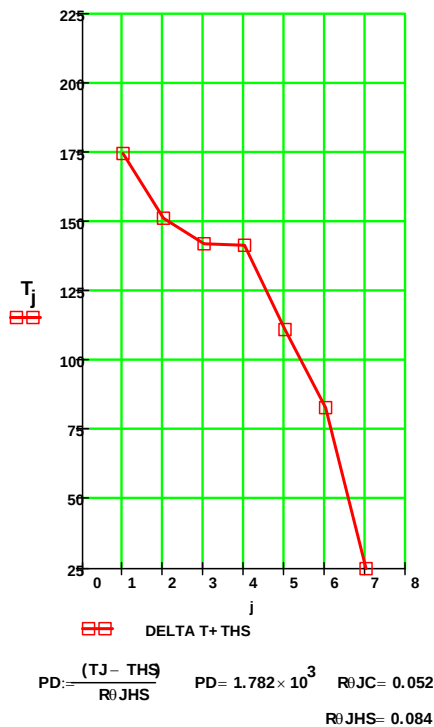


Figure 10. VRF154 Thermal Profile

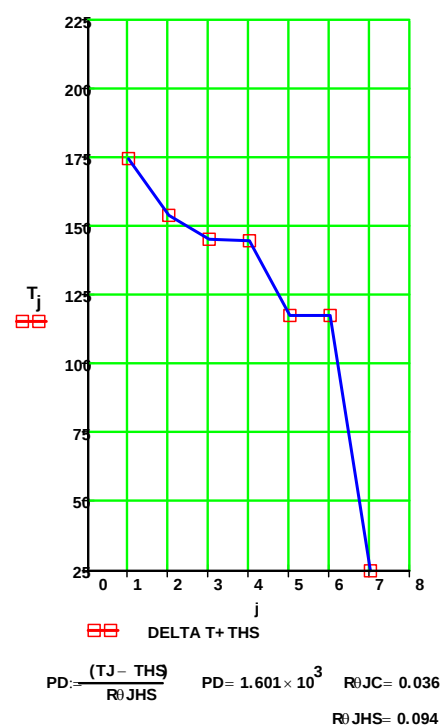


Figure 11. MRF154 Thermal Profile

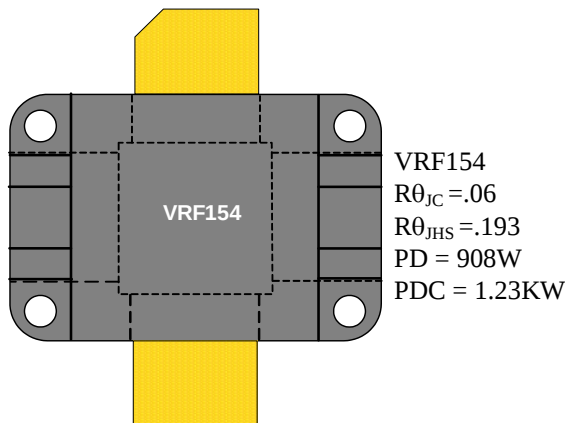


Figure 12. VRF154

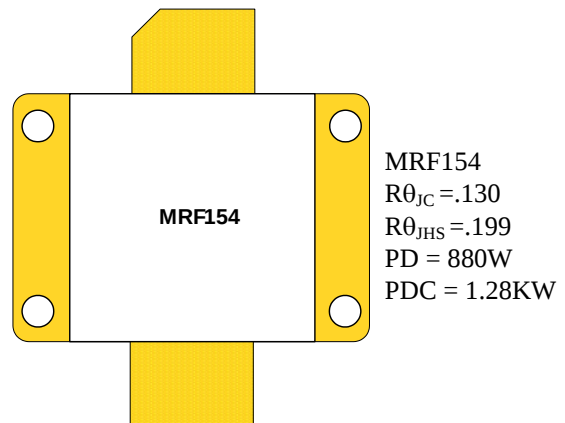


Figure 13. MRF154

The most important point is that the new VRF154 Flangeless Design, Figure 12, and the MRF154 legacy design, Figure 13, are very similar in thermal performance. In electrical performance they are, for all practical purposes, identical. As was true for the previous section, the cost is different. For the VRF154 and the MRF154, this difference is substantial.

Power Calculations

These calculations are for the Driver portion of the DRF family of devices. The driver power consumption is low but not insignificant. This necessitates a design step for the proper operation of any of the DRF Series Hybrids, DRF12XX, DRF13XX and DRF14XX.

Driver Power Loss

$$P = C_{NET} \times V_{GS}^2 \times f$$

Miller Capacitance

C_{NET} must include the driver C_{oss} and the C_{iss} , C_{rss} of the MOSFET used in the Hybrid. This is given in the Data Sheet. In the case of the DRF100, use only the C_{oss} of the Driver and the load power.

$$C_{NET} = \left[C_{ISS(MOSFET)} + \left[C_{RSS(MOSFET)} \left[\frac{\Delta V_{DS} - \Delta V_{GS}}{\Delta V_{GS}} \right] \right] \right] + C_{OSS(DRIVER)}$$

Let:

Driver $C_{OSS} = 2500\text{pF}$

$C_{ISS(MOSFET)} = 1890\text{pF}$ (Load to Driver)

$C_{RSS(MOSFET)} = 75\text{pF}$ (Load to Driver)

$\Delta V_{DS} = 400\text{V}$

$\Delta V_{GS} = 15\text{V}$

$V_{DD} = 15\text{V}$

$f = 13.56\text{MHz}$

$R_{\theta JSH} = 2.53^\circ\text{C/W}$

$$C_{NET} = \left[1890\text{pF} + \left[75\text{pF} \left[\frac{400\text{V} - 15\text{V}}{15\text{V}} \right] \right] \right] + 2500\text{pF}$$

$$C_{NET} = 1890\text{pF} + 1925\text{pF} + 2500\text{pF} = 6315\text{pF}$$

Power Loss in the Driver is:

$$P = 6315\text{pF} \times 15^2 \times 13.56\text{MHz}$$

$$P = 19.26\text{W}$$

Driver V_{DD} Current

$$I_{DRIVER} = \frac{P}{V_{DD}} = \frac{19.26\text{W}}{15\text{V}} = 1.284\text{A}$$

Operating Temperature

$$\Delta T = R_{\theta JHS} \times P$$

$$\Delta T = 2.53^\circ\text{C/W} \times 19.26\text{W} \approx 49^\circ\text{C}$$

For a DRF device, the total Driver Power of 19.26W must be added to the power loss that will be dissipated in the Power MOSFET(s) during operation. The Heat sink must be designed accordingly.

Driver Power Outputs and Power Grounds

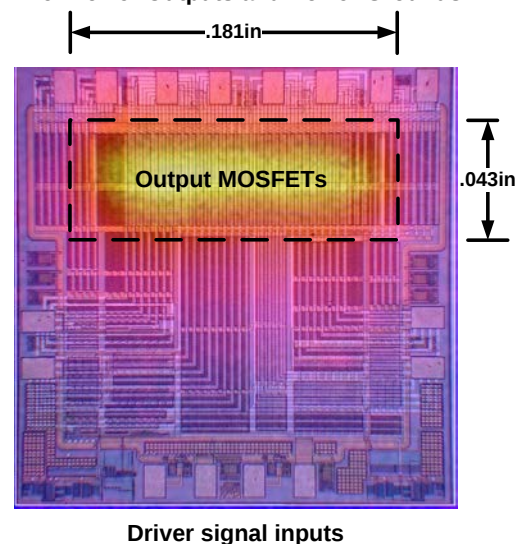


Figure 14. Internal Thermal Image of Driver Die

The heat distribution in the Driver Die is illustrated in Figure 14. As we see the Output MOSFET Section of the die is the hottest. The balance of the die generates very little heat. Therefore the DRF100 datasheet uses the 0.181in x 0.043 in. area for the thermal power dissipation specification. Assuming a 45°C heat sink, the Junction Temperature will be 94°C. This is well below the 150°C rating of the device.

DRF Hybrids

DRF100 Driver Die Operation

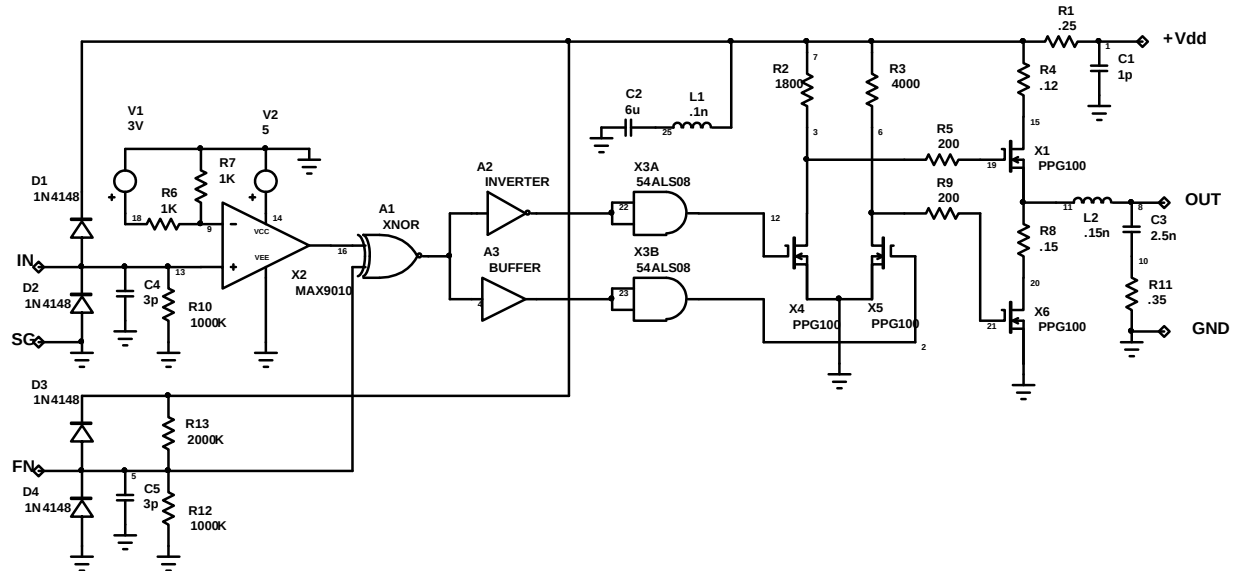


Figure 15. DRF100 Equivalent SPICE Sub-Circuit Diagram

DRF100 Driver Die Sub Circuit Diagram

The DRF SPICE Sub Circuit Diagram is illustrated in Figure 15 above. X2, the MAX9010 model, is used as the input comparator. The Switching Speed is a close match to the DRF100 input, however, the Hysteresis has been altered to more closely model the DRF100 performance. The XOR gate A1 is used to provide the Invert Function of the FN pin. Inverters A2 and A3 are used to create the Device Delay. Gates X3A and X3B provide the drive for the differential pair X4 and X5. These two devices provide the drive and signal timing for the Half-Bridge Output devices X1 and X6. L2, C3 and R11 model the output characteristics of the DRF100. All parameters of the DRF100 Model are accurate with respect to the device performance, with the exception of the DC idle current. The specification is $\cong 2\text{mA}$ however the model idle current is $\cong 4\text{mA}$. It should be noted that the SPICE Model of Figure 15 will not function if the Reference Ground is not at $\text{DC}=0$ and $\text{dV/dt}=0$ and the Anti-Ring function is not modeled.

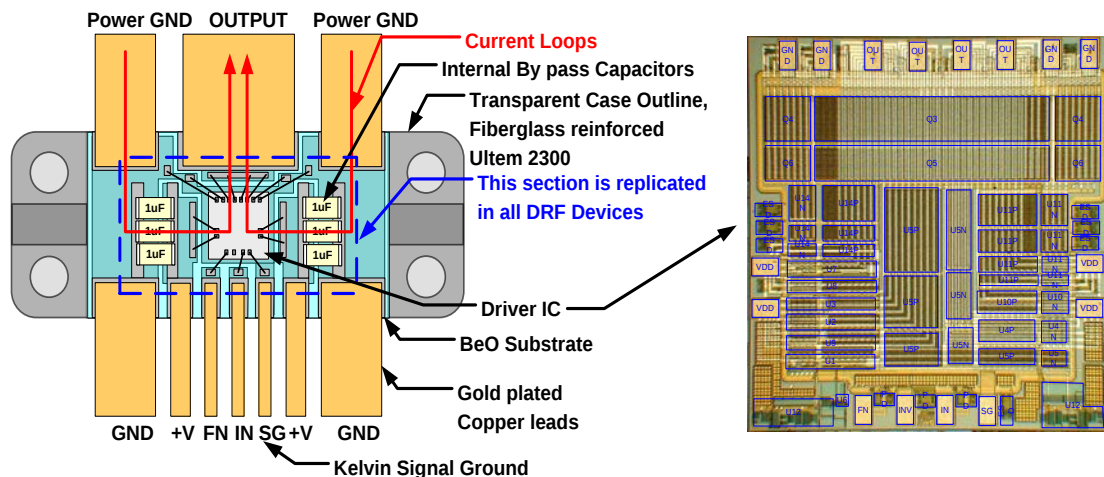
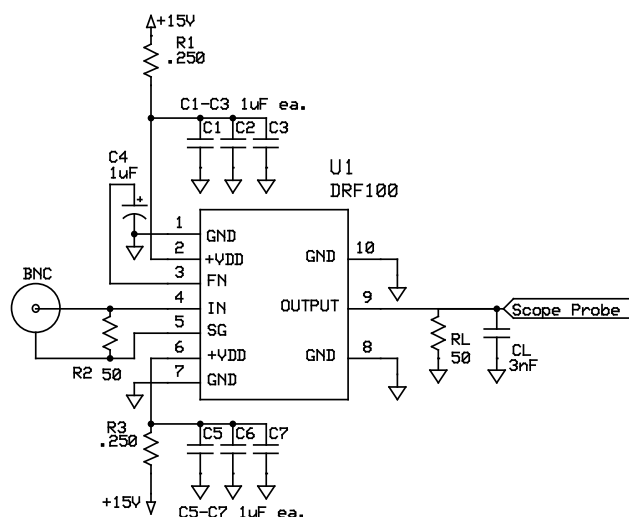


Figure 16. DRF100 Internal View

Referring to the discussion of inductive loops on Page 4, the Internal High Speed bypassing capacitors and the Coplanar Current Loop are illustrated in Figure 16. The symmetry of the Coplanar Loop, minimizing the area and the opposing currents, provides for a reduction in apparent inductance. Locating the internal High-Speed By-Passing within this loop enables the fast turn on and off performance of the driver. Moving the capacitors outside of the package would severely compromise the switching speed by increasing the Loop Inductance as previously stated. We will see that reducing the cross-sectional area, balanced and opposed current flows via circuit symmetry are necessary to reduce inductive strays and therefore increase the system operating RF Frequency.

DRF100 Test Circuit

The Test Circuit for the DRF100 is shown in Figure 17 and the Fixture is shown in Figure 4.



In Figure 17 we see that both V_{DD} pins 2 and 6 are heavily bypassed. This is recommended for optimum operation performance and stability. The FN pin can be bypassed for increased noise immunity in the Non-Inverting mode. In the Inverting Mode this is not necessary. The control signal is applied to the IN pin via a BNC connector. This signal is terminated in 50Ω for the test circuit, however this input can be terminated in 500Ω to $1K\Omega$ depending on circuit requirements and noise immunity requirements.

Figure 17. DRF100 Test Circuit

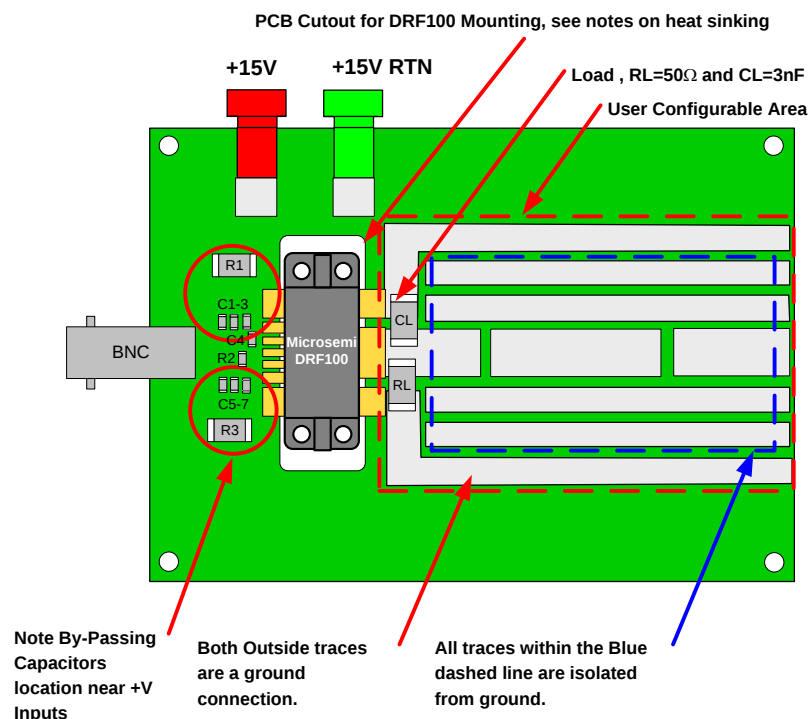


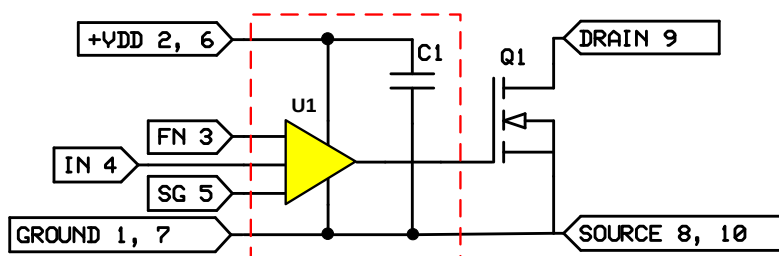
Figure 18 is an illustration of the DRF100 Evaluation Board. +15V, the VDD supply and the Ground for the supply are shown as red and green banana connectors. A large portion of the PCB, red dashed rectangle, was allocated for circuit development. The PCB is a Full Ground Plane layout. This platform was used in the design and parameter extraction of the device.

Figure 18. DRF100 Test Board

The suggested PCB layout for the DRF100 is illustrated in Figure 18. The external by-passing for the DRF100 Vdd inputs are placed symmetrically on the PCB, and illustrated in the **red** circle. All the supporting driver components must be kept in a close group as illustrated in the Figure. No power DC or RF traces should pass through this area and no control or low voltage power for the DRF100 should pass through the high power RF section.

DRF1200

The DRF1200 is the second in the DRF Series of devices. In the DRF1200 the RF Driver die, used in the DRF100, is combined with a High Voltage RF Power MOSFET. This combination gives the designer an RF Hybrid which allows the control of $\approx 1\text{KW}$ of RF power with $\approx 10\text{W}$ of RF drive (see power calculations section). This is a power gain of $\approx 20\text{db}$. Figure 19 shows the circuit diagram of the DRF1200.



FN	IN	MOSFET
High	High	ON
High	Low	OFF
Low	High	OFF
Low	Low	ON

Table 2

Figure 19. DRF1200 Circuit Diagram

All previous discussions of the DRF100 apply to the input section of the DRF1200. In the following section, the DRF1200 design and testing guidelines are addressed. Table 2 illustrates the truth diagram for the DRF1200.

Figure 20 is an internal view of the DRF1200.

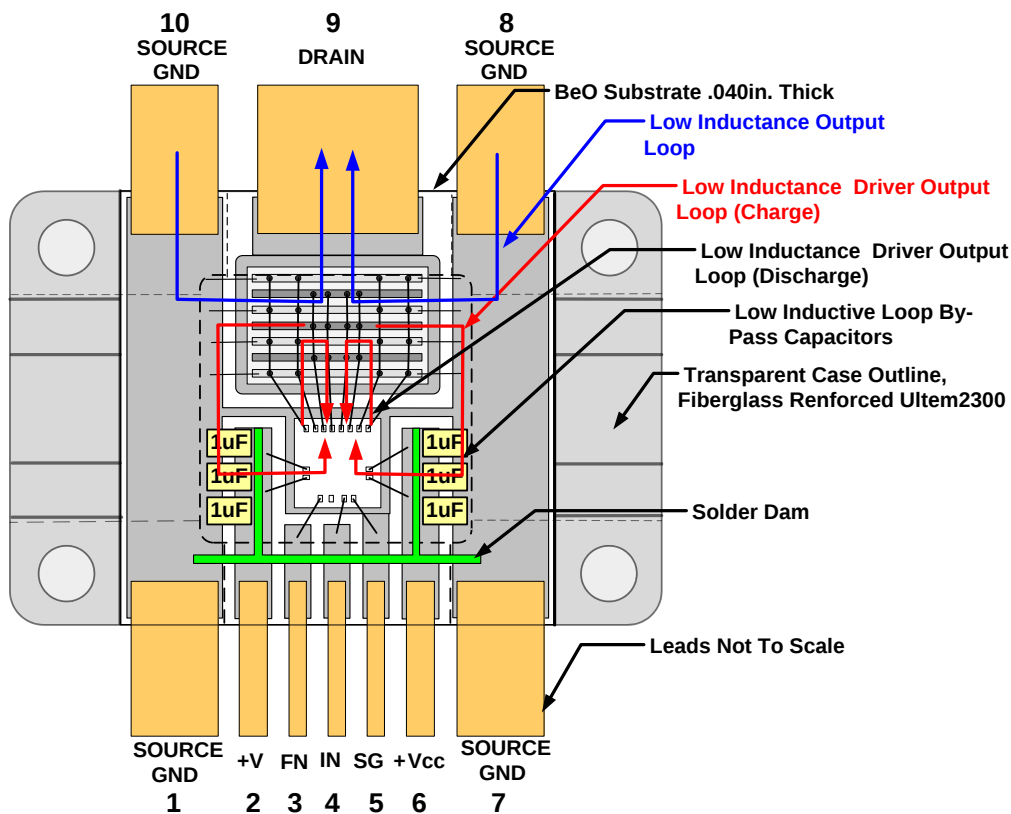


Figure 20. DRF1200 Internal View

There are **three** important features that must be addressed. The **first** is the Driver CI Output Loop, for the MOSFET gate charge and discharge, is illustrated in **red**. Much care has been taken to reduce the magnitude of the inductance between the Driver and the MOSFET. The lower the value of this stray parameter the higher the operating frequency will be.

The Loop is composed of two nested loops, one on the right and one on the left. These current loops are magnetically coupled and form a Coplanar Line. Following the **red** line on the right from the Tail to the Point of the arrow, during Turn-On of the MOSFET, the current flow is from the Source and the power ground, through the By-Pass Capacitors into the Driver IC, then out of the driver IC and into the Gate of the MOSFET. During Turn-Off of the MOSFET, the currents flow in the opposite direction. During both Turn-On and Turn-Off the two currents are forced by topology to flow in opposite directions. Given this flow and the level of the coupling between the two loops, the Inductance is effectively reduced.

The **second**, the MOSFET Output Loops shown in **blue**, operate in the same manner, as the Driver Loops.

The **third**, the compressed layout of components, aids in reducing internal stray inductance.

The combination of these features allows the DRF1200 to have switching speeds of ≈ 5 ns and operate at frequencies of ≈ 30 MHz.

Figure 21 illustrates the schematic diagram of the DRF1200 Test Circuit and Figure 22 the DRF1200 Evaluation Switching Board.

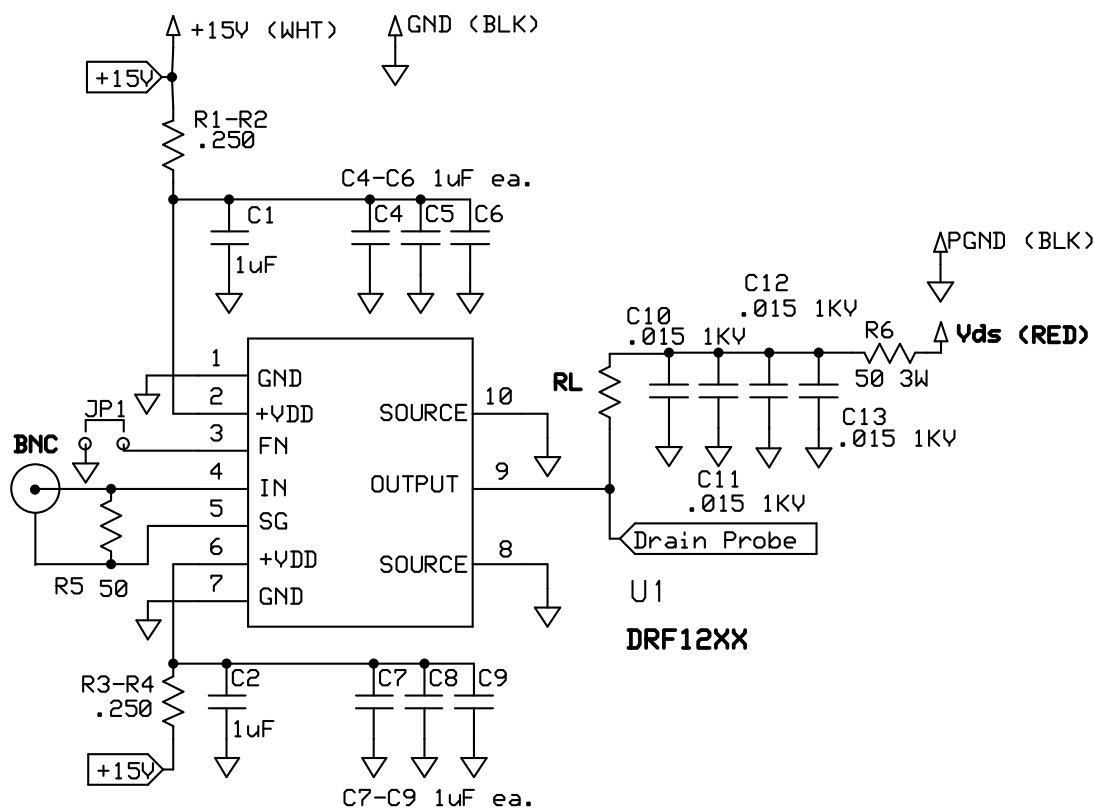


Figure 21. DRF1200 Test Circuit

In Figure 21, the input circuits of the DRF1200 have the same requirements as the DRF100 and therefore are identical. Pin 8 and Pin 10 are the power grounds. It should be noted that Pins 1, 7, 8 and 10 are common points and connected inside of the DRF1200. The Output Pin 9 is connected to the resistor **RL**. The value of this resistor is sized such that when **Vds** is at Maximum, the **Ids** will also be at the specified Maximum. This is true for all DRF Testing.

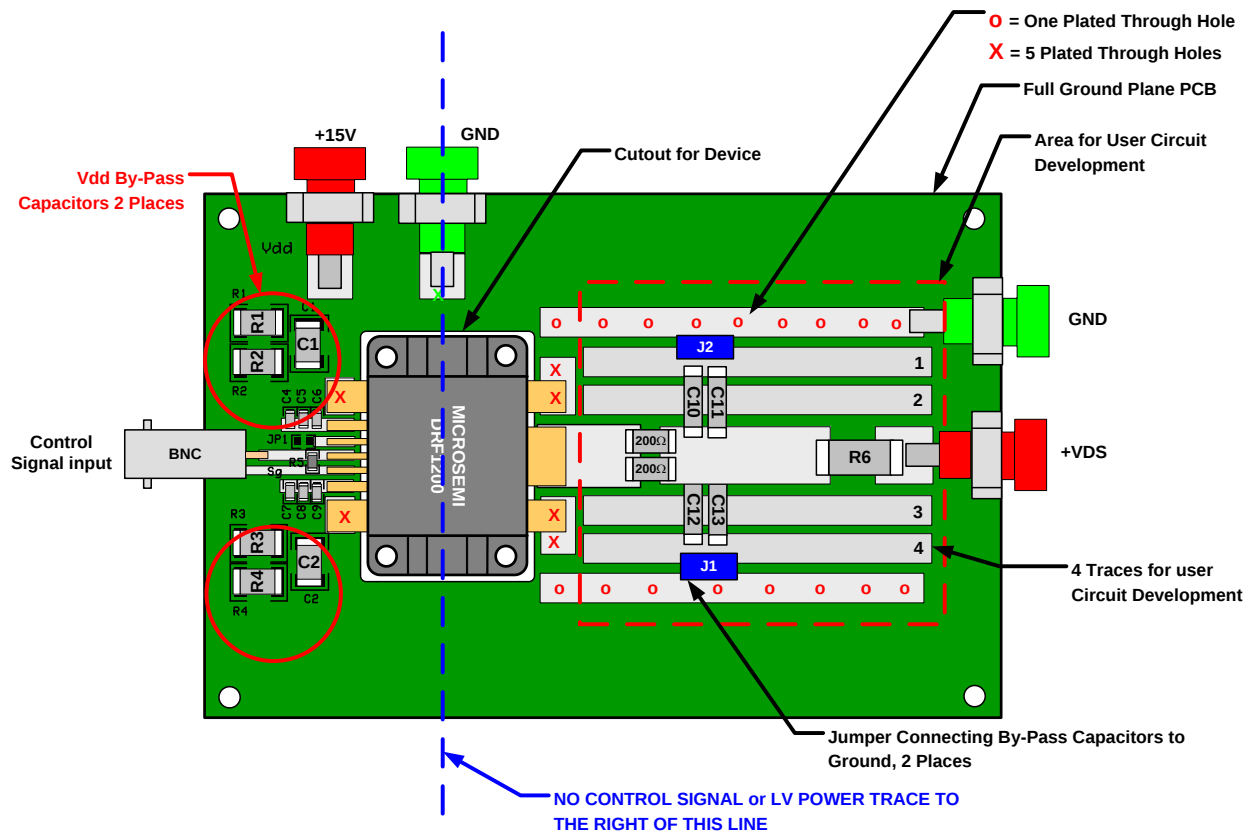


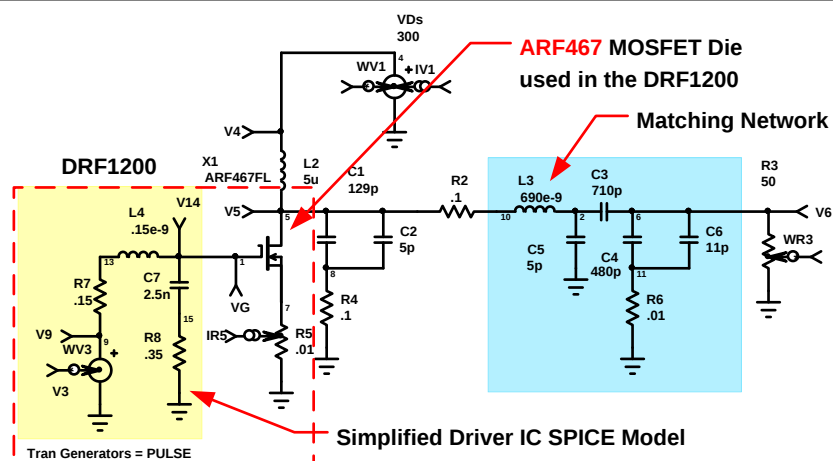
Figure 22. DRF1200 Switching PCB

Figure 22 is the DRF1200 Switching PCB. This layout was used for device characterization. Also illustrated is the suggested PCB layout for the DRF1200 driver input side.

Spice simulations will be used throughout the text for ease of discussion and as an illustrative tool. All circuits discussed have been realized in bench hardware, the models include appropriate strays and predict the bench data with reasonable accuracy.

Figure 23 illustrates the DRF1200 in a Class-E RF Generator circuit (see relevant publications at end of text). The circuit is a Single-Ended, Non-Linear, fixed Frequency design, capable of generating > 1KW of RF output power with 12.1W input power, about 20db gain. The power is most commonly controlled by adjusting the DC Supply (VDs).

Circuit Parameters have been adjusted for the Highest Efficiency and Highest Power Output while limiting the MOSFETs junction temperature to a maximum of $\approx 100^{\circ}\text{C}$ and limiting the Drain to Source Margin to a positive number or zero. These are defined as the Boundary Conditions. This term will be referenced later in the text. All values shown in the following text were acquired with these constraints. The DRF1200 model in Figure 23 is a template for all devices in the DRF series.



Circuit Performance	
Vsupply	+300V
Pout	1252W
Pin	1328W
PLOSS	76W
Eff	94.3%
Pulse Gate Drive	PW=17ns
Ths	45°C
TjX1	91°C
Vds Margin	53V
Drain Z=6Ω	Out Z=50Ω

Table 3

Figure 23. Class-E RF Generator using the DRF1200

Table 3 lists the performance for the RF Generator of Figure 23 which is typical for this topology utilizing the DRF1200 (see Application Note 1811, DRF1200 13.56MHz Reference Design Kit, Microsemi website).

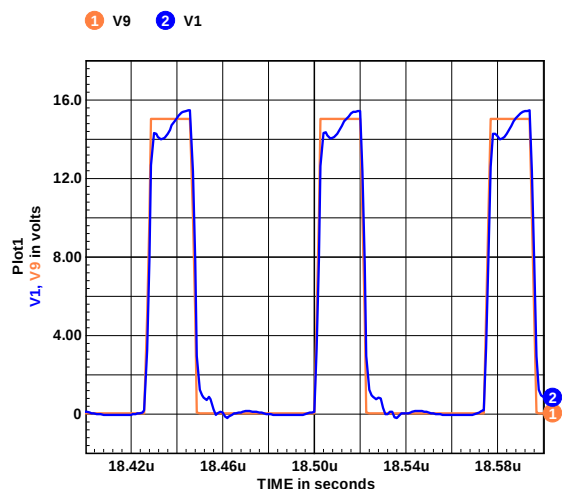


Figure 24. Gate Drive

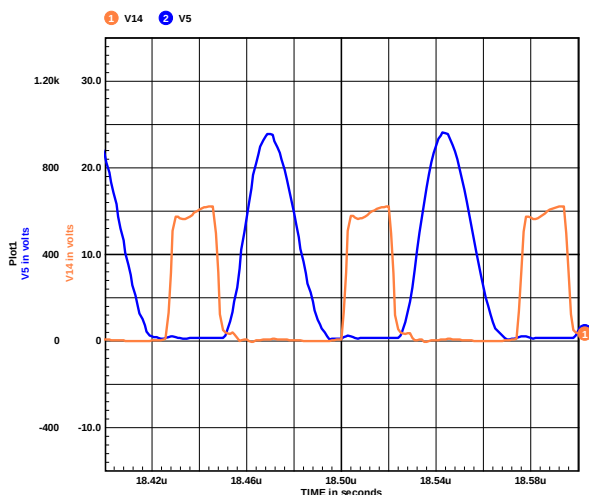


Figure 25. Gate V1 and Drain V5

Figure 24 illustrates the input gate drive at V14 and the signal on the Gate of the Device at (VGs). V9 is the input gate drive and V1 is the signal on the gate structure of the MOSFET die. Circuit stray inductance L4, the Resistance R7, and the Miller Effect are responsible for the distortion of this Square wave input drive.

Figure 25 shows the Gate Drive (V14) and the Drain wave form (V5). The Resonant tank circuit L3, C3 and C4-C6 filter the V5 wave form to create a sine wave output. These components also match the load impedance of 50Ω to the much lower drain output impedance at V5.

DRF1300

The DRF1300 is the third in the DRF Series of devices. In the DRF1300, the RF Driver die used in the DRF100 is combined with a High Voltage RF Power MOSFET in a Push Pull Configuration. This combination gives the designer an RF Hybrid which allows the control of $\approx 2\text{KW}$ of RF power with $\approx 20\text{W}$ of RF drive, this is a power gain of $\approx 20\text{db}$. Figure 26 shows the circuit diagram of the DRF1300.

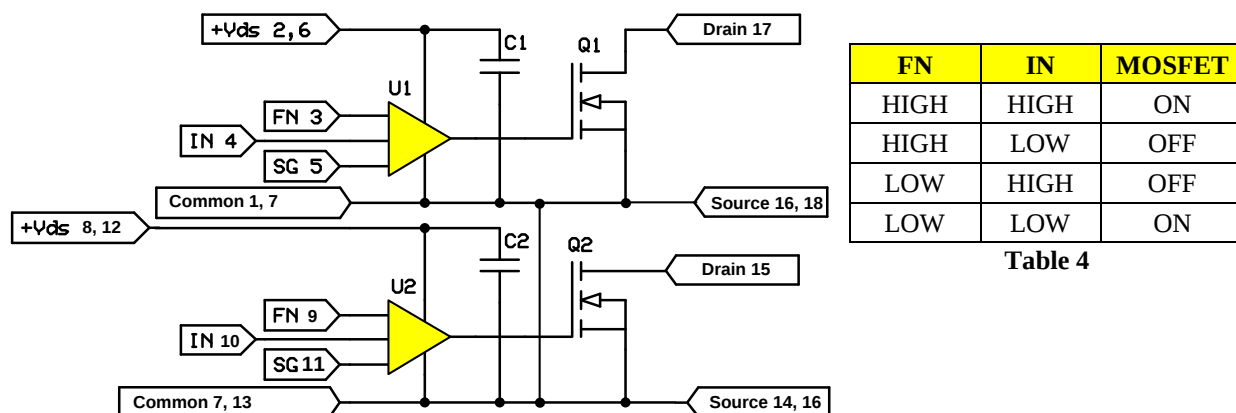
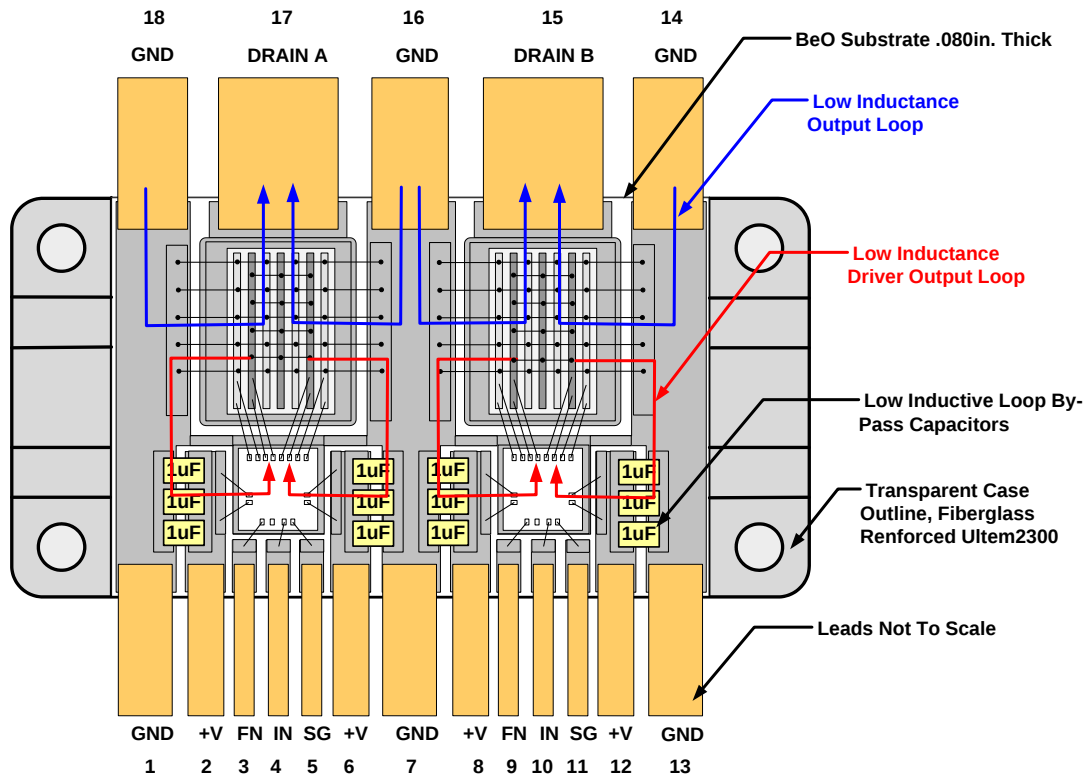


Figure 26. DRF1300 Circuit Diagram

All previous discussions of the DRF100 apply to the input section of the DRF1300. In the following section, the DRF1300 design and testing guidelines are addressed. Table 4 illustrates the truth diagram for the DRF1300.

Figure 27 is an internal view of the DRF1300. The DRF1300 is, in essence, two DRF1200s in the same package; these two devices are completely independent.



DRF1300 Internal View

Figure 27.

There are **three** important features that must be addressed. The **first** is the Driver CI Output Loop, illustrated in **red**. Much care has been taken to reduce the magnitude of the inductance between the Driver and the MOSFET. The lower the value of this stray parameter, the higher the operating frequency will be.

The Loop is composed of two nested loops, one on the right and one on the left. These current loops are magnetically coupled and form a Coplanar Line. Following the **red** line on the right from the Tail to the Point of the arrow, during Turn-On of the MOSFET the current flow is from the Source and the power ground, through the By-Pass Capacitors into the Driver IC, then out of the driver IC and into the Gate of the MOSFET. During Turn-Off of the MOSFET, the currents flow in the opposite direction. During both Turn-On and Turn-Off, the two currents are forced by topology to flow in opposite directions. Given this flow and the level of the coupling between the two loops, the Inductance is effectively reduced.

The **second**, the MOSFET Output Loops shown in **blue**, operate in the same manner as the Driver Loops.

The **third** is that compressing the layout of components further aids in reducing internal stray inductance.

The combination of these features allows the DRF1300 to have switching speeds of ≤ 5 ns and operate at frequencies of up to 30MHz.

The DRF1300 is assembled with adjacent MOSFET die and adjacent driver die. This means that the two MOSFET die are selected based on their location on the silicon wafer, side-by-side. This will not provide an exact match of functional parameters but very close. The driver dies are selected in the same manner with similar results. Overall the DRF1300 will have all parameters of the left side and the right side of the device nearly a match.

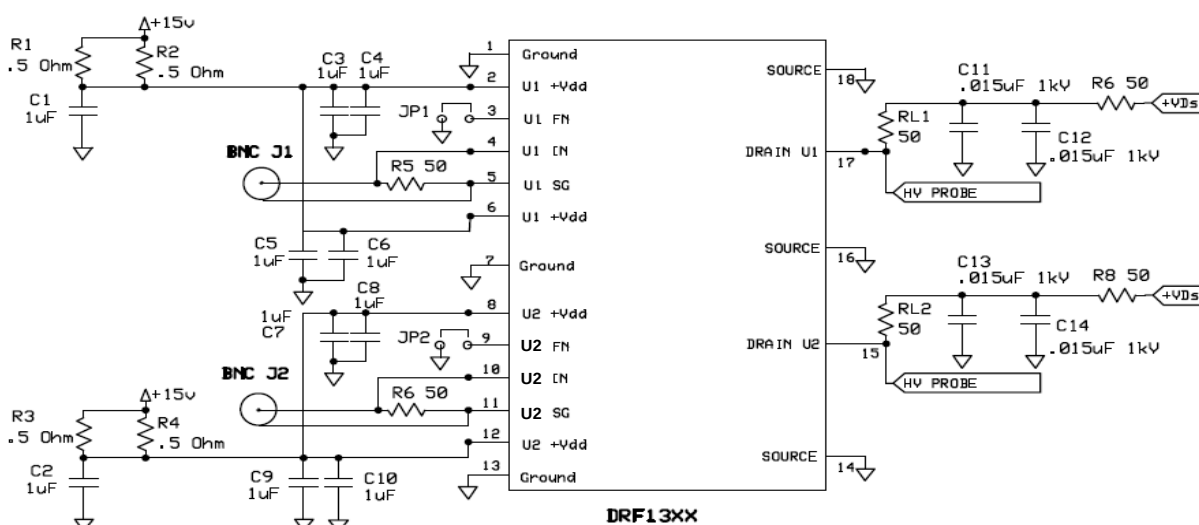


Figure 28. DRF1300 Test Circuit

Figure 28 is a schematic diagram of the DRF1300 Test Circuit. A 5V max signal input is applied to either J1 or J2. Using the Signal Ground (SG) for the BNC shielding provides a Kelvin connection for the input increasing noise immunity. The driver supply from the +15V (VCC) input is applied to U1 Vdd pins 2 and 6 that are both externally and internally connected to help balance pulse currents in the hybrid. The same applies for U2 Vdd pins 8 and 12. U1 section and the U2 section do not share an internal power connection. Connecting the Jumper JP1 will cause the U1 side of the DRF1300 to operate in the Inverting mode, while JP2 provides this function for the U2 side. The output sections as configured have 50Ω resistive pull-up circuits with on board filtering for the High Voltage power supply. Electrical performance data is captured with a test circuit similar to Figure 29.

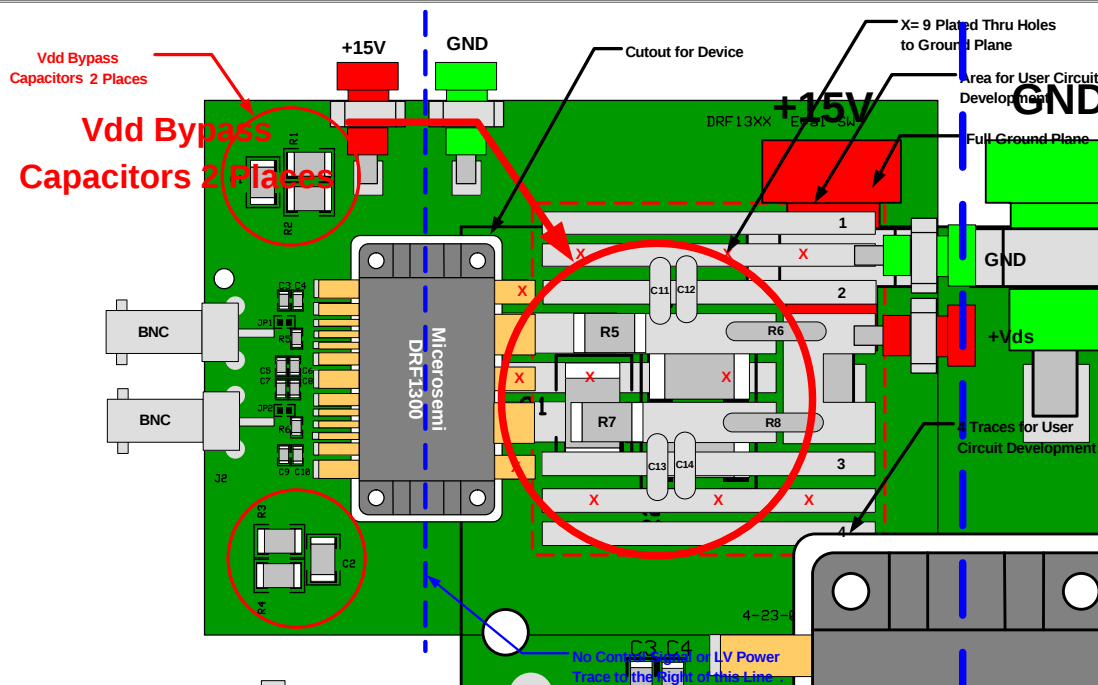


Figure 29. DRF1300 Evaluation Switching

Figure 29 is an illustration of the DRF1300 Evaluation Switching PCB. The user configurable area is illustrated by the dashed red line. For example, this area can be modified to be a Push-Pull Class-D RF Generator.

DRF1300 Push-Pull RF Generator 2.8KW

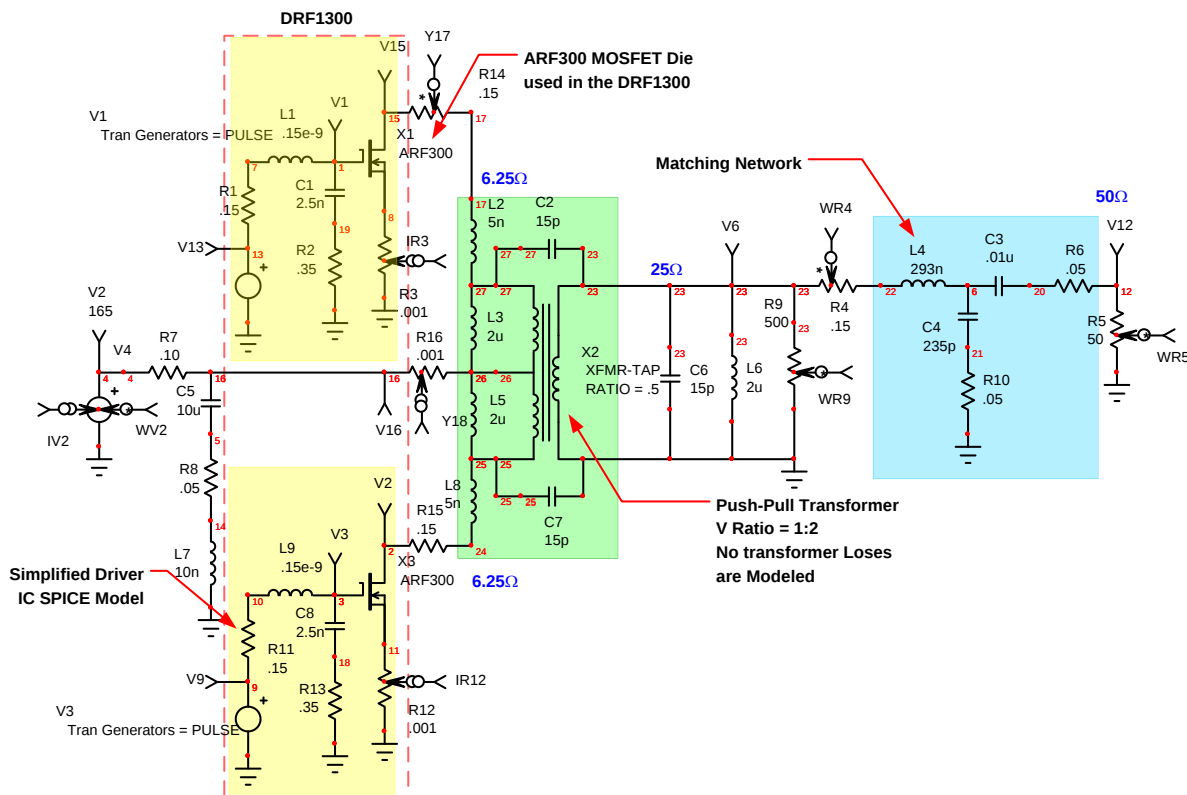
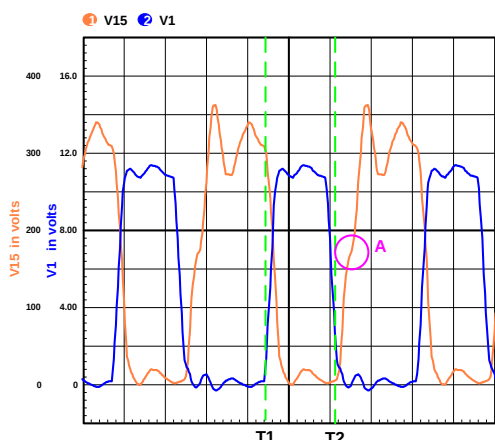
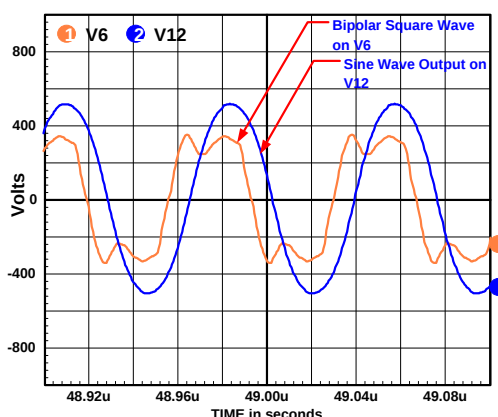


Figure 30. DRF1300 Push-Pull RF Generator

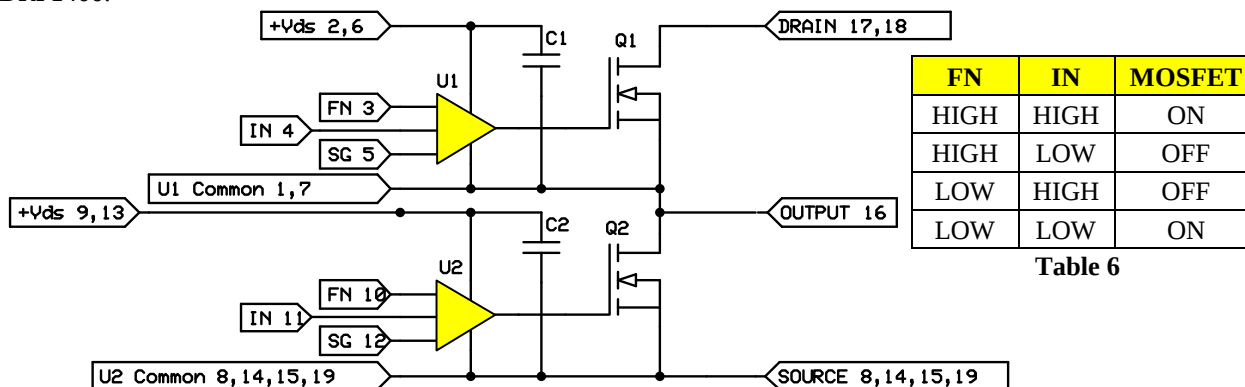
Figure 30 illustrates the DRF1300 in a push-pull Class-D circuit configuration. Table 5 lists the performance. In this mode of operation, the MOSFETs X1 and X3 are gated in an alternating pattern. This applies power to alternate windings of the transformer X2. The transformer primary to secondary ratio is 1:2, which translates to a reduction of 4:1 in impedance, Load to MOSFET Drain, 50Ω Load to 6.26Ω Drain. The RF Driver IC is modeled in Figure 30 in the yellow highlighted areas, X1 for the High Side Switch and 3X for the Low Side switch. The largest difficulty in a push-pull Class-D circuit design is the design of the transformer. This is also true for the SPICE model. In a push-pull Class-D circuit configuration, it should be noted that the simulations are less precise due to the transformer model. This being said, the circuit model is still instructive for the completeness of understanding. Figure 31 shows the Gate and Drain waveform timing. Illustrated at (A) on the Drain waveform is a small discontinuity in the Rate of Rise, which is the result of slightly more inductance than necessary for resonance. However this small inductance makes a noticeable increase in Efficiency, see Application Note 1808. T1 and T2 illustrate the gate on time. Figure 32 illustrates the relationship between the nDrain waveform and the RF sine wave on the output load R5.

Circuit Performance	
Vsupply	+165V
Pout	2859W
Pin	3459W
PLoss	561W
Eff	83.6%
Pulse Gate Drive	PW=25ns
Ths	25°C
Tj X3	101°C
TjX1	101°C
Vds Margin	138V
Drain Z=6Ω	Out Z=50Ω

Table 5

Figure 31. Gate and Drain Waveforms

Figure 32. Transformer and Output Waveforms

DRF1400

The DRF1400 is the fourth in the DRF Series of devices. In the DRF1400, the RF Driver die used in the DRF100 is combined with two High Voltage RF Power MOSFETs in a Half Bridge Topology. This combination gives the designer an RF Hybrid which allows the control of $\approx 5\text{KW}$ of RF power with $\approx 20\text{W}$ of RF drive. This is a power gain of $> 24\text{db}$. Figure 33 shows the circuit diagram of the DRF1400 and Table 6 illustrates the truth diagram for the DRF1400.


Figure 33. DRF1400 Circuit Diagram

FN	IN	MOSFET
HIGH	HIGH	ON
HIGH	LOW	OFF
LOW	HIGH	OFF
LOW	LOW	ON

Table 6

The DRF1400 is assembled with adjacent MOSFET die and adjacent driver die. This means that the two MOSFET die are selected based on their location on the silicon wafer, side-by-side. This will not provide an exact match of functional parameters but very close. The driver die are selected in the same manner with similar results. Overall the DRF1400 will have all parameters of the left side and the right side of the device nearly a match.

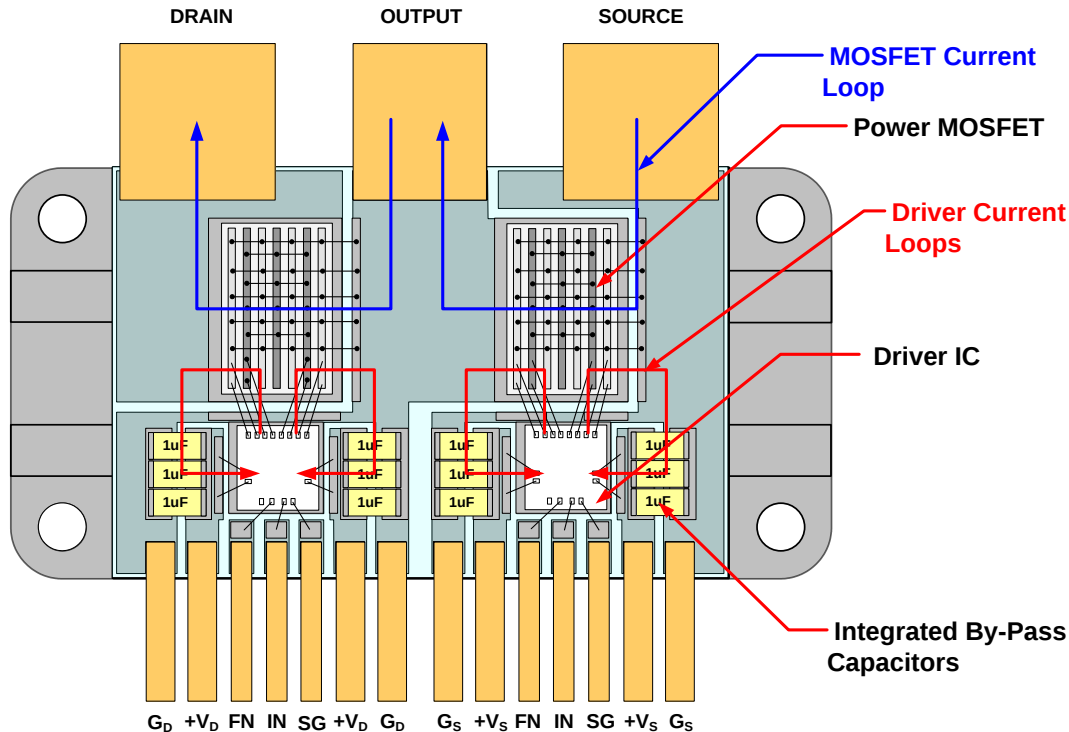


Figure 34. DRF1400 Internal View

Figure 34 is an internal view of the DRF1400, the Half Bridge topology in the DRF Family. The input Driver and MOSFET circuitry are virtually identical to the DRF1200. The current loops are magnetically coupled and form a Coplanar Line. Following the **red** line on the right from the Tail to the Point of the arrow, during Turn-On of the MOSFET the current flow is from the Source and the power ground, through the Bypass Capacitors into the Driver IC, then out of the driver IC and into the Gate of the MOSFET. During Turn-Off of the MOSFET the currents flow in the opposite direction. During both Turn-On and Turn-Off, the two currents are forced by topology to flow in opposite directions. Given this flow and the level of the coupling between the two loops, the Inductance is effectively reduced as in DRF1300. However, the MOSFET Output Loops shown in **blue** do not operate in the same manner as the DRF1200 and DRF1300. Here, there is no symmetry, which leads to increased inductance in the drain source loop. This increased inductance is offset by the typically high voltage operation of the Half Bridge Topology. In addition this inductance will subtract from the value of the Output Network Inductor (see output network on Page 24). The DRF1400 is capable of switching speeds of ≤ 5 ns and operate at frequencies of up to 30MHz.

The Half-Bridge circuit topology

The Half-Bridge circuit topology offers the highest forward launched RF power for a given amount of silicon of any ISM RF power topology. However there are downsides to utilization of this configuration. The Half Bridge is complex, requires a very stable high side controller, and can operate at drain voltages approaching 800V. At this operating point, component selection can become extremely critical.

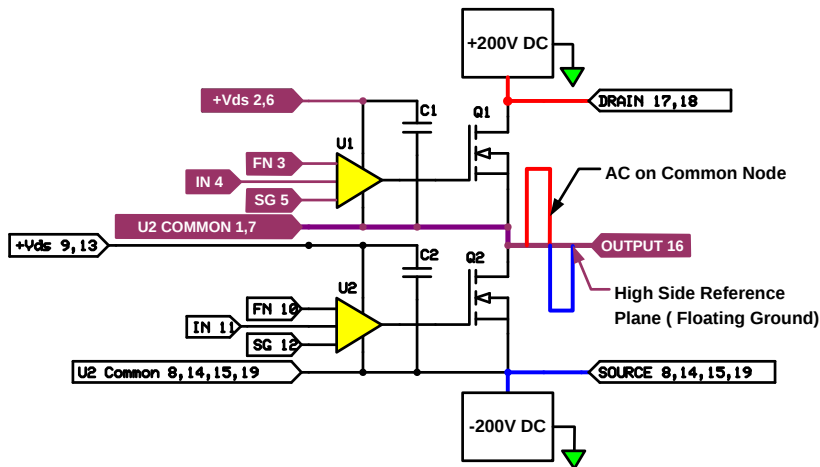


Figure 35. Half-Bridge

Using this circuitry we will look at the critical circuit areas. The most troublesome area is maintaining control of the high side switch. Referring to Figure 35 we see that the Power Output (pin 16) Node in the circuit (shown in purple) is also the signal reference plane (Floating Ground) for all the driver inputs (pin 1, 2, 3, 4, 5, 6 and 7). We will see in the following text that we will need about -50db CMR to maintain control of the high side switch.

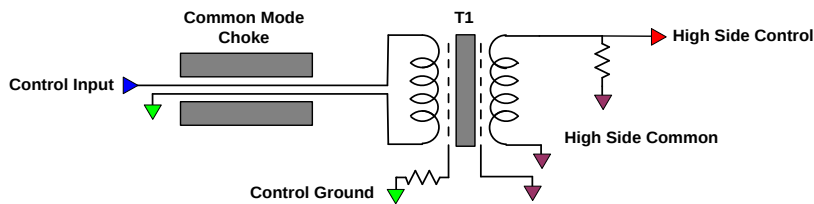


Figure 36. Isolation Transformer

The Isolation Transformer is the first and simplest approach for isolation and control. Fiber-Optics are somewhat easier to implement and have very high CMR. The cost is higher, however assembly is less problematic. For this discussion we will start with the Isolation transformer approach.

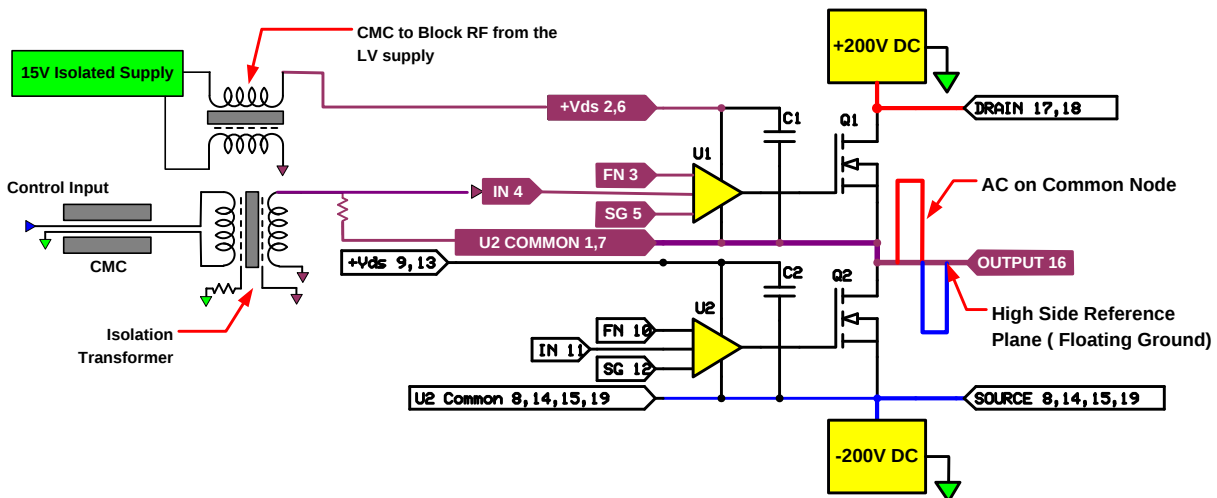


Figure 37. Half Bridge with Control signal and Support Power

Figure 37 illustrates the Half Bridge of Figure 35 with the addition of the Isolation Transformer of Figure 36. We have also included a CMC installed in the Low voltage power path. The Half Bridge of Figure 37 now includes the three elements which require the most understanding and the most attention to detail. The isolated 15V supply will isolate a DC potential a DC of 1KV from the secondary. However we must also provide isolation from the RF square wave at the Output pin 16. This is accomplished with the insertion of a CMC in the DC path, Figure 37 upper left. The input control Isolation Transformer, shown in Figure 37, must also have a CMC. Both the CMC and the Isolation Transformer will be discussed in more detail.

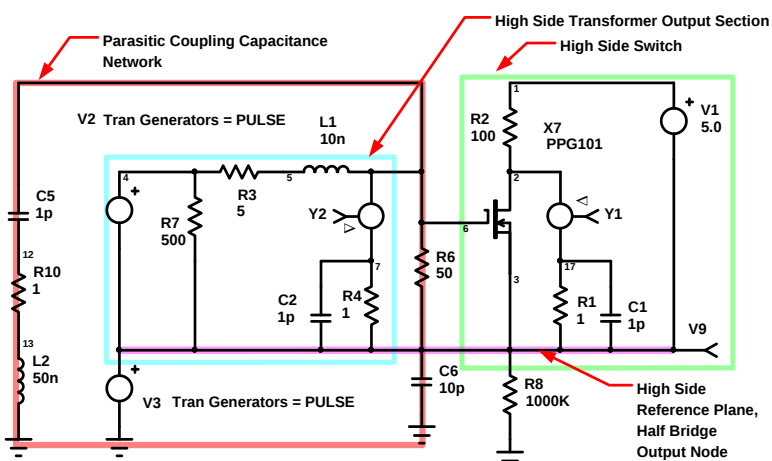


Figure 38. Parasitic Coupling Capacitance

Figure 38 illustrates the Parasitic Coupling Capacitance Network in the Isolation Transformer, highlighted in **red**, the secondary of the Control Signal Coupling Transformer in the **blue** highlighted box, and the High Side Switch Driver in the **green** highlighted box. The Parasitic Coupling Capacitance Network models the coupling from the primary of the transformer to the secondary. With a very modest capacitance at C5, the circuit can lose stability. This will be catastrophic for the Half or Full Bridge circuit.

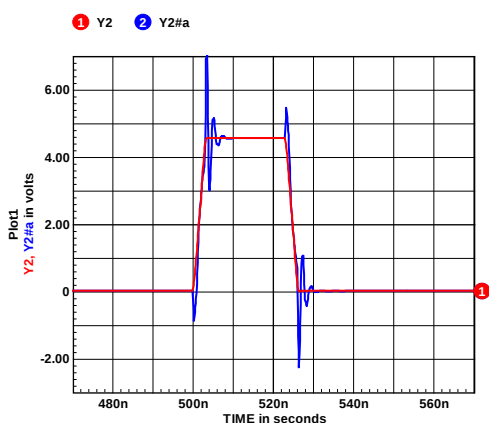


Figure 39. Y2 High Side wave form

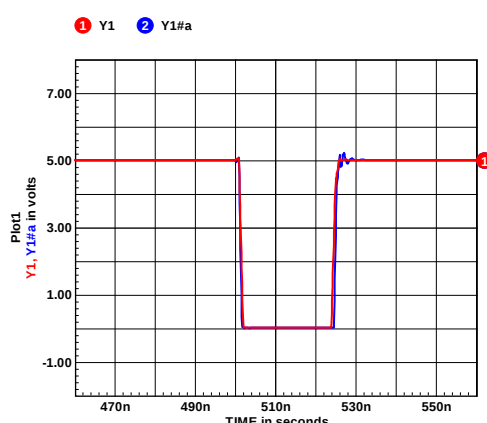


Figure 40. Y1 High Side wave form

In Figures 39-40 we see the effect of the Parasitic Coupling from the Ground Plane to the high voltage Reference Plane which is the output node of the Half Bridge. This coupling forces a current through the Parasitic Network Loop, highlighted in **red** and shown in Figure 38. The **red** trace is the Y2 signal with no parasitic coupling; the **blue** trace is the Y2 signal with the parasitic coupling. The level of coupling is just beginning to affect the control signal at Y1 illustrated in Figure 40, with a C5 value of 0.25pF. This signal is about -51db from the Half Bridge output level.

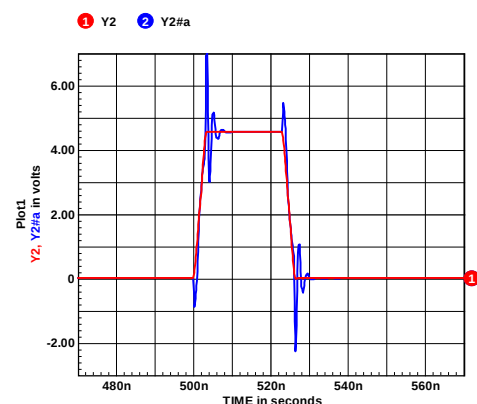


Figure 41. Y2 High Side wave form

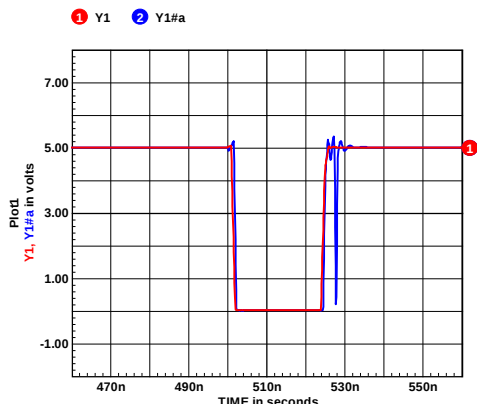


Figure 42. Y1 High Side wave form

The level of coupling in Figure 41 is now clearly affecting the control signal at Y1 illustrated in Figure 42, which is at -48.9db from the Half Bridge output level, with a C5 value of 0.5pF. At this point, the circuit is cross-conducting.

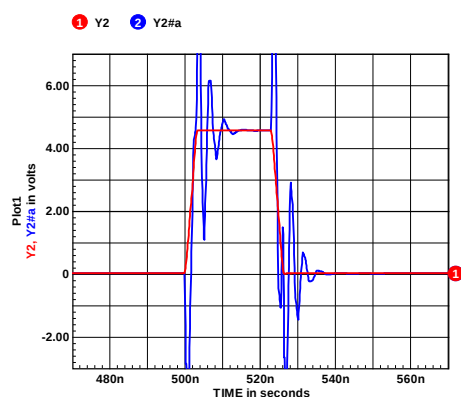


Figure 43. Y2 High Side wave form

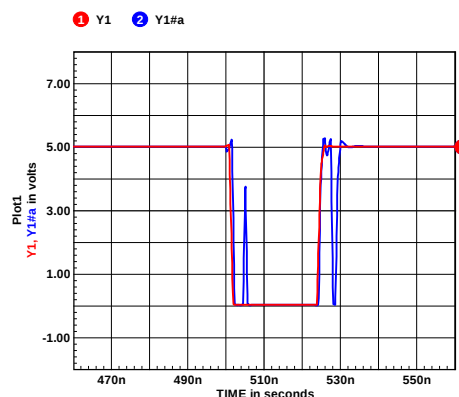


Figure 44. Y1 High Side wave form

The level of coupling in Figure 43 is now seriously affecting the control signal at Y1 illustrated in Figure 44. This is at -45.3db from the Half Bridge output level, the value of C5 is now 1pF. The circuit is now cross-conducting on both the leading edge and the trailing edge.

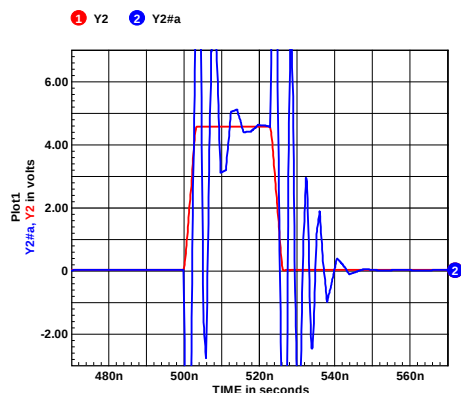


Figure 45. Y2 High Side wave form

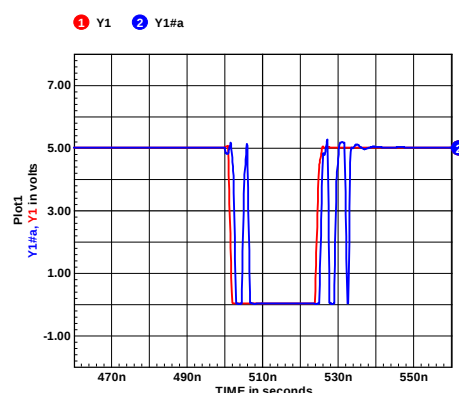


Figure 46. Y1 High Side wave form

The level of coupling in Figure 45 has completely disrupted the control signal at Y1 illustrated in Figure 46, which is at -38.8db from the Half Bridge output level. The value of C5 is now at only 2pF. The circuit now is oscillating and the switching devices most likely have been destroyed. This sequence of wave forms clearly shows that in order to maintain system control in the RF Half Bridge we must be extremely careful in the Design and Implementation of the isolated control circuitry. Keeping this Parasitic Capacitance as low as practical and the addition of Common Mode Chokes can mitigate this potentially serious problem.

Common Mode Rejection

In order to maintain system control in an RF Half Bridge as illustrated in the preceding Figure 37, we must be extremely careful in the Design and Implementation of the isolated control circuitry. Keeping the Parasitic Capacitance of the Isolation Transformer as low as practical and the addition of Common Mode Chokes can help.

Figure 47 Illustrates a DC Isolated Transformer and Common Mode Choke input.

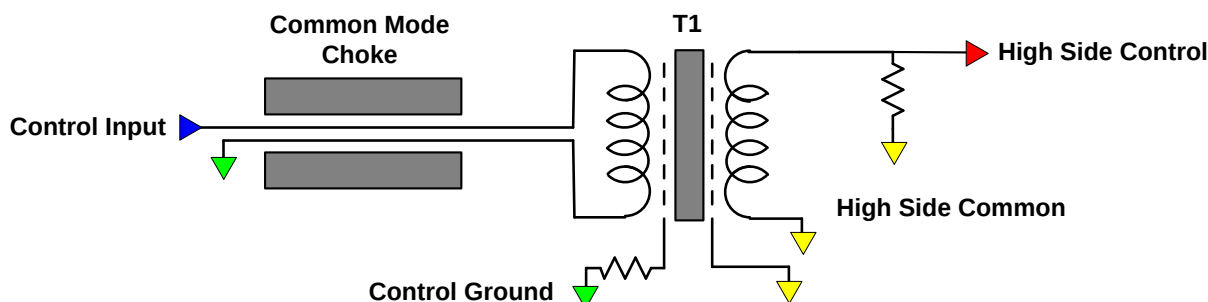


Figure 47. Ground to High Side Control

The Gate Drive is a +15V Pk pulse. This is coupled through T1 and applied to the High Side control, see Figure 47. The Signal at this point is Bi-polar, a positive pulse with a DC offset proportional to the Pulse Width and the Duty Cycle. Transformer coupling and CMCs were chosen for simplicity. T1 incorporates two electro static shields. These effectively shunt the capacitive coupling to ground and improve the CMR, however they make the transformer very difficult to build.

Common Mode Chokes (CMC)

Constructions of the CMC's are illustrated in Figure 48. The CMC on the left should be used for both the +15V input and the +HV V_{DS} input. These lines are tightly twisted pairs (5-8 twists per inch). The CMC on the right should be used for the control signal Input and on the Scope Probe Cable, when making measurements. Three to five turns on each is sufficient. The CMC's should be placed as close to the circuit as practical.

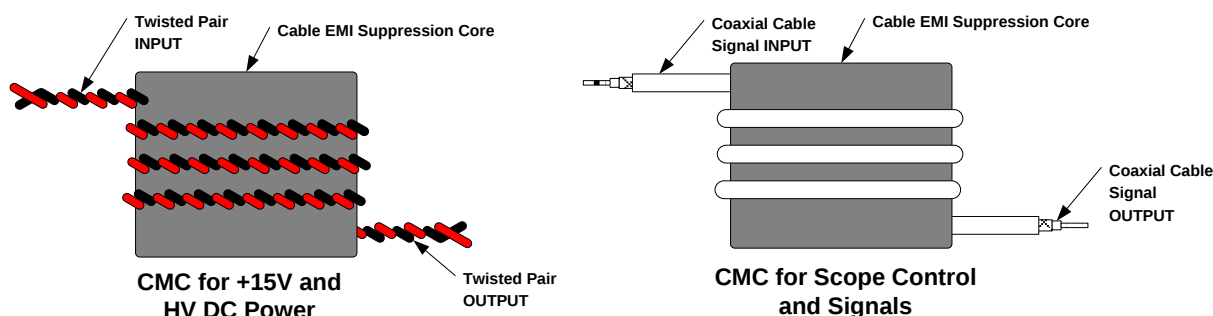
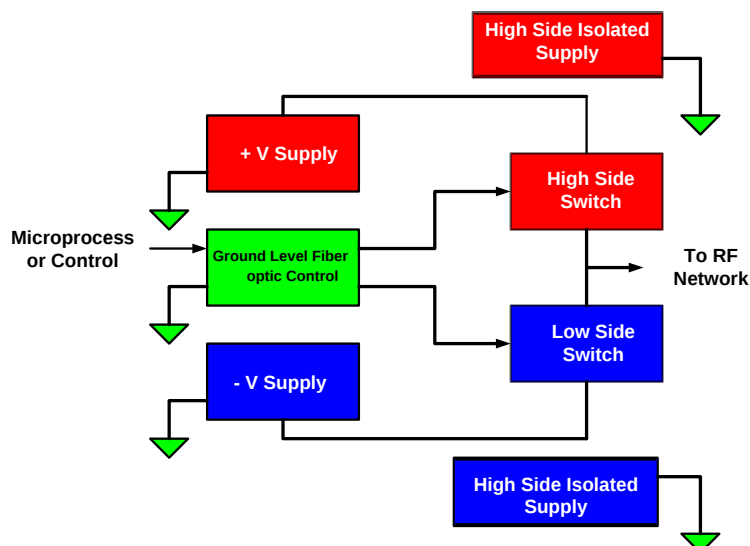


Figure 48. Common Mode Choke (CMC)
FairRite part number 0431164181

The suppression of the 400-800V Common Mode Signal on the High Side Control to the Driver Circuit Input must be on the order of -51 db for stable operation. For high power Half Bridge RF Generators, the Common Mode Signal Slew Rate can be $\geq 100\text{KV}/\mu\text{s}$ at the high side Reference Plane. This rules out the use of low-cost Opto-isolators. This would seem to indicate that we are relegated to the use of a transformer, however this is not the case. With the modern innovations in fiber optic devices, and the reduction in cost, they are now an appealing choice to address the High Common Mode requirements of the High Power Half Bridge, and the cost is in the same area as the transformer solution. Illustrated in Figure 49 is a High Power Half Bridge utilizing a Fiber Optic Link for control of the High Side Switch. It is suggested that two identical links be used, as opposed to a slower, cheaper link for the low side switch. This maintains the Phase of the two control signals. Low Voltage supplies are not shown.



In Figure 49 the Microprocessor applies the control signals to the two fiber optic links. One assigned to the High Side switch and the other the Low Side switch. With this method of signal control, all ground loops are severed and the High CMR of the Optical Link provides stable control signals to the High Side switch. One could use a cheaper optical link for the Low Side switch; however threshold, delay and thermal drift parameters may be difficult to match. It is best to use the same link for both controls.

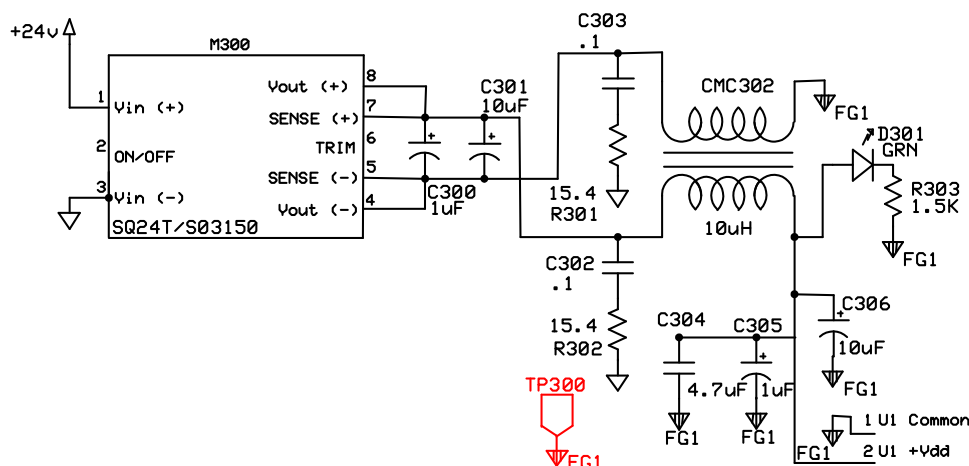


Figure 50. DC-DC Supply

Referring to Figure 50, M300 is a Switch Mode DC-DC converter that supplies +15V at 1.5A for the Driver when operating at 13.56MHz. It also has 1KV DC isolation. The low voltage DC power path for FG1 is through CMC302 and is filtered by C303, R301 and C302, R302. DC isolation for the FG1 plane is via the DC-DC power supply M300. C304, C305 and C306 provide local by-passing for U1 on the FG1 plane. This allows the DC to DC converter to remain stable while the FG1 plane is slewing from +Vds to -Vsd. The operation of the DC-DC Supply for FG2 is in the same manner.

N Channel – N Channel Half Bridge

Figure 51 illustrates a classical N Channel - N Channel Half Bridge RF Generator. The High Side Switch X2 and the Low Side Switch X1 form the two active devices in the Half Bridge. X1 and X2 commute in an alternating fashion providing a pseudo Square Wave drive to the input of the RF Network at V1. The RF network provides an impedance match from the Drain Impedance of X1, X2 of about 3Ω to the 50Ω load, via an L Match Network, L4 and C3. This network is also resonant at 13.56MHz so that the output at V8 is a Sine Wave. It should be noted that the network only performs the impedance translation at the design frequency. The common design formulas account only for a resistive source and load. Since the output devices have parasitic capacitance, the network design must be modified to account for the stray capacitance. This is done with the addition of a series inductance (L7). A value of $L7 \approx 10\%$ to 25% higher than the calculated is typically required to bring the network to full efficiency. Circuit performance is shown in Table 7.

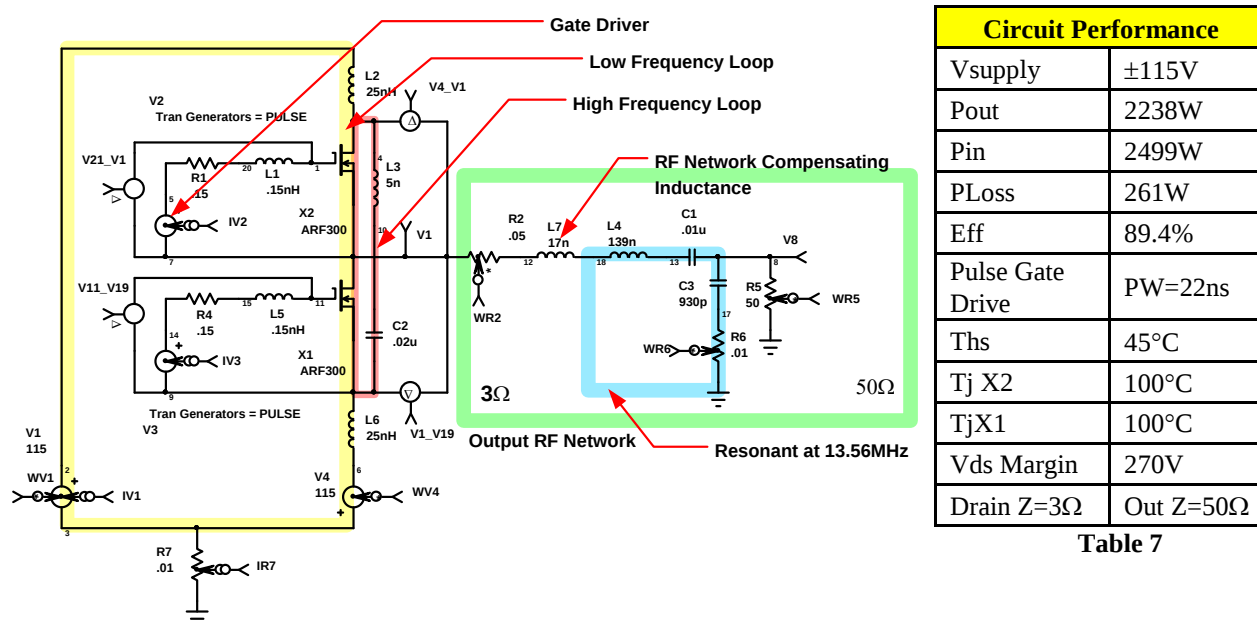


Figure 51. N - N Channel Half Bridge

The Half Bridge Circuit Topology of Figure 51 contains two current loops. A low frequency loop is highlighted in yellow, and the High Frequency Loop is highlighted in red. These loops are illustrated with near-minimum stray inductance. Great care should be taken to achieve inductance values near the illustrated values. If we allow L2 and L6 to reach 100nH or greater, performance will be degraded. The inductance of the Inner Loop, L3, is a very Critical Stray Component. Values greater than a few nH can cause stability problems and excessive harmonics. Shown in Table 8 are a set of values for variations in the three Stray Inductive terms, L2, L3 and L6 and the impact on circuit performance.

Table 8. L2, L3, L6 Variations

L2, L3, L6	L2=25nH L3=5nH L6=25nH	L2=100nH L3=20nH L6=100nH	L2=250nH L3=50nH L6=250nH
Vsupply	±115V	±173V	±235V
Pout	2238W	1856W	816W
Pin	2499W	2116W	1060W
PLoss	261W	260W	244W
Eff	89.40%	87.7%	77.0%
Pw	26ns	26ns	26ns
Ths	45°C	45°C	45°C
Tj X2	100°C	100°C	96°C
TjX1	100°C	100°C	96°C
Vds Margin	270V	139V	5V

For Columns 2, 3 and 4, Circuit Parameters have been adjusted for the Highest Efficiency and Highest Power Output while not exceeding the Boundary Conditions as stated in the Introduction. If we allow L2 and L6 to reach 100nH or greater, performance will be degraded. Power Output Capability and Efficiency are reduced significantly. The inductance of the Inner Loop, L3, is a very Critical Stray Component. Values greater than a few nH can cause stability problems and excessive harmonics.

Designing A Half Bridge Output Network

Generally, the output impedance of the half bridge – the load that will accept the maximum amount of power from it – is nowhere near the typical 50Ω used for power measurement and coaxial cables. A tuned matching network is used to change the output impedance of the amplifier to 50Ω.

The transistors are not ideal devices, they have a finite output capacitance, C_{oss} . This causes the half bridge's output impedance to be slightly capacitive. This is important to consider, but it can be easily accommodated by the output network if the first tuning element is a series inductor, which is usually the case.

The output impedance is calculated from the operating voltage and the allowable level of stress on the transistors. If, for instance, the operating supply is 200 volts rail-to rail and the desired output power is 1kW, the output impedance is calculated by Equation 1. So $R_L = 40\Omega$.

$$\text{Equation 1. } R_L = \frac{V_{dd}^2}{P_{OUT}}$$

The C_{oss} is essentially in parallel with this output impedance. If the C_{oss} is 200 pF and the operating frequency is 13.56 MHz, the output impedance is the parallel combination of R_L and $X_{C_{oss}}$ or $40\Omega // -j58.7\Omega$. Converting this to an equivalent series impedance gives $R_L = 27.3 - j18.6$. This is the “output impedance” of the amplifier that must now be matched to 50Ω.

Since the output of a class D amplifier contains a high amount of harmonic energy, it is convenient to employ a matching network that is also a lowpass filter. The simplest network that will fulfill this requirement is an L-network consisting of a series inductor and a shunt capacitor.

The first element in the matching network is an inductor that cancels the series capacitive reactance caused by C_{oss} . Its reactance is $+j18.6\Omega$ at 13.56 MHz or 218 nH. Now the network is calculated in Equation 2.

$$\text{Equation 2. } X_L = R_2 \sqrt{\frac{R_1}{R_2} - 1} \quad \text{and} \quad X_C = R_1 / \sqrt{\frac{R_1}{R_2} - 1} = \frac{R_1 R_2}{X_L}$$

R_1 must always be greater than R_2 . Here R_1 is the load (typ 50Ω) and R_2 is the real part of the output impedance, 27.3Ω in our example. So the series inductance is $j24.9$ or 292 nH, and the shunt capacitor is $-j54.8$ or 214 pF.

The final network is the combined inductors, $(218+292) = 510$ nH, in series with the output and the shunt capacitor of 214 pF in shunt with the output. There is one more element required. This is the blocking capacitor. It does not form part of the matching network, but is needed to make sure there is no DC voltage on the output connector. It can be placed in series with the inductor so as to reduce the stress on the output shunt capacitor. It must be a low loss type because it carries the full output current of the generator, given by Equation 3.

$$\text{Equation 3. } I_o = \sqrt{\frac{P_{out}}{R_L}} \text{ or } 6A.$$

	A	B	C	D	E	F	G	H
1	L-Network Calculator							
2	RL	Rs	XLs	XCp	Q	F MHz	L nH	C pF
3	Enter RL	Enter RS	=B3*E3	=A\$3/E3	=SQRT((A\$3/B3)-1)	Enter MHz	=1000*C3/(2*PI()*F3)	=1000000/(2*PI()*F3*D3)

Table 9. Excel L-Network Calculator

Table 9 is an instructive tool for the investigation of the network design, the circuit efficient and power output.

Low Frequency Loop, High Frequency Loop and Stray Inductance

Recall Table 8. Stray Inductance in most cases is detrimental to circuit performance. For the HB circuit configuration we included a table with three sets of stray inductances. The preferred is Set (1), 25nH, 5nH, 25nH. Set (2), 100nH, 20nH, 100nH is usable but not advised and Set (3), 250nH, 50nH, 250nH is not acceptable,

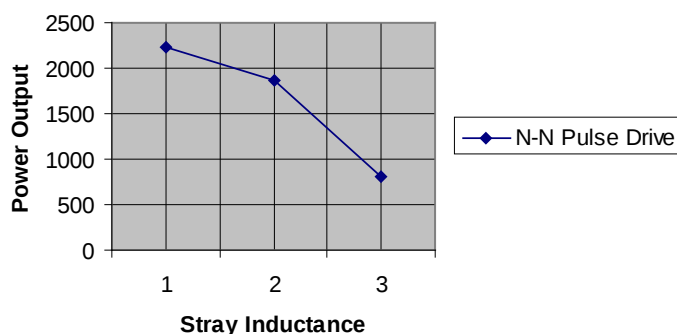


Figure 52 illustrates Power Output vs. Stray Inductance. For Sets 1, 2 and 3 the Power Output is reduced by well over a 1000W.

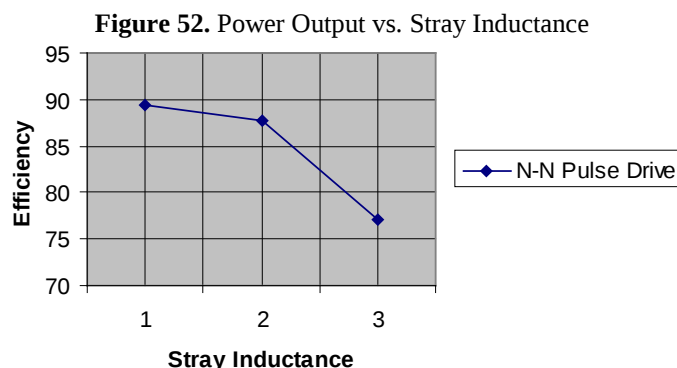


Figure 52. Power Output vs. Stray Inductance

Figure 53 illustrates Efficiency vs. Stray Inductance. For Set 2 the Efficiency is reduced by $\approx 5\%$, and for Set 3 by $\approx 14\%$

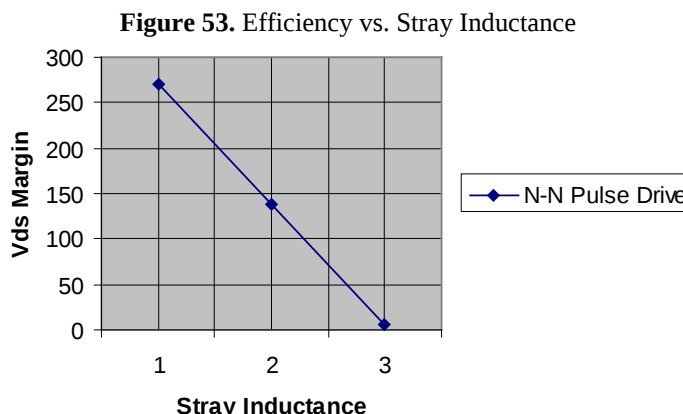


Figure 53. Efficiency vs. Stray Inductance

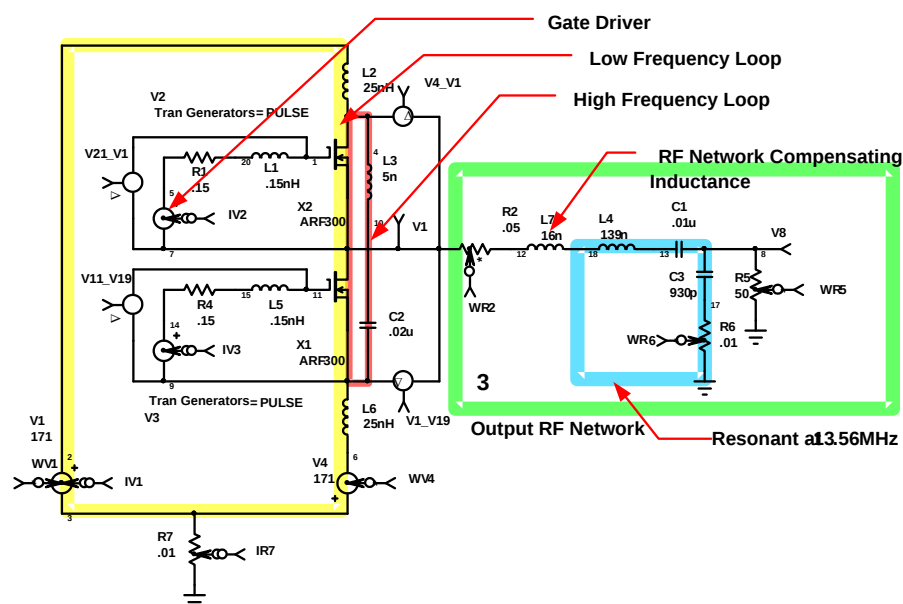
Figure 54 illustrates Vds Margin vs. Stray Inductance. The Vds Margin is reduced by almost 100V for Set 2, and by over 200V for Set 3.

Figure 54. Vds Margin vs. Stray Inductance

Figures 52, 53 and 54 illustrate the value of taking great care in the minimization of the Stray Inductance in the Low Frequency and the High Frequency loops shown in the preceding text.

High Power

Circuit Parameters, for Figure 55, have been adjusted for the Highest Efficiency and Highest Power Output while limiting the MOSFETs junction temperature to a maximum of $\approx 125^{\circ}\text{C}$ and limiting the Drain to Source Margin to a positive number or zero. These are defined as the Boundary Conditions all values shown in the following text were acquired with these constraints, see Table 10.



Circuit Performance	
Vsupply	$\pm 171\text{V}$
Pout	5001W
Pin	5693W
PLoss	593W
Eff	89.6%
Pulse Gate Drive	PW=26ns
Ths	45°C
Tj X2	125°C
TjX1	125°C
Vds Margin	155V
Drain Z=3 Ω	Out Z=50 Ω

Table 10

Figure 55. N - N Channel Half Bridge

Figure 55 is very similar to Figure 51 on Page 24, however we have changed the Boundary Conditions. We have allowed the Junction Temperature to rise to 125°C , and the Power Output to rise to 5.01KW. This is not an unreasonable operating point provided that the load is a 50 Ω Flat Line. Once we change the load, Power must also be altered to maintain the output devices X1 and X2 at a Tj of less than 125°C or we may damage the MOSFET devices. Carrying this further, we can combine two Half Bridges to get 10KW. In Figure 56 we combine four modules to get 20KW RF Output at 13.56MHz

More Power

Figure 55 illustrates a 5KW N Channel Half Bridge at 13.56MHz. In Figure 56 we have added two MOSFETs and formed a new Series Array Half Bridge. This type of Half Bridge can be constructed to $> 10\text{KV}$ Series Array Half Bridge with 2MW peak power. As the Power and the Voltage increase, the working circuit becomes more and more difficult to realize. For example, implementing the circuit of Figure 56, at operating levels of 10KV 30A and at 1MHz is difficult. However 10KV 30A at 15MHz and 30MHz is very difficult. Referring to Figure 56, as the number of stages are increased, the mechanical length of the array may approach a multiple of one or more of the higher order harmonics of the design frequency. This can be very problematic. At some point a Vacuum Tube may still be the best choice.

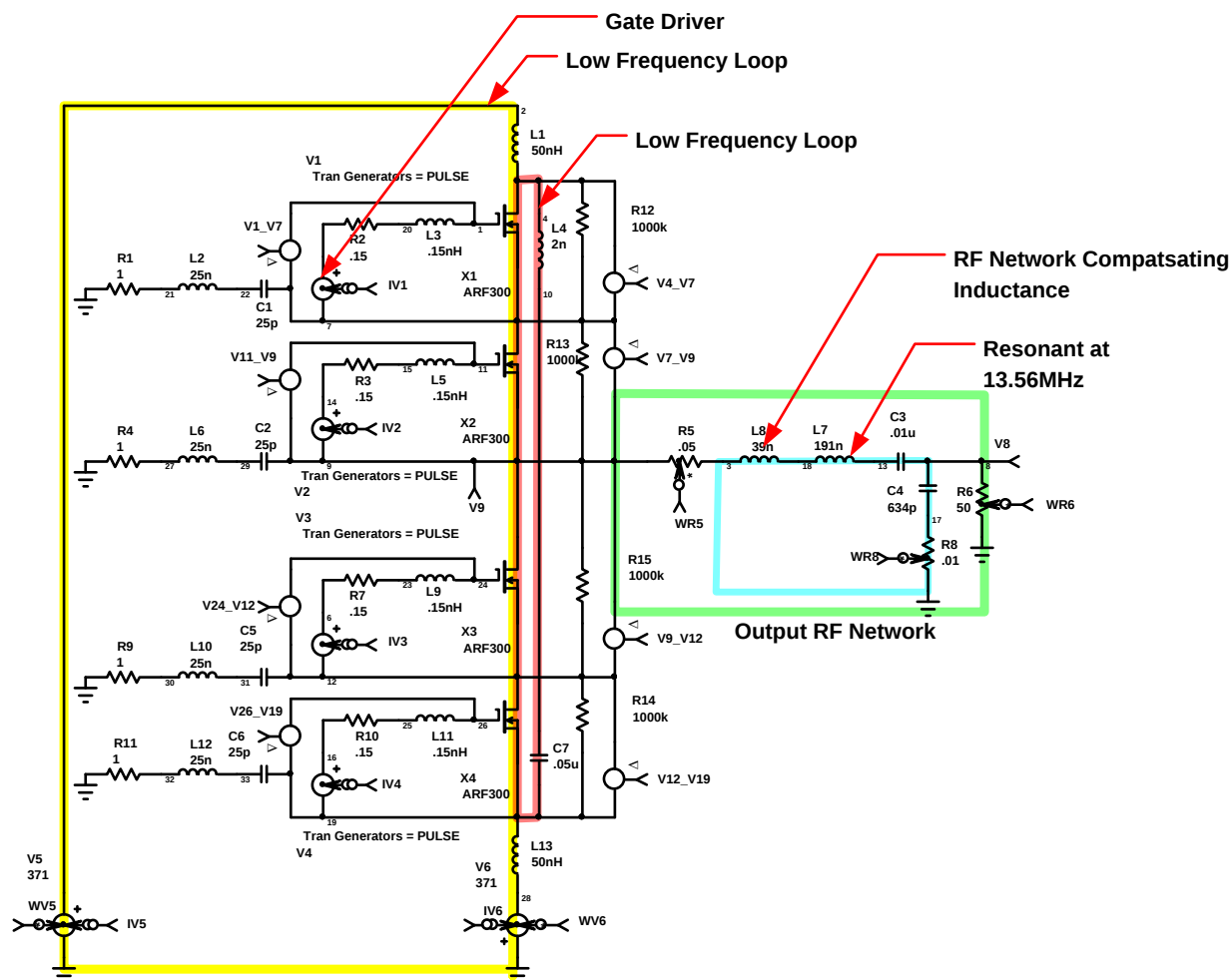


Figure 56. 10KW Half Bridge

The previous topology discussions are also valid for Figure 56. In fact their effects are more intense. Control stability is very exacerbated. The CMR required for 10KV signal with a 10ns rise time is on the order of -120db. A Fiber optic control system is the most viable solution. The Optical Control approach has additional benefits: System Layout, repeatability and the potential to extract High Side Data.

Circuit Performance	
Vsupply	±371V
Pout	10KW
Pin	11.258KW
PLoss	1258W
Eff	88.8%
Pulse Gate Drive	PW=26ns
Ths	45°C
Tj= X1, X2	130°C
Tj=X3, X4	130°C
Vds Margin	154V
Drain Z=6Ω	Out Z=50Ω

Table 11

Very High Power

Combiners

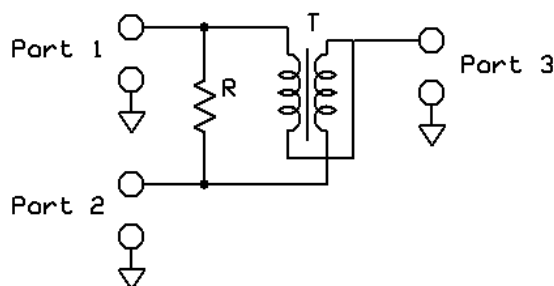


Figure 57. Three Port Combiner

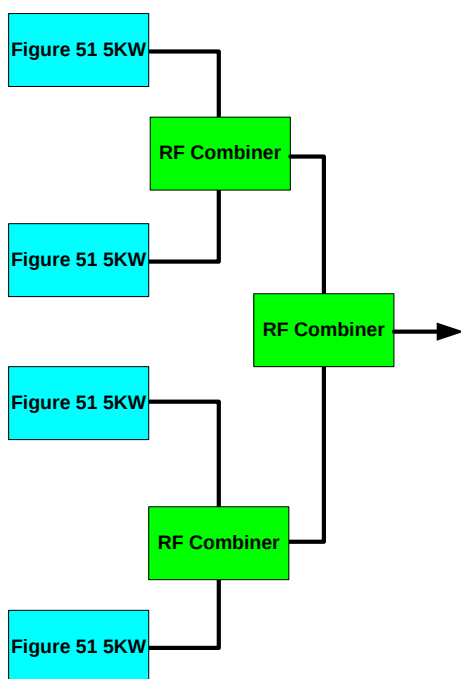


Figure 58. RF Combiners

Combiners can take many forms and their design is beyond the scope of this article. There are two basic types – transmission line “Wilkinson” combiner, and the broadband ferrite-loaded combiner. Regardless of the type used, all have several common requirements. They must take two or more signals and combine (add) their power together at a single output port. There must be isolation between the inputs such that the function of one input does not affect the others. Each input port must present a proper load to the power sources, and the output impedance of the combiner should be the same as each of the sources being combined. The combining must be accomplished efficiently. Even a 1% loss at 20kW is a considerable heating factor.

At the other end of the signal chain, the signal splitters divide the drive signal. Except for power handling capability, a splitter is exactly the same as a combiner connected in reverse.

A broadband lumped element combiner is illustrated in Figure 57. Ports 1 and 2 are the inputs. Two in-phase signals applied at the input will be combined at Port 3. Since these signals are essentially in parallel, the output impedance of Port 3 is half of the input impedance and another matching transformer must be used to bring it back up to the source's impedance. The resistor is important to the operation in two ways. If the two input signals are exactly the same amplitude and phase, no power will be lost in the resistor, but if there is any difference it will be dissipated here. If there is only one input signal, half of it will be dissipated here the other half will be delivered to the output. If the value of the resistor is twice the input Z_o , the isolation between ports will be very high.

Individual 2-way combiners can be combined in pairs, “echelon” fashion, to combine a larger number of sources. The total number of input ports is always a binary number. As illustrated in the first diagram, three 2-way combiners are used to combine four signals.

Using the three combiners of Figure 58 as a platform we can use some of the HB RF Generators we have discussed to build RF Generators to higher power levels.

Figure 51 2.5KW RF Output 4 HB 3 Combiners Power Out = 10KW Good Safety Margin

Figure 55 5.0KW RF Output 4 HB 3 Combiners Power Out = 20KW medium Safety Margin

Figure 56 10KW RF Output 4 HB 3 Combiners Power Out = 40KW Low Safety Margin

Non reactive and Reactive loads

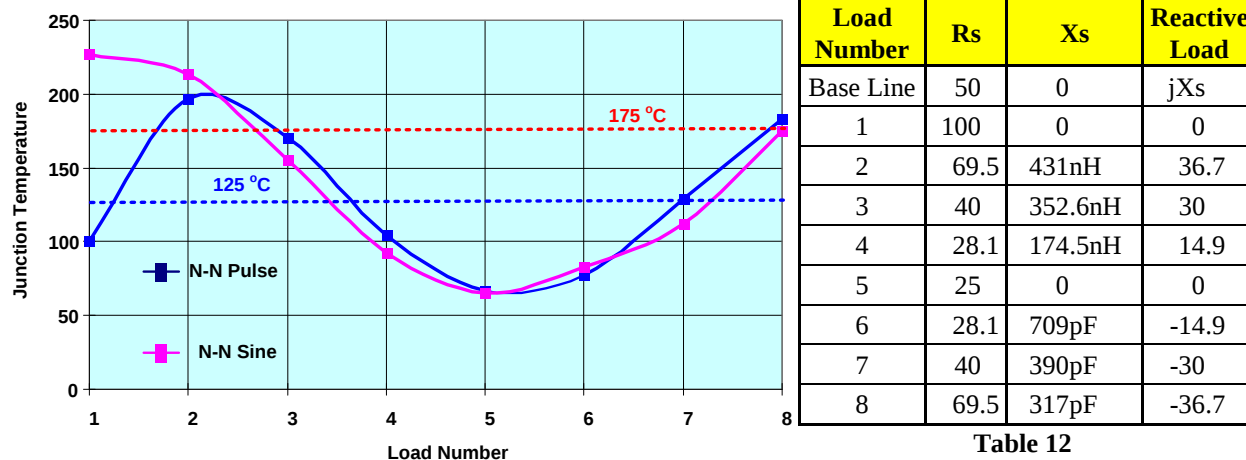


Figure 59. Loads vs. Configuration

Each of these loads illustrated in Figure 59 and Table 12, present a 2:1 VSWR mismatch to 50 Ω . They are equally spaced every 45° around a 2:1 VSWR load circle. In each of the circuits, the 50 Ω load is transformed through the output matching network (i.e. L5+L6 and C2 in Figure 1) to approximately 3 Ω at the Drains of transistors X1 and X2. A load other than 50 Ω is “mismatched” and its effect on the circuit is quite different. From a reliability standpoint, keeping the load between 3-4 on the left and at or below 7 on the right is the preferred operating space. In addition, minimizing the time spent at or above 175°C is advisable.

For a detailed discussion of N-N Pulse vs. N-N Sine drive see Microsemi Application Note 1808, ARF300-ARF301 in N-N and N-P Half Bridge RF Generators with Pulse and Sine Drive.

An output load impedance lower than 50 Ω will be transformed to a higher impedance load at the devices. The transistors can more easily supply the full output voltage to this higher impedance. Consequently, the output power is less and the junction temperature is lower. Load impedance greater than 50 Ω on the output is transformed through the matching network to an impedance lower than 3 Ω at the transistor junction. This causes the devices to be overloaded and mistuned. This puts the full voltage on this lower impedance creating more output power at lower efficiency which in turn causes the rise in junction temperature. Figure 59 clearly demonstrates the importance of maintaining a proper load on the output of the RF Generator.

Conclusion

In the preceding pages we have discussed a lengthy array of topics, focused on the ISM RF power arena. Discussions from the design of high power hybrids to the circuits’ need to exploit their maximum power capabilities. In these pages we have discussed the design approaches for RF Power systems from 1KW to 20KW all based on the DRF Series of Hybrid Devices. In the following section a collection of Relevant Publications is given.

Relevant Publications

Combiners

Krauss, Bostian, Raab, "Solid State Radio Engineering", John Wiley & Sons, 1980.

Dye, Granberg, "Radio Frequency Transistors: Principles and Practical Applications", Butterworth-Heinemann, 1993. Chapter 11.

H. Granberg, "Broadband Transformers and Power Combining Techniques for RF", AN-749, Motorola Semiconductor Products Inc.

Thermal and Cooling

DRF Device Mounting Procedures And Power Dissipation

AAVID Thermal Technologies, Inc., Box 400, Laconia, NH 03247.

Transformers

Hilbers, A.H., Design of HF wideband power transformers, Philips Semiconductors, ECO 6907, March 1998

Hilbers, A.H., Power Amplifier Design, Philips Semiconductors, Application Note, March 1998

Hilbers, A.H., Design of HF wideband power transformers Part II, Philips Semiconductors, ECO 7213, March 1998

Sevick, J., Transmission Line Transformers, Noble Publishing, 4th Ed, 2001. ISBN: 1884932185

Fair-Rite Products Corp., PO Box J, One Commercial Row, Wallkill, NY 12589.

Chris Trask, "Designing Wide-band Transformers for HF and VHF Power Amplifiers", QEX, Mar/Apr 2005, pp. 3-15.

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Krauss, Bostian, Raab, "Solid State Radio Engineering", John Wiley & Sons, 1980.

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H. Granberg, "Broadband Transformers and Power Combining Techniques for RF", AN-749, Motorola Semiconductor Products Inc.

Devices

N. Dye and H. Granberg, Radio Frequency Transistors – Principles and Practical Applications, Boston: Butterworth-Heinemann 1993. ISBN: 0-7506-9059-3. 0750672811 (2nd Ed., 2001)

Oxner, Edwin, Power FETS and Their Applications, Prentice-Hall, 1982. ISBN 0-13-686923-8

Matching

Gonzalez, Martin, Lopez, "Effects of Matching on RF Power Amplifier Efficiency and Output Power", Microwave Journal, April 1998.

RF Design

ARF300 – ARF301 In N-N and N-P Half Bridge RF Generators with Pulse and Sine Drive

Microsemi AN 1808

3KW and 5KW Half-Bridge Class-D RF Generators at 13.56MHz with 89% Efficiency and limited Frequency Agility. IXYS RF.

PRF-1150 1KW 13.56 MHz CLASS E RF GENERATOR EVALUATION MODULE. IXYS RF

SmithTM Chart is a trademark and property of Analog Instruments Co., New Providence, NJ.

Sokal, HEPA-PLUS/WB v3.29, Design Automation, Inc., Lexington, MA

MIMP, Copyright Motorola, Inc. 1992, available through Motorola RF products group.

WinSMITH, v 2.0 copyright Eagleware Corp., 1998, available through Noble Publishing, Inc.

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Davis and Rutledge, "Industrial Class-E Power Amplifiers With Low-cost Power MOSFETs and Sine-wave Drive" Conf. Papers for RF Design '97, Santa Clara, CA, Sept 1997, pp. 283-297.

M. K. Kazimierczuk and W. A. Tabisz, "Class C-E High-efficiency Tuned Power Amplifier", IEEE Transactions on Circuits and Systems, vol. 36, no. 3, pp. 421-428, March 1989.

R. Frey, "A push-pull 300 watt amplifier for 81.36 MHz," Applied Microwave and Wireless, vol. 10 no. 3, pp. 36-45, April 1998.

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US Patent 4,607,323 "Class E High-Frequency High-Efficiency Dc/Dc Power Converter" Nathan O. Sokal; Richard Redl, August 19, 1986.