

ATA6570 CAN Partial Networking Configuration

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INTRODUCTION

The ATA6570 is a stand-alone high-speed CAN transceiver with partial networking that interfaces a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus designed for high-speed CAN applications in the automotive environment.

The ATA6570 provides local and enhanced remote wake-up capabilities and is available in a SOIC-14 package. It has a very low power consumption in the Standby and Sleep modes. Besides local wake-up via the WAKE pin and remote wake-up pattern according to ISO 11898-2: 2016, the ATA6570 additionally supports ISO 11898-2: 2016 compliant CAN partial networking. A CAN frame decoder evaluates the bus traffic and checks for a matching frame that has been configured into registers via the SPI. The device is able to keep the complete ECU in a low-power mode even when bus traffic is present until a valid wake-up frame is received.

This application note describes the steps necessary to configure the device for selective wake-up according to ISO 11898-2: 2016.

CONFIGURING THE WAKE-UP FRAME

The following registers need to be configured for the Wake-Up frame to work. Depending on what parts of the frame should be used for wake-up, the configuration bits have to be set. [Table 1](#) gives an overview of this process.

1. TRXCR (0x20)

Set CPNE to '1' to enable selective wake-up.

CFDPE must be set to '1' if CAN FD frames should be ignored.

2. TRXECR (0x23)

Set CWUE to '1' to enable CAN wake-up detection.

3. CFCR (0x2F)

Configure Standard/Extended ID, whether or not DLC and data should be checked against the data mask (bit PNDM) and set the DLC.

The device can now be configured to wake up on a specific frame or on a group of IDs. To use a specific frame configure the CIDRx registers described in [CIDRx \(0x27 - 0x2A\)](#). To configure a group of frames, configure the CIDMRx registers described in [CIDMRx \(0x2B - 0x2E\)](#).

4. CIDRx (0x27 - 0x2A)

These registers store the Standard ID/Extended ID, depending on how IDE was configured in Step 3 - [CFCR \(0x2F\)](#).

5. CIDMRx (0x2B - 0x2E)

These registers store the Standard ID/Extended ID Mask, depending on how IDE was configured in Step 3.

The ID of every incoming frame in Selective Sleep mode is checked against the ID configured in CIDRx. All bits set to '1' in the mask register are ignored in the comparison.

6. CDMRx (0x68-0x6F)

These registers store a Mask for the data bytes. As soon as there is at least one matching '1' between frame and mask in any of the bytes the transceiver will wake-up.

Care must be taken that for DLC < 8 the first DM byte to be used is NOT DM0. It starts with DM(8-DLC). See [Table 2](#) for reference.

7. TRXCR (0x20)

After the correct configuration for Partial Networking has been written it must be confirmed by writing a '1' to the PNCFOK bit in register TRXCR.

TABLE 1: SELECTIVE WAKE-UP OPTIONS

Parts of the Frame to Check	Bits to Configure	Registers to Configure
Identifier + Valid CRC	CWUE = '1', CPNE = '1', PNDM = '0'	TRXCR, TRXECR, CFCR, CIDRx, CIDMRx
Identifier + DLC + Data + Valid CRC	CWUE = '1', CPNE = '1', PNDM = '1'	TRXCR, TRXECR, CFCR, CIDRx, CIDMRx, CDMRx

TABLE 2: CAN FRAME TO DATA MASK MATCHING

Type	DLC										
CAN frame	DLC > 8	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC
Data Mask	—	DLC	00	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC

CAN frame	DLC = 8	DLC	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	CRC
Data mask	—	DLC	DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC

CAN frame	DLC = 7	—	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	CRC
Data mask	—	—	DLC	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC

CAN frame	DLC = 6	—	—	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	CRC
Data mask	—	—	—	DLC	DM2	DM3	DM4	DM5	DM6	DM7	CRC

CAN frame	DLC = 5	—	—	—	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	CRC
Data mask	—	—	—	—	DLC	DM3	DM4	DM5	DM6	DM7	CRC

CAN frame	DLC = 4	—	—	—	—	DLC	Byte0	Byte 1	Byte 2	Byte 3	CRC
Data mask	—	—	—	—	—	DLC	DM4	DM5	DM6	DM7	CRC

CAN frame	DLC = 3	—	—	—	—	—	DLC	Byte 0	Byte 1	Byte 2	CRC
Data mask	—	—	—	—	—	—	DLC	DM5	DM6	DM7	CRC

CAN frame	DLC = 2	—	—	—	—	—	—	DLC	Byte 0	Byte 1	CRC
Data mask	—	—	—	—	—	—	—	DLC	DM6	DM7	CRC

CAN frame	DLC = 1	—	—	—	—	—	—	—	DLC	Byte 0	CRC
Data mask	—	—	—	—	—	—	—	—	DLC	DM7	CRC

Locking the Configuration

After the configuration has been written it can be locked to protect it against accidental modification via SPI.

The RWPR - Register Write Protection Register provides bits to lock register regions from further change.

The following bits should be set. Care must be taken that this can only happen after the device is fully configured as there are other registers in the locked regions.

1. Bit 6 - WP6

This bit locks the Data mask and the GLF register.

2. Bit 2 - WP2

This bit locks the ID and ID mask registers and the transceiver configuration.

Checking the Configuration

Now the entire configuration can be checked for errors.

All the configured registers should be read and checked against the expected value.

Example Configurations

1. Wake up on two specific STD ID (0xC0 and 0xC1), DLC = 0 no data

TRXCR = 0x50, TRXECR = 0x03

CFCR = 0x00, CIDR0 = 0x00

CIDR1 = 0x00, CIDR2 = 0x00

CIDR3 = 0x03, CIDMR0 = 0x00

CIDMR1 = 0x00, CIDMR2 = 0x04

CIDMR3 = 0x00, TRXCR = 0x72

2. Wake up on one specific EXT ID (0xAA02), DLC = 2, bit 2 in Byte 0 or bit 3 in Byte 1.

TRXCR = 0x50, TRXECR = 0x03,

CFCR = 0xB2, CIDR0 = 0x02,

CIDR1 = 0xAA, CIDR2 = 0x00,

CIDR3 = 0x00, CIDMR0 = 0x00,

CIDMR1 = 0x00, CIDMR2 = 0x00,

CIDMR3 = 0x00, CIDMR0 = 0x04,

CIDMR1 = 0x08, TRXCR = 0x72

REFERENCES

1. ATA6570 - [Product Details](#)
2. ATA6570 Data Sheet, "High-Speed CAN Transceiver with Partial Networking", Microchip Technology Inc.

APPENDIX A: REVISION HISTORY

Revision C (September 2022)

- Updated the “[Example Configurations](#)” section.

Revision B (August 2019)

- Updated the “[Example Configurations](#)” section.

Revision A (July 2019)

- Original release of this document

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