

Using the MD1730 Ultra-Low Phase Noise CW Transmit Beamformer for Medical Ultrasound Applications

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INTRODUCTION

In recent years, capabilities of medical ultrasound flow imaging systems have increased enormously. Color flow imaging, Continuous Wave Doppler (CWD) and Doppler analysis that provide new flow image features are now commonly used. It is essential for the ultrasound system to generate low-phase noise, high-quality CW transmission waveforms to get higher-quality Doppler echo signals.

This application note describes how Microchip's MD1730 can help ultrasound systems achieve higher-quality, lower phase noise, focused CW array transmitters.

MD1730 is a very low-phase noise, 8-channel CW beamforming waveform generation IC. It is designed for CW Doppler mode in a medical ultrasound image system.

CW BEAMFORMER TOPOLOGY

Normally, in CW mode, only ± 2 to ± 6 V peak-to-peak voltages are needed to drive the piezoelectric elements in the ultrasound transducer probe. Therefore, the MD1730 circuit has been designed using the high-speed, low-voltage and low-time jitter CMOS technology. The MD1730 provides an ultra-low phase noise CW waveform, a high resolution CW frequency divider and the per-channel delay timer for CW beamforming function. These features help provide eight frequency-programmable CW sources with phase delay beamforming functions in a small 6 x 6 mm QFN package. It helps save significant PCB real estate for portable medical ultrasound system. [Figure 1](#) shows a typical beamforming application for focused CWD in a medical ultrasound system.

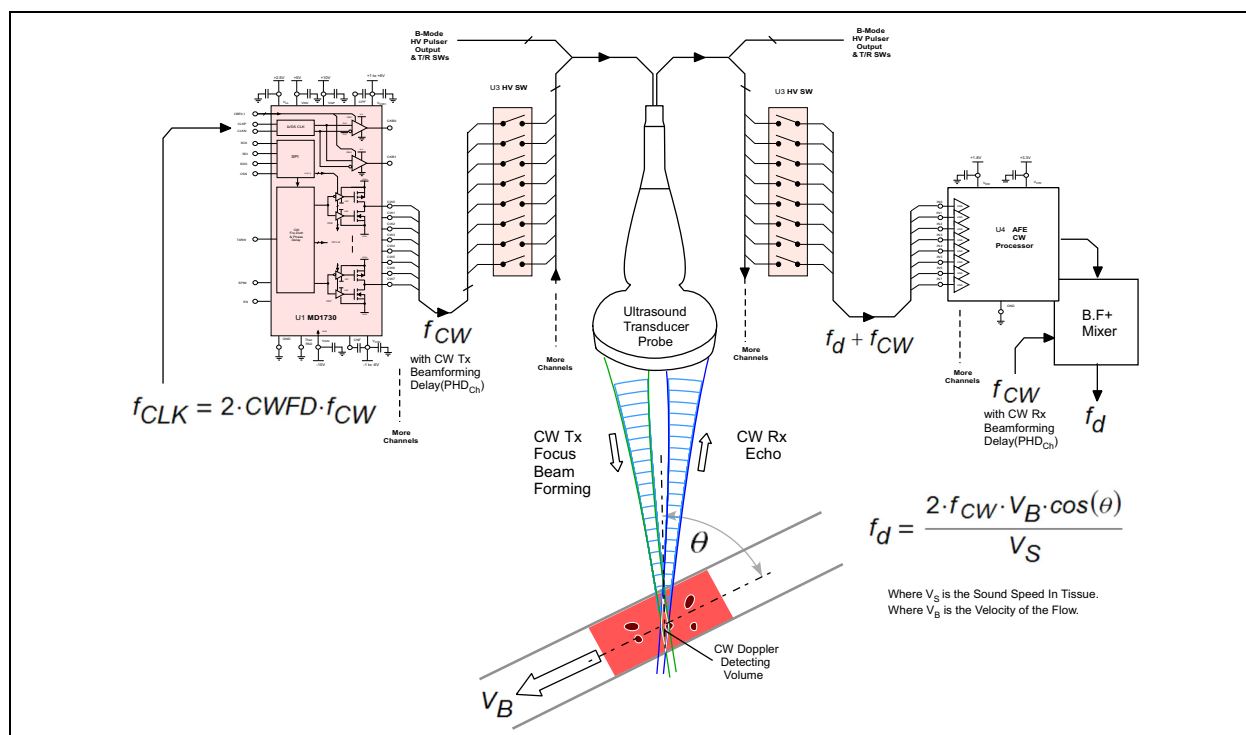
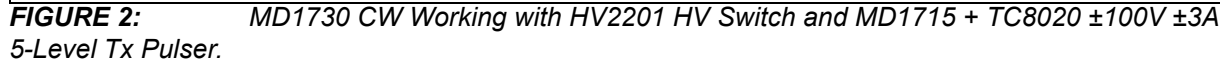


FIGURE 1: Forced CWD Beamforming in Medical Ultrasound System.

The ultra-low phase noise, high-speed and low-voltage outputs of the MD1730 cannot withstand the high-voltage B-mode transmit pulse voltages. Therefore, HV analog switches must be used to block the Tx pulser outputs from the MD1730 during B-mode. [Figure 2](#) shows an example implementation where Microchip's HV2201 8-channel analog MUX is used with the MD1730. HV2201 has eight high-voltage analog switches that can withstand a $\pm 100\text{V}$ peak

voltage of transmit pulses. When the HV switches are on, their low on-resistance has an extremely low contribution to the overall phase noise and phase retardation of the CW waveforms. One MD1730, when combined with one HV2201, can be used with four sets of MD1715s and TC8020s to form an 8-channel, 5-level $\pm 100\text{V}$ high-end Tx pulser with ultra-low phase noise CW digital beamformer. During B-mode operation, MD1730 is disabled using its EN pin, and the HV2201 switches are turned off using its CLR pin. In CW mode, the MD1730 is enabled and the HV2201 switches are turned on.



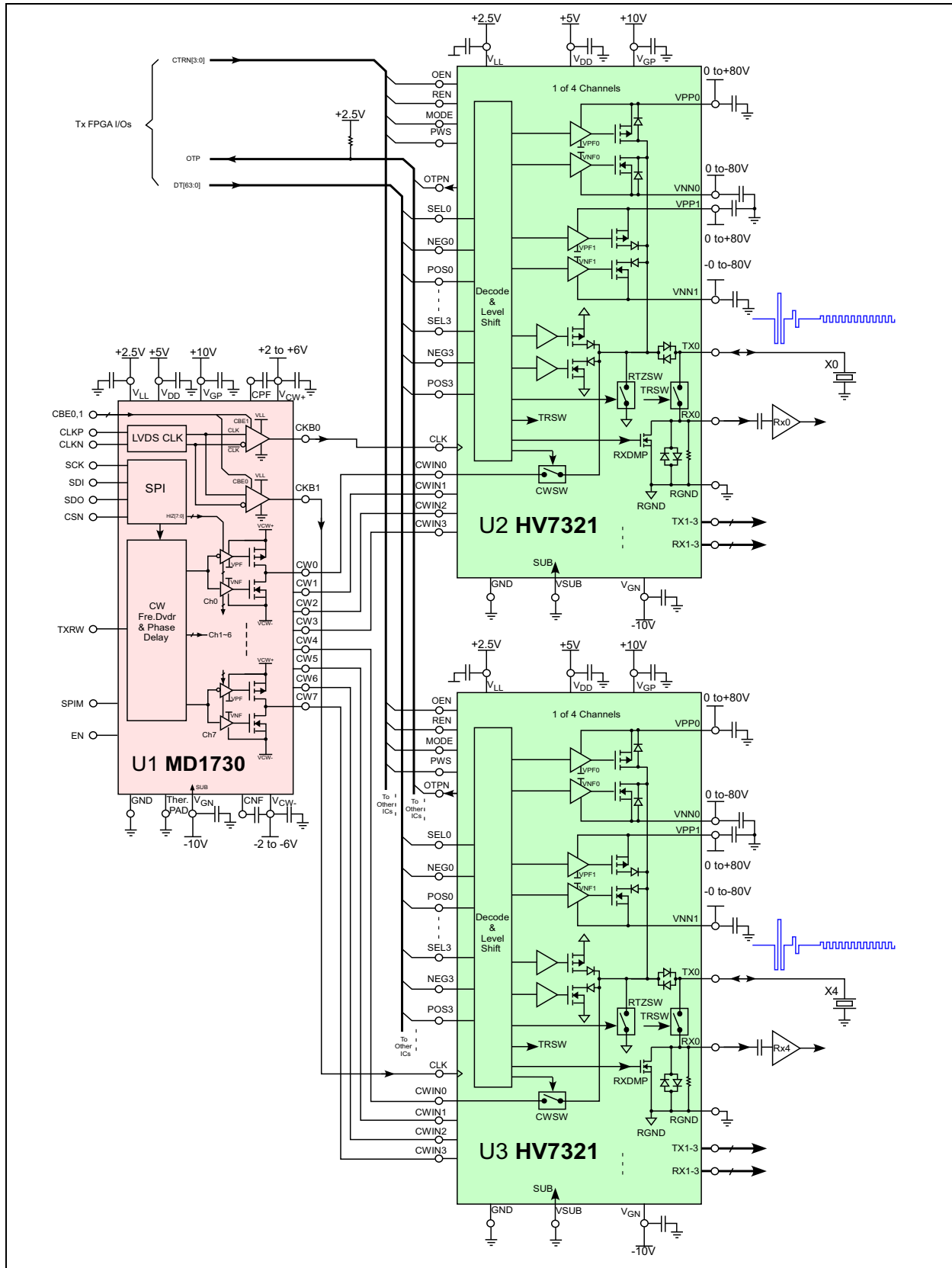


FIGURE 3: MD1730 with Two HV7321 as Low-Phase Noise CW Beamformer.

MD1730 WORKING WITH HV7321 TX PULSER

For the higher integration levels required in portable medical ultrasound systems with tighter PCB spacing, Microchip's HV7321 ultrasound transmit pulser, along with MD1730, offer a better and simpler solution. Refer to [Figure 3](#).

HV7321 is specifically designed to work with low-voltage, ultra-low phase noise CW waveform generators such as the MD1730. HV7321 is a four-channel, 5-level $\pm 80\text{V}$, 2.6A ultrasound transmitter. HV7321 has integrated T/R switches (TRSW) and RTZ switches (RTZSW) along with high-voltage analog CW switches (CWSW).

When in B-mode, all CW switches are off and they block the high-voltage pulses. When the HV7321 is in CW Mode-1, these CW switches are turned on. The input terminals of the CW switches on the HV7321 (CWIN0-3) connect to the MD1730's CW outputs (CW0-7).

With the built-in CW switches, the HV7321 output pins can be directly connected to the ultrasound transducers. The HV7321's built-in high-voltage analog switches act like a high-voltage MUX, blocking the high voltages in B-mode and passing through the low-voltage CW signals to the MD1730.

CONTROLLING THE MD1730 AND THE HV7321

During B-mode, the MD1730 does not need to be enabled. Setting $\text{EN} = 0$ will reduce power consumption. The user can turn off the MD1730's clock on CLKP and/or CLKN for power saving.

If MD1730's $\text{EN} = 1$, the user must set $\text{TXRW} = 0$, to make sure the CW0-7 output are all in high Z state. At the same time, HV7321's CWSW0-3 must be turned off, by setting the pin to $\text{MODE} = 0$. When the MD1730's CW signals are expected, the HV7321 is set to CW Mode-1.

The following steps should be taken to ensure proper operation:

1. Apply all power supply rails to both chips and set HV7321's to $\text{OEN} = \text{REN} = \text{PWS} = 1$ along with MD1730's to $\text{EN} = 1$ to enable both chips. Set all other logic input pins to zero.
2. Adjust the $V_{\text{CW+}}$ and $V_{\text{CW-}}$ power supplies to the required peak-to-peak voltage levels for CW output transmission. Please note that a higher peak-to-peak transmission voltage will result in the MD1730 dissipating more power. The power dissipation of the MD1730 is proportional to the square of the peak-to-peak voltage (about 2 to $12V_{\text{P-P}}$).
3. Set HV7321's $\text{MODE} = 1$.

4. Program the MD1730 with the desired CW frequency divider and delay settings for CW transmission.

For more details, please see the MD1730 data sheet "8-Ch Ultra Low Phase Noise CW Transmitter with Beamformer" (DS20005586).

5. To place a channel in receive mode, set the channel's SEL, NEG and POS pins to 0, 1 and 1 respectively on the HV7321. To place a channel in CW transmit mode, set the channel's SEL, NEG and POS to any other combination other than 0,1 and 1 respectively on HV7321. This will put that channel of the HV7321 high-voltage Tx output in high Z mode, but it will turn on the channel's CW switch (CWSW).

To set the MD1730's CW pin in high Z mode, set the corresponding bit in the high Z register to 1.

6. Once the system is ready to perform CW Doppler measurement, assert TXRW high to start the CW transmission on the selected channels.

LOW PHASE NOISE CLOCK INPUTS AND OUTPUT BUFFERS

MD1730's built-in eight independent channels share one pair of synchronization clock input pins: CLKP/CLKN. The IC can accept a clock frequency up to 250 MHz. These clock inputs can be connected as differential LVDS input, or as single-ended LVCMOS 2.5V input.

If a higher CW frequency step resolution is needed, then the differential LVDS or SSTL2.5V type clock input method can be used, as shown [Figure 4](#); a 100Ω differential termination resistor must be connected as closely as possible to the CLKP and CLKN pins.

LVDS clock line pair traces on the PCB should be designed as two 50Ω transmission lines with respect to GND plane, and the differential traces should be run as closely as possible after they leave the multi-LVDS buffer IC.

However, for the best phase noise performance, use an LVCMOS-2.5V single-ended type clock input, as shown in [Figure 4](#). The clock frequency should be in the range of 80 to 120 MHz. Select a very low phase noise LVCMOS 2.5V clock buffer, like Microchip's PL133-47. The input clock of the buffer IC should be from an ultra-low phase crystal oscillator source.

If the CLKP input pin is connected to a single-ended LVCMOS-2.5V buffer output, then the CLKN input pin must be connected to 1.25V with a $0.1\mu\text{F}$ bypass capacitor to GND.

To use as an inverting phase of clock input, the CLKP and CLKN input pins can be swapped. CLKN should be connected to the buffer output, and CLKP should be connected to 1.25V and bypassed with a capacitor to GND.

In the single-ended clock input case, a 33Ω reverse termination resistor must be placed in-series with each buffer output. These resistors should be placed close to the buffer output pins. The clock trace on the PCB should be designed as a 50Ω transmission line with respect to the GND plane. Figure 4 shows this reverse termination method. The clock trace reaches to the MD1730 clock input pin, so a 50Ω resistor will no longer be needed to terminate to GND.

Following this method, the user can save power consumption for the clock distribution circuit. For the best phase noise performance, the value of the reverse termination resistor should be optimized based on the CWD mode phase noise results.

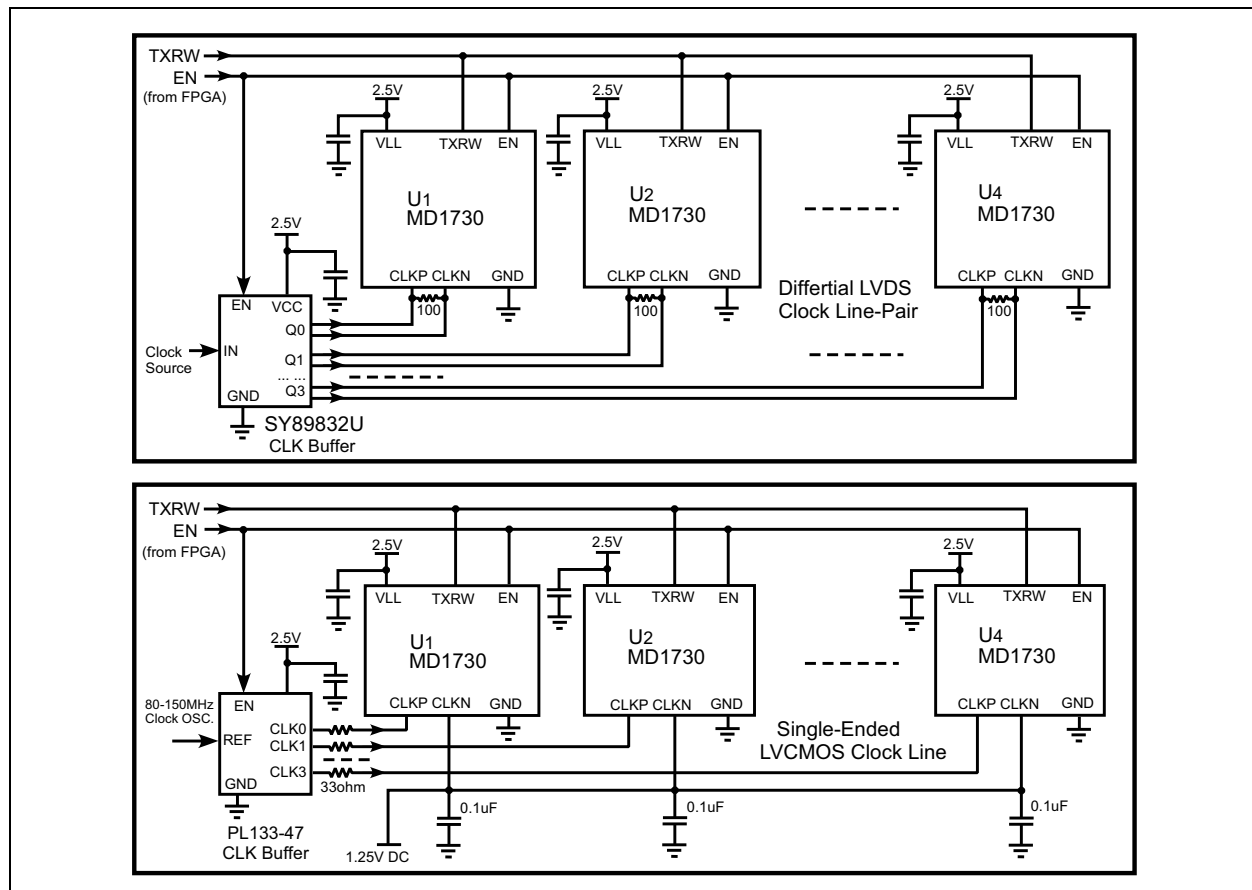


FIGURE 4: Configuration as LVDS or LVCMOS - 2.5V Single-Ended Clock Inputs.

INTERFACE AND REGISTERS CONFIGURATION

MD1730 has two registers that can be configured via SPI interfaces. The first register is the per-channel beamforming delay register $PHD_{ch}<7:0>$. The second register is the CW frequency divider number register $CWFD<7:0>$. Normally, it only needs to be configured once, and all the MD1730 chip's CWFD registers should have the same number.

Multiple MD1730s can be daisy-chained and programmed as shown in Figure 5. Use the normal SPI operation mode to write the first type ($PHD_{ch}<7:0>$) of register and use the Broadcasting mode to set the $CWFD<7:0>$ quickly on each chip.

NORMAL SPI MODE VS. SPI BROADCASTING MODE

The MD1730 SPI interface circuitry is designed to directly connect to a normal SPI on a FPGA I/O pins. To write into the MD1730 SPI registers, the user must always send the MSB data bit first.

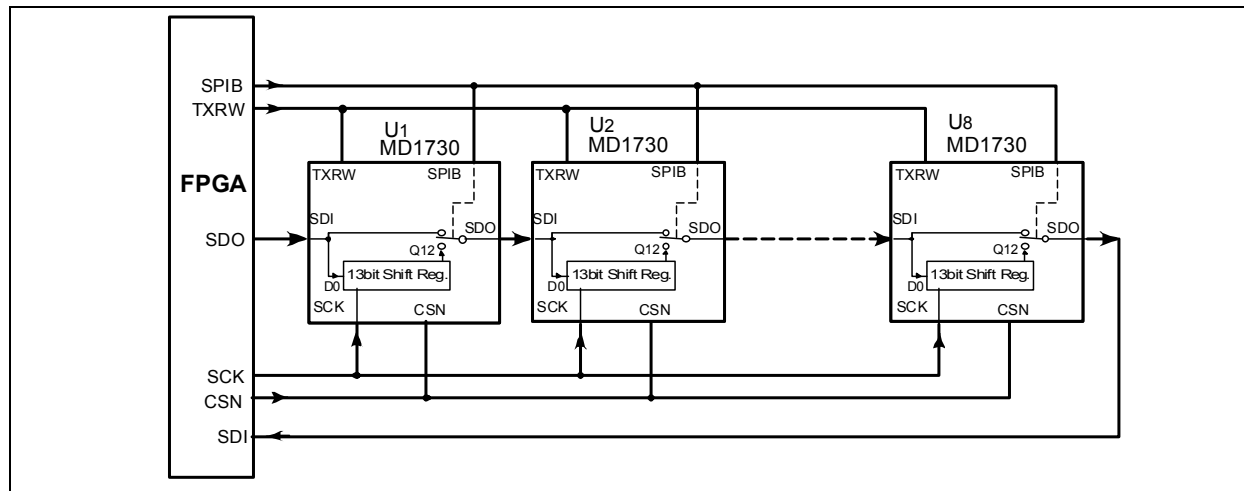


FIGURE 5: Multiple MD1730 Devices SPI Daisy Chain.

When SPIB = 0, the chip is configured in normal SPI read/write mode. In this mode, multiple MD1730s can be configured using the daisy chain.

When SPIB = 1, the chip will support the Broadcasting mode, in which multiple MD1730s can be programmed with the same value simultaneously. This high-speed Broadcasting mode reduces the programming time significantly and can be used to program the beamforming CW frequency registers.

In addition, all the data being written into the registers in each chip during the broadcasting mode can be read out by the normal SPI read operations to be verified. This read-back feature helps with software debugging and testing.

EXAMPLE OF SPI WRITE OPERATION

The following is a 1-byte writing example for the register at ADD = 0011b with the data D<7:0> = 01010101 when SPIB = TXRW = 0:

1. The write operation starts with setting CSN to low.
2. SDI data is shifted into the shift register:
D<12> = 1 (W/R bit is set high); writing is enabled.
ADD<11:8> = 0011b, address for channel 3's phase delay register.
D<7:0> = 01010101b, data to be written into channel 3's phase delay register.

The SDI data is shifted in at the rising edge of SCK.

3. Once the complete data has been shifted in, the CSN should be set high to finish the writing operation. The SDI data is latched into channel 3's phase delay register on the rising edge of CSN. CSN has to be kept high for a minimum of two SCK cycles for the data to be written into the appropriate register.

In the case of eight chips daisy-chained together, there should be $13 \times 8 = 104$ cycles of SCK before the CSN is set high.

MD1730 can also be used in Broadcasting mode to write several daisy-chained chips with the same data. The Broadcasting mode can be used to reduce the time required to write using SPI if several MD1730 chips have to be programmed with the same data. An example of writing to MD1730 in broadcasting mode is given below:

1. Set TXRW = 0 and SPIB = 1. Set CSN = 0 (broadcasting operation starts).
2. Shift in the following SDI data to the first MD1730 chip with SCK clock:
D<12> = 1 (W/R bit is set high), writing is enabled.
ADD<11:8> = 0011b, address for the channel 3's phase delay register.
D<7:0> = 01010101, data to be written into the channel 3's phase delay register.

The SDI data is shifted in at the rising edge of SCK.

In broadcasting mode, the same set of data shifted into the first chip is sent to all the MD1730 chips along the daisy chain. When SPIB = 1, an internal switch connects the SDI and SDO directly, bypassing the shift register.

3. Once the complete data has been shifted in, the CSN should be set high to finish the writing operation. The SDI data is latched into each chip's channel 3 phase delay register on the rising edge of the CSN signal. CSN has to be kept high for a minimum of two SCK cycles for the data to be written into the appropriate register.

SPI READ OPERATION EXAMPLES

The following is an example to read 2-byte data from the MD1730 register at ADD = 0011b (channel 3's phase delay register) when SPIB = TXRW = 0:

1. Set CSN = 0. Read-write operation starts.
2. SDI shifts in the following data:
D<12> = 0 (W/R bit is set low). Reading is enabled.
ADD<11:8> = 0011b, address for channel 3's phase delay register.
D<7:0> = x, for a read operation, the data field is 'don't care'.
The SDI data is shifted in at the rising edge of SCK.
3. Once the complete data has been shifted into the SPI, the CSN is set high. While CSN is high, the MD1730 fetches the data located at ADD<11:9> = 0011b and places it in its internal shift register.
CSN has to be kept high for a minimum of two SCK cycles for the data to be fetched and placed into the internal shift register.
4. CSN is set low and during the next 13 SCK clock cycles, the fetched data in the internal shift register is clocked out on the rising edge of SCK from the SDO of the MD1730.

POWER SUPPLY DECOUPLING

MD1730 is designed for ultra-low phase noise operation. However, the overall phase noise will not be only be dependent on the MD1730 internal circuit design and manufacture, but also dependent on the following application conditions:

- power supply ripple noise
- power supply switching spike noise
- power supply topology
- power supply circuit layout

- selection and layout of the decoupling capacitors for the MD1730's power pins
- PCB stack-up and ground planes

It is highly recommended that the user selects an ultra-low ripple noise and well-filtered DC power source for each one of the six power supplies required by the MD1730.

It is also recommended to use a low-noise, isolated, DC/DC power supply followed by a linear, low-dropout, post regulator.

A suitable power supply topology for this application is a push-pull converter. This converter has good efficiency, low output noise and high common mode noise isolation.

Every design must pass EMI/RFI regulation compliance for medical equipment. Typical methods to meet these requirements include using low-inductance PCB layout techniques and adding R-C snubbers at switching nodes.

The DC-to-DC converter circuit's DC input and output voltage node to the ground must have considerable bypassing capacitors to achieve lower switching ripple and spike noise filtering. It is very important to select low ESR/ESL ceramic surface mount capacitors.

The switching power supply isolation transformer design must have good electrical and magnetic shielding, ground and flex bindings.

Ensure that the switching noise from the DC/DC converter does not contaminate the MD1730's ground plane.

An example of a power supply ground connections to ensure a low-noise power supply is shown in [Figure 6](#).

It is recommended to define a localized copper area for each circuitry block of the DC-to-DC converters as each block circuitry common ground. All the components within the circuitry block have to be placed on a localized common ground area. Then all local ground traces, as short as possible, must connect to each other first. Then, the local ground summing node goes through via(s) connecting to the second-layer ground copper plane. After that, use only one point, such as one big via to connect this localized common ground to the GND plane of the PCB. This method should also be used for the post LDO linear voltage regulators.

Using an LDO at the output of DC-to-DC converter helps improve voltage regulation, as well as reduce noise from the DC-to-DC converter in the 100 Hz to 100 kHz range.

Selecting correct decoupling capacitors (value and type) is important. It is recommended that the decoupling capacitors used are low ESR/ESL, multi-layer ceramic chip capacitors. [Table 1](#) lists the recommended capacitors at each of the power supply pins of the MD1730.

The switching frequencies of the DC/DC converters should be synchronized to the CW frequency or the input clock frequency.

Supply Rail	De. Cap. Value/Voltage Rating	Capacitor Type
V _{LL} to GND	1.0 μ F/10V _{DC}	Low ESR/ESL Ceramic X5R or X7R 0603/0402
V _{DD} to GND	1.0 μ F/10Vdc	
V _{GP} to GND	2.2 μ F/16V _{DC}	
V _{GN} to GND	2.2 μ F/16V _{DC}	
V _{CW+} to GND	1.0 μ F/16V _{DC}	
V _{CW-} to GND	1.0 μ F/16V _{DC}	
CPF to V _{CW+}	1.0 μ F/16V _{DC}	
CNF to V _{CW-}	1.0 μ F/16V _{DC}	

MD1730 CW OUTPUT PHASE NOISE MEASUREMENT

In this setup, an RF mixer is used as phase detector. The mixer must be a wide-bandwidth symmetric-diode ring type. The two CW waveforms are at 90 degrees phase-shifted with respect to each other. The two channels under evaluation can belong to one or two DUT chips of MD1730. Both CW channels can be driven by a single clock source CLK. The clock source and the buffers phase noise will be rejected by the symmetric mixer. But the CW channel frequency divider and channel phase delay counter circuits are independent. The phase noise generated by the two channels cannot be considered to be correlated to each other. Therefore, the final phase noise measurement should be considered as the sum of the two independent MD1730 channels noises.

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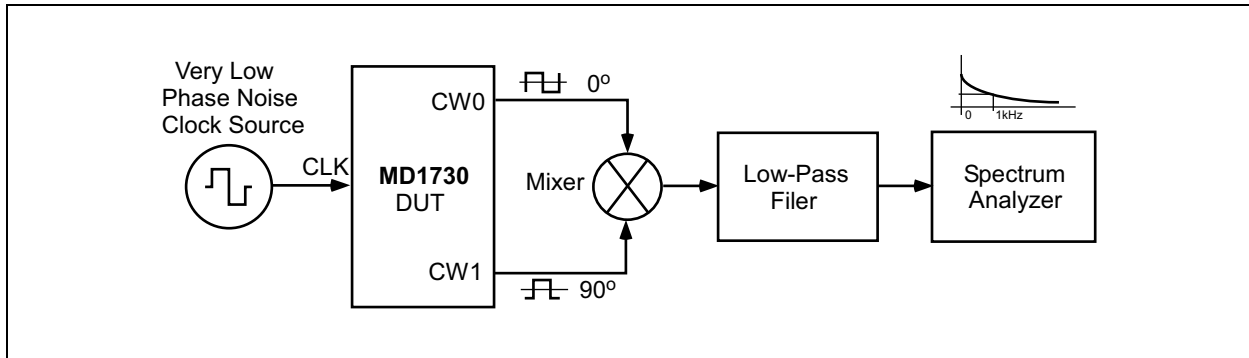


FIGURE 7: MD1730 CW Output Phase Noise Measurement Setup.

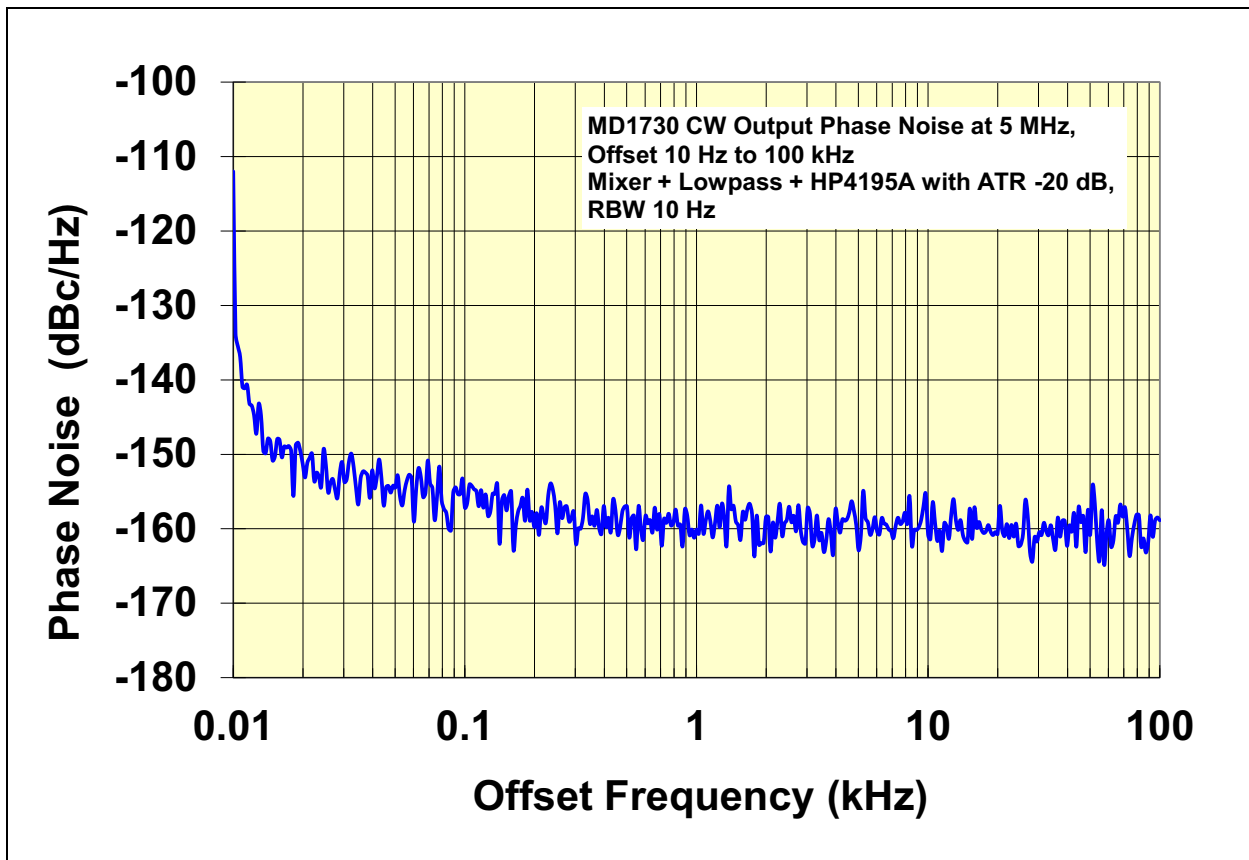


FIGURE 8: MD1730 CW Output Typical Phase Noise.

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