| REV | CHANGE DESCRIPTION | NAME | DATE |
|---|---|---|---|
| A | Release | | 11-25-13 |
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## DOCUMENT DESCRIPTION

**Schematic Checklist for the LAN7500I, 56-pin QFN Package**

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| Document Number | Revision |
|---|---|
| SC471247 | A |

# Schematic Checklist for LAN7500I

### Information Particular for the 56-pin QFN Package

## LAN7500I QFN Phy Interface:

1. TR0P (pin 44); This pin is the transmit/receive positive channel 0 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

2. TR0N (pin 43); This pin is the transmit/receive negative channel 0 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

3. TR1P (pin 47); This pin is the transmit/receive positive channel 1 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

4. TR1N (pin 46); This pin is the transmit/receive negative channel 1 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

5. TR2P (pin 52); This pin is the transmit/receive positive channel 2 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

6. TR2N (pin 51); This pin is the transmit/receive negative channel 2 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

7. TR3P (pin 55); This pin is the transmit/receive positive channel 3 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

8. TR3N (pin 54); This pin is the transmit/receive negative channel 3 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

9. For Transmit/Receive Channel connections and termination details, refer to Figure 1.

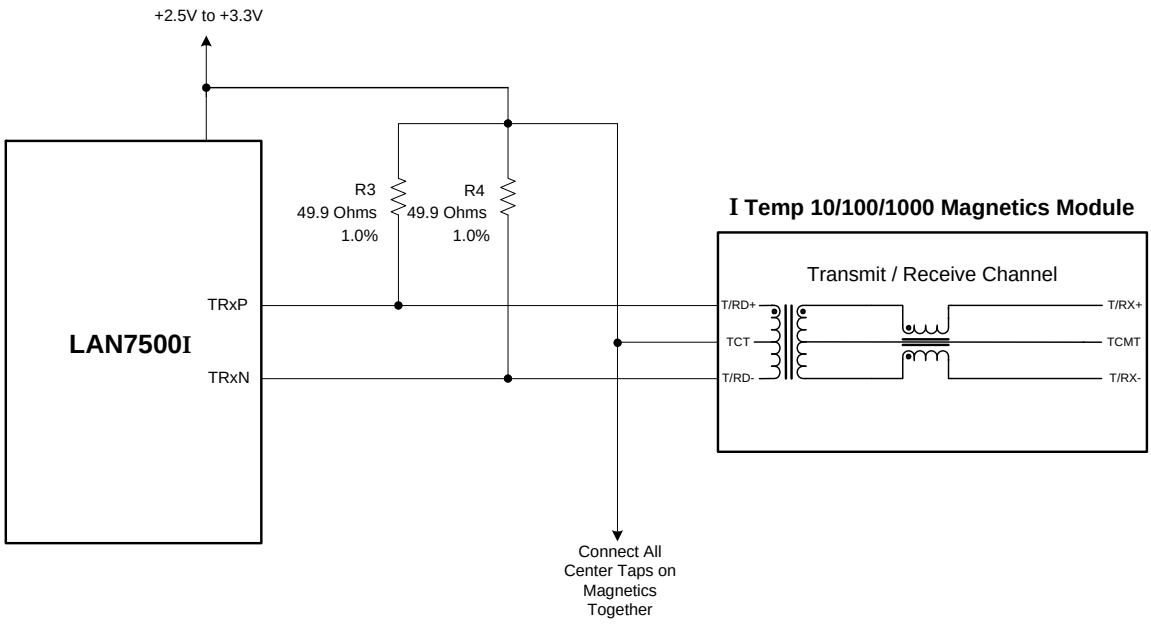



**Figure 1 – Transmit / Receive Channel x Connections and Terminations**

## LAN7500I QFN Magnetics:

1. The center tap connection on the LAN7500I side for each channel must be connected to the same power supply as the bias supply for the Ethernet terminations.

2. The center tap connection on the cable side (RJ45 side) for each channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

3. Assuming the design of an end-point device (NIC), TR0P (pin 44) of the LAN7500I QFN should trace through the magnetics to pin 1 of the RJ45 connector.

4. Assuming the design of an end-point device (NIC), TR0N (pin 43) of the LAN7500I QFN should trace through the magnetics to pin 2 of the RJ45 connector.

5. Assuming the design of an end-point device (NIC), TR1P (pin 47) of the LAN7500I QFN should trace through the magnetics to pin 3 of the RJ45 connector.

6. Assuming the design of an end-point device (NIC), TR1N (pin 46) of the LAN7500I QFN should trace through the magnetics to pin 6 of the RJ45 connector.

7. Assuming the design of an end-point device (NIC), TR2P (pin 52) of the LAN7500I QFN should trace through the magnetics to pin 4 of the RJ45 connector.

8. Assuming the design of an end-point device (NIC), TR2N (pin 51) of the LAN7500I QFN should trace through the magnetics to pin 5 of the RJ45 connector.

9. Assuming the design of an end-point device (NIC), TR3P (pin 55) of the LAN7500I QFN should trace through the magnetics to pin 7 of the RJ45 connector.

10. Assuming the design of an end-point device (NIC), TR3N (pin 54) of the LAN7500I QFN should trace through the magnetics to pin 8 of the RJ45 connector.

11. In order to guarantee IEEE compliancy over the entire temperature range of operation, the magnetics used in conjunction with the LAN7500I must be rated for Industrial Temperature use.

## RJ45 Connector:

1. The RJ45 shield should be attached directly to chassis ground.

## +3.3V Power Supply Connections:

1. **Note:** There are no internal regulators within the LAN7500I. All power pins on the LAN7500I must be supplied by external power supplies.

2. The analog supply (VDD33A) pin on the LAN7500I QFN is pin 15. This pin requires a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

3. The VDD33A pin should also have one .01 µF (or smaller) capacitor to decouple the LAN7500I. The capacitor size should be SMD_0603 or smaller.

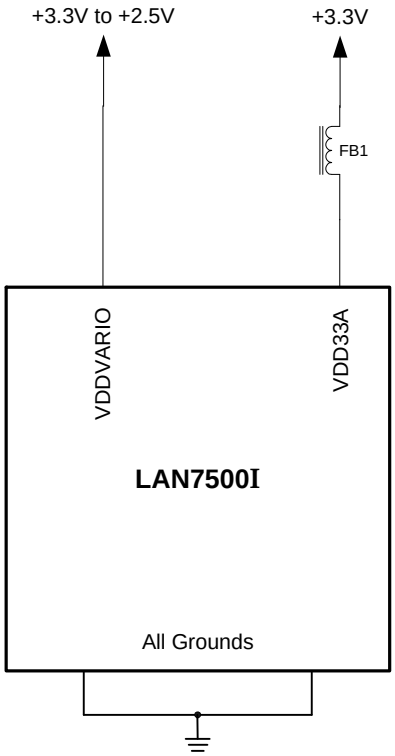



**Figure 2 - +3.3V Power Supply Connections**

## VDDVARIO Power Supply Connections:

1. The power drawn by the VDDVARIO pins, the Ethernet terminations and the 10/100/1000 magnetics is approximately 210 mA. The design engineer should be sure to size the external power supply appropriately being able to supply at least two times the expected current. This should allow for enough headroom to compensate for any system variations.

2. The VDDVARIO supply pins on the LAN7500I QFN are 7, 19, 24 & 37. These pins require a connection to +3.3V - +2.5V.

3. Each VDDVARIO pin should also have one .01 μF (or smaller) capacitor to decouple the LAN7500I. The capacitor size should be SMD_0603 or smaller.

## +1.2V Power Supply Connections:

1. **Note:** There are no internal regulators within the LAN7500I. All power pins on the LAN7500I must be supplied by external power supplies.

2. The power drawn by the VDD12CORE pins, the VDD12A pins, the VDD12USBPLL pin, the VDD12BIAS pin, and the VDD12PLL pin is approximately 460 mA. The design engineer should be sure to size the external power supply appropriately being able to supply at least two times the expected current. This should allow for enough headroom to compensate for any system variations.

3. VDD12CORE (pins 8, 11, 20, 23, 30 & 36), these six pins must be connected to an external +1.2V supply and provide power to the +1.2V core of the LAN7500I.

4. The VDD12CORE pins should each have one .01 µF (or smaller) capacitor to decouple the LAN7500I. The capacitor size should be SMD_0603 or smaller.

5. VDD12A (pins 45, 48, 53 & 56), these four pins supply power to the analog block of the LAN7500I. These pins must be connected to an external +1.2V supply through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

6. The VDD12A pins should each have one .01 µF (or smaller) capacitor to decouple the LAN7500I. The capacitor size should be SMD_0603 or smaller.

7. VDD12BIAS (pin 49), this pin must be connected to an external +1.2V supply directly (no ferrite bead required).

8. The VDD12BIAS pin should have one .01 µF (or smaller) capacitor to decouple the LAN7500I. The capacitor size should be SMD_0603 or smaller.

9. VDD12USBPLL (pin 17), this pin supplies power for the USB PLL. This pin must be connected to an external +1.2V power supply through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

10. The VDD12USBPLL pin should have one .01 µF (or smaller) capacitor to decouple the LAN7500I. The capacitor size should be SMD_0603 or smaller.

11. VDD12PLL (pin 50), this pin supplies power for the Ethernet PLL. This pin must be connected to an external +1.2V power supply through a third ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

12. The VDD12PLL pin should have one .01 µF (or smaller) capacitor to decouple the LAN7500I. The capacitor size should be SMD_0603 or smaller.

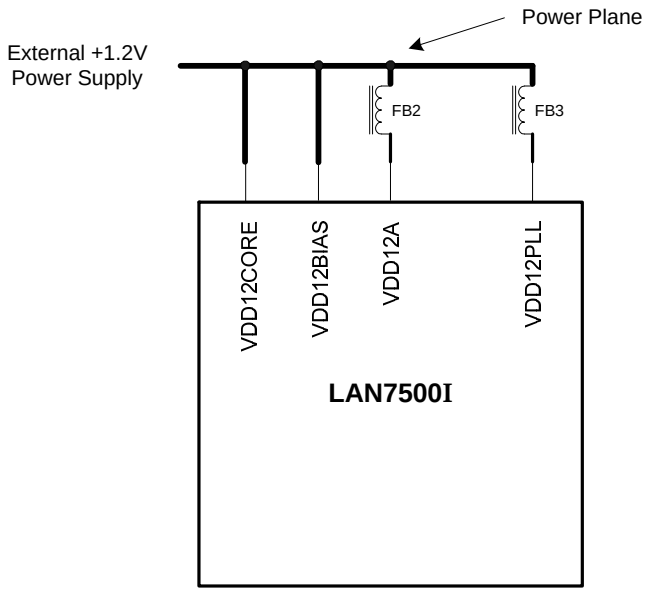



**Figure 3 - LAN7500I +1.2V Power Connections**

## Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN7500I QFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN7500I must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

## Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN7500I QFN. For exact specifications and tolerances refer to the latest revision LAN7500I data sheet.

2. XI (pin 5) on the LAN7500I QFN is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 6) on the LAN7500I QFN is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN7500I QFN.

6. In order to guarantee IEEE compliancy over the entire temperature range of operation, the crystal used in conjunction with the LAN7500I must be rated for Industrial Temperature use.

## EEPROM Interface:

1. EECS (pin 29) on the LAN7500I QFN connects to the external EEPROM's CS pin.

2. EECLK (pin 26) on the LAN7500I QFN connects to the external EEPROM's serial clock pin.

3. EEDI (pin 27) on the LAN7500I QFN connects to the external EEPROM's Data Out pin.

4. EEDO (pin 28) on the LAN7500I QFN connects to the external EEPROM's Data In pin.

5. Be sure to select a 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation.

## ETHRBIAS Resistor:

1. ETHRBIAS (pin 41) on the LAN7500I QFN should connect to digital ground through a 8.06K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

## USBRBIAS Resistor:

1. USBRBIAS (pin 16) on the LAN7500I QFN should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded USB Physical device.

## Required External Pull-ups/Pull-downs:

1. GPIO0 (pin 31) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
2. GPIO1 (pin 32) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
3. GPIO2 (pin 33) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
4. GPIO3 (pin 34) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
5. GPIO4 (pin 35) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
6. GPIO5 (pin 38) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
7. GPIO6 (pin 40) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
8. GPIO7 (pin 10) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
9. GPIO8 (pin 18) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
10. GPIO9 (pin 21) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
11. GPIO10 (pin 22) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
12. GPIO11 (pin 25) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

## USB Interface:

1. USBDP (pin 13), this pin is the USB channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, upstream USB connector (Type “B”).

2. USBDM (pin 12), this pin is the USB channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, upstream USB connector (Type “B”).

3. Typical Bus Powered applications will connect pin 1 (VCC) on a standard 4-pin, upstream USB connector (Type “B”) directly to a 2000 mA ferrite bead. This ferrite bead will in turn feed a LDO +5.0V-to-+3.3V voltage regulator to power the LAN7500I.

4. We recommend no bulk capacitance be placed on pin 1 (VCC) of the USB connector in Bus Powered applications. On the voltage regulator side of the ferrite bead, we recommend limiting the bulk capacitance to 4.7 uF. This should satisfy the 10.0 uF total capacitance to limit in-rush current as required by the USB specification.

5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, upstream USB connector (Type “B”) directly to digital ground.

6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.

7. VBUS_DET (pin 14), this pin detects the state of the supplied upstream power. This pin must be tied to VDD33A when operating in Bus-Powered mode. When using the LAN7500I in Self-Powered mode, this pin should be tied to the USB power through the recommended circuit below. This pin has a weak internal pull-down.

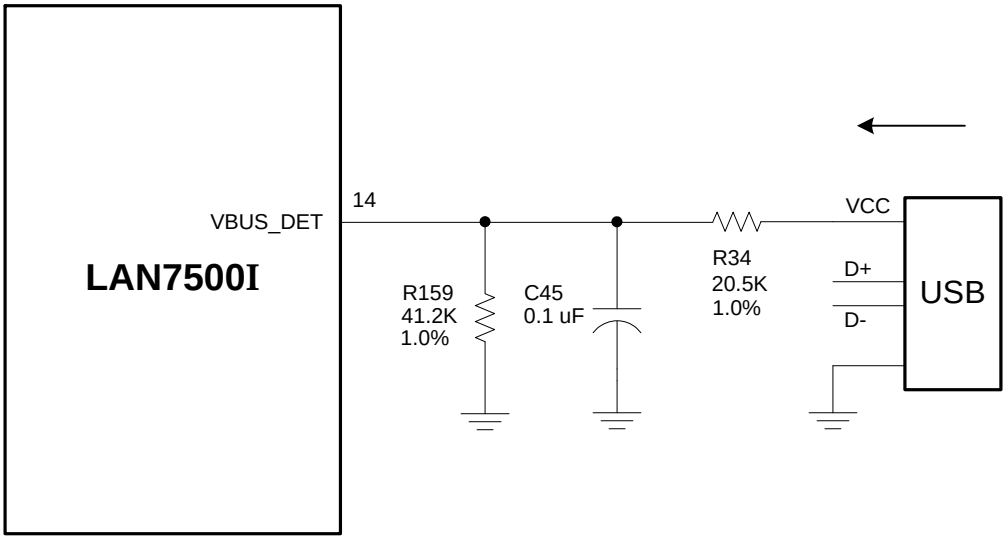



**Figure 4 - Self-Powered Mode Circuitry**

## Miscellaneous:

1. nRESET (pin 42), this pin is an active-low reset input. This signal resets all logic and registers within the LAN7500I. This signal is pulled high with a weak internal pull-up resistor. The nRESET should not be left unconnected as the +3.3V internal power-on reset circuitry is RC based. SMSC strongly recommends the use of an external POR for the nRESET pin.

2. SW_MODE (pin 9), when asserted, this output of the LAN7500I places an external switching regulator into a power savings mode.

3. LED0 (pin 31), LED1 (pin 32), LED2 (pin 33), LED3 (pin 34) & LED4 (pin 35), can be programmed via register settings to display various Ethernet activity such as Speed, Link & Duplex Status. See the latest version of the LAN7500I data sheet for complete details.

4. The LAN7500I has an IEEE 1149.1 compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board level testing to ensure system functionality and board manufacturability. For details, see the LAN7500I data sheet.

5. TEST (pin 39), this pin must be tied directly to digital ground in order to ensure proper operation.

6. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

7. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

8. In order to guarantee IEEE compliancy over the entire temperature range of operation, all components used in the customer's application must be rated for Industrial Temperature use. Processors, crystals, oscillators, magnetics and all integrated circuits must be rated properly to avoid operational inconsistencies.

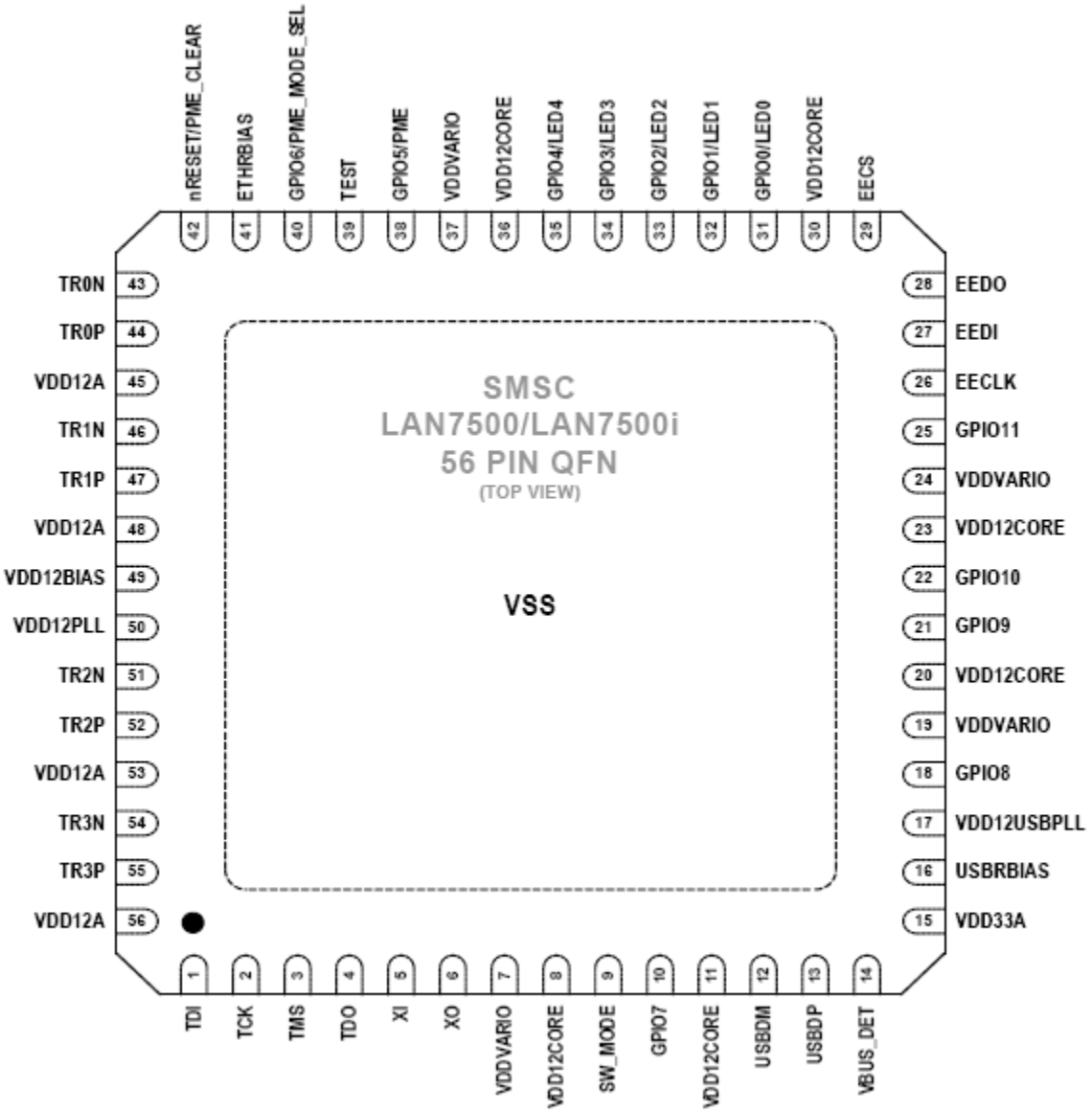
## LAN7500I QFN QuickCheck Pinout Table:

Use the following table to check the LAN7500I QFN shape in your schematic.

| LAN7500I QFN | | | |
|---|---|---|---|
| **Pin No.** | **Pin Name** | **Pin No.** | **Pin Name** |
| 1 | TDI | 29 | EECS |
| 2 | TCK | 30 | VDD12CORE |
| 3 | TMS | 31 | GPIO0 / LED0 |
| 4 | TDO | 32 | GPIO1 / LED1 |
| 5 | XI | 33 | GPIO2 / LED2 |
| 6 | XO | 34 | GPIO3 / LED3 |
| 7 | VDDVARIO | 35 | GPIO4 / LED4 |
| 8 | VDD12CORE | 36 | VDD12CORE |
| 9 | SW_MODE | 37 | VDDVARIO |
| 10 | GPIO7 | 38 | GPIO5 / PME |
| 11 | VDD12CORE | 39 | TEST |
| 12 | USBDM | 40 | GPIO6 / PME_MODE_SEL |
| 13 | USBDP | 41 | ETHRBIAS |
| 14 | VBUS_DET | 42 | nRESET / PME_CLEAR |
| 15 | VDD33A | 43 | TR0N |
| 16 | USBRBIAS | 44 | TR0P |
| 17 | VDD12USBPLL | 45 | VDD12A |
| 18 | GPIO8 | 46 | TR1N |
| 19 | VDDVARIO | 47 | TR1P |
| 20 | VDD12CORE | 48 | VDD12A |
| 21 | GPIO9 | 49 | VDD12BIAS |
| 22 | GPIO10 | 50 | VDD12PLL |
| 23 | VDD12CORE | 51 | TR2N |
| 24 | VDDVARIO | 52 | TR2P |
| 25 | GPIO11 | 53 | VDD12A |
| 26 | EECLK | 54 | TR3N |
| 27 | EEDI | 55 | TR3P |
| 28 | EEDO | 56 | VDD12A |
| **57** | | **EDP Ground Connection<br>Exposed Die Paddle Ground<br>Pad on Bottom of Package** | |

## Notes:

## LAN7500I QFN Package Drawing:



## Reference Material:

1. SMSC LAN7500I Data Sheet; check web site for latest revision.
2. SMSC LAN7500I CEB Schematic, Assembly No. 6588 ; check web site for latest revision.
3. SMSC LAN7500I CEB PCB, Assembly No. 6588 ; order PCB from web site.
4. SMSC LAN7500I CEB PCB Bill of Materials, Assembly No. 6588 ; check web site for latest revision.
5. CEB stands for Customer Evaluation Board.
6. SMSC LAN7500I Reference Design, check web site for latest revision.
7. SMSC Reference Designs are schematics only; there are no associated PCBs.
8. For Qualified / Suggested Magnetics, use these two links to the SMSC LANCheck website:

https://www2.smsc.com/mkt/web_lancheck.nsf/MagList?OpenForm

https://www2.smsc.com/mkt/web_lancheck.nsf/MagCheck?OpenForm