

## ZL30291/ZL30292 Power Supply Decoupling Recommendations

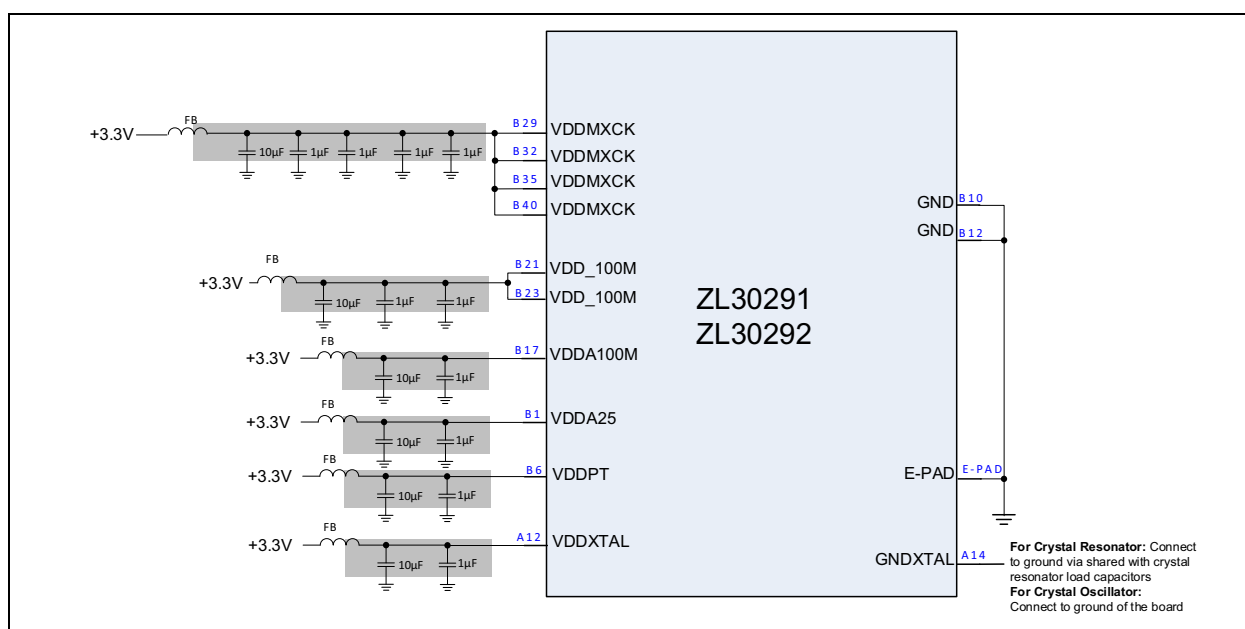
### INTRODUCTION

ZL30291 is PCIe clock and Platform Timing generator that is fully compatible with the Intel CK440Q standard. ZL30292 is an identical device to ZL30291 where the only difference is that the embedded output series resistors are set for differential transmission lines with 100Ω characteristic impedance.

This document details the recommended power supply decoupling and device layout practices for ZL30291/292 devices.

### POWER DECOUPLING

Jitter levels on the device output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise as shown in [Figure 1](#).



**FIGURE 1:** ZL30291/ZL30292 Crystal Oscillator Circuit.

The following common layout practices are recommended for improved power rail noise rejection:

- A number of “power islands” could be created for the device to improve isolation from the noise present on power planes and to reduce coupling between different supply pins. This is not mandatory, but it might improve jitter performance for the noise board. A power island is a local copper area, separated from the main power plane by a series passive component (1Ω to 2Ω resistor or ferrite bead with maximum impedance at 100 MHz). Power islands are shown as shaded areas in [Figure 1](#).
- Each power island should have a bulk capacitor of 10 µF. It is recommended to use ceramic bulk capacitors (X5R or X7R) with low ESR and ESL. Typically, smaller the size of capacitor the lower the ESR and ESL are:
  - Smallest possible 1 µF decoupling ceramic capacitors (X5R or X7R) with low ESR and ESL should be placed as close as possible to each power pin.
  - EPAD should be connected to ground with a minimum 5 x 5 via matrix.

NOTES:

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