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A	Release		6-12-15
B	Corrected E2PSIZE Configuration Strap Information, Page 23		10-15-15

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DOCUMENT DESCRIPTION
Schematic Checklist for the LAN9252, 64-pin SQFN Package

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	Document Number	Revision
	SC471248	B

Schematic Checklist for LAN9252

Information Particular for the 64-pin SQFN Package

LAN9252 SQFN Port A Copper Twisted Pair Phy Interface:

1. TXPA (pin 53); This pin is the transmit twisted pair output positive connection from the primary internal Phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33TXRX1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.
2. TXNA (pin 52); This pin is the transmit twisted pair output negative connection from the primary internal Phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33TXRX1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.
3. For Port A, Transmit Channel connection and termination details, refer to Figure 1.
4. RXPA (pin 55); This pin is the receive twisted pair input positive connection to the primary internal Phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33TXRX1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.
5. RXNA (pin 54); This pin is the receive twisted pair input negative connection to the primary internal Phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33TXRX1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.
6. For Port A, Receive Channel connection and termination details, refer to Figure 2.
7. For added EMC flexibility in a LAN9252 design, the designer should include four low valued capacitors on the TXPA, TXNA, RXPA & RXNA pins. Low valued capacitors (less than 22 pF) can be added to each line and terminated to digital ground. These components can be added to the schematic and should be designated as Do Not Populate (DNP).



LAN9252 SQFN Port B Copper Twisted Pair Phy Interface:

1. TXPB (pin 62); This pin is the transmit twisted pair output positive connection from the secondary internal Phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33TXRX2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.
2. TXNB (pin 63); This pin is the transmit twisted pair output negative connection from the secondary internal Phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33TXRX2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.
3. For Port B, Transmit Channel connection and termination details, refer to Figure 1.
4. RXPB (pin 60); This pin is the receive twisted pair input positive connection to the secondary internal Phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33TXRX2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.
5. RXNB (pin 61); This pin is the receive twisted pair input negative connection to the primary internal Phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33TXRX2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.
6. For Port B, Receive Channel connection and termination details, refer to Figure 2.
7. For added EMC flexibility in a LAN9252 design, the designer should include four low valued capacitors on the TXPB, TXNB, RXPB & RXNB pins. Low valued capacitors (less than 22 pF) can be added to each line and terminated to digital ground. These components can be added to the schematic and should be designated as Do Not Populate (DNP).



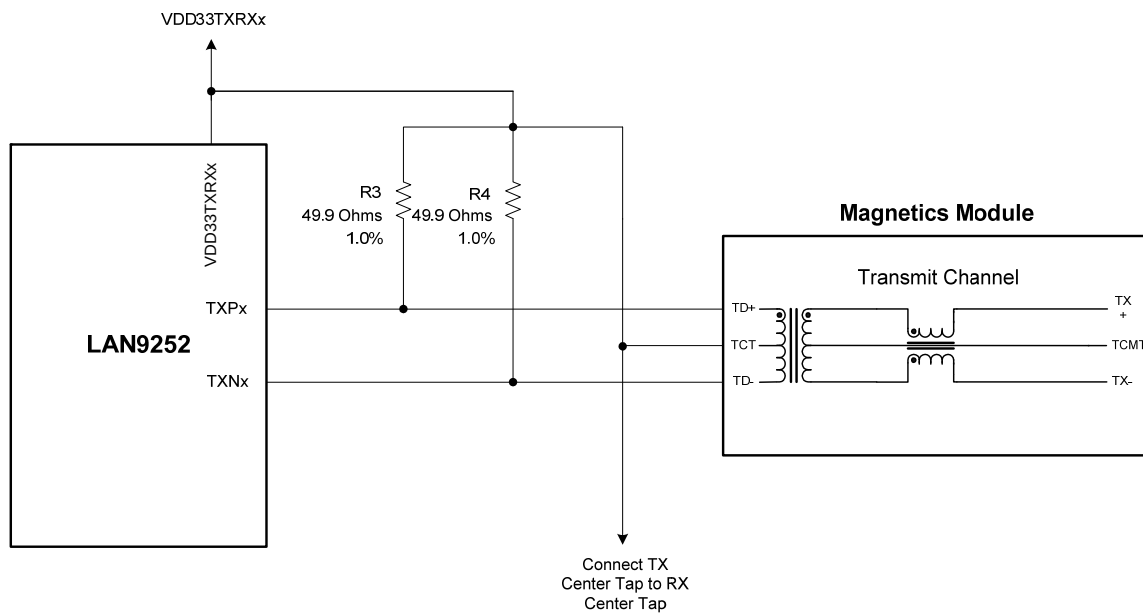


Figure 1 – Transmit Channel Connections and Terminations

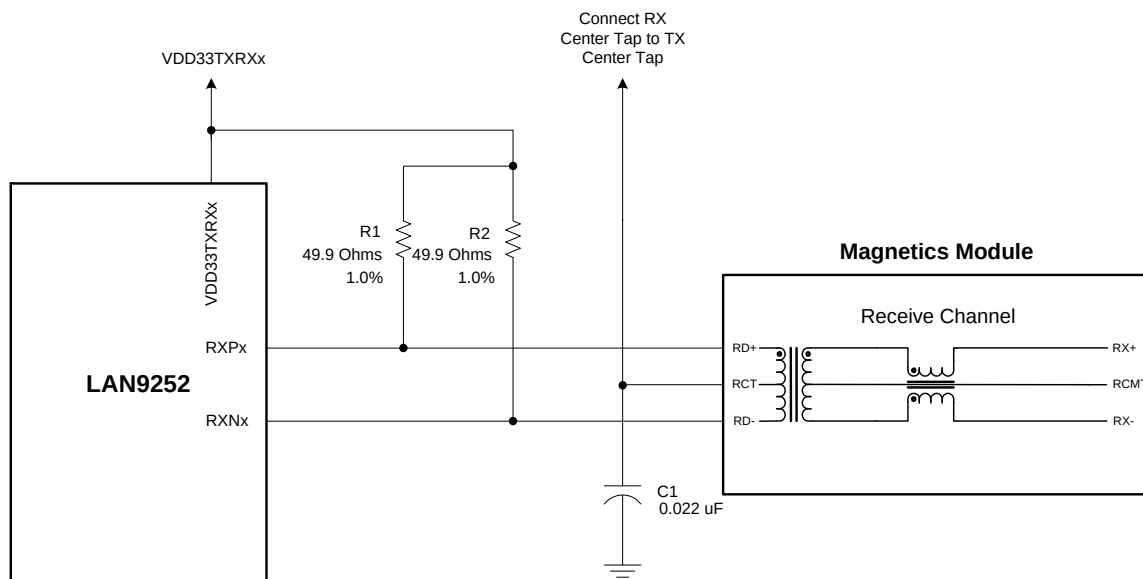


Figure 2 - Receive Channel Connections and Terminations

LAN9252 SQFN Port A Copper Twisted Pair Phy Magnetics:

1. The center tap connection on the LAN9252 side for the transmit channel must be connected to VDD33TXRX1 (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.
2. The center tap connection on the LAN9252 side for the receive channel is connected to the transmit channel center tap on the primary magnetics. In addition, a 0.022 μ F capacitor is required from the receive channel center tap of the primary magnetics to digital ground.
3. The center tap connection on the cable side (RJ45 side) for the primary transmit channel should be terminated with a 75 Ω resistor through a 1000 pF, 2KV capacitor ($C_{magterm}$) to chassis ground.
4. The center tap connection on the cable side (RJ45 side) for the primary receive channel should be terminated with a 75 Ω resistor through a 1000 pF, 2KV capacitor ($C_{magterm}$) to chassis ground.
5. Only one 1000 pF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.
6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXPA (pin 53) of the LAN9252 SQFN.
7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXNA (pin 52) of the LAN9252 SQFN.
8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXPA (pin 55) of the LAN9252 SQFN.
9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXNA (pin 54) of the LAN9252 SQFN.
10. When using the LAN9252 in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the Reference Material section of this document for proper magnetics.



LAN9252 SQFN Port B Copper Twisted Pair Phy Magnetics:

1. The center tap connection on the LAN9252 side for the transmit channel must be connected to VDD33TXRX2 (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.
2. The center tap connection on the LAN9252 side for the receive channel is connected to the transmit channel center tap on the secondary magnetics. In addition, a 0.022 μ F capacitor is required from the receive channel center tap of the secondary magnetics to digital ground.
3. The center tap connection on the cable side (RJ45 side) for the secondary transmit channel should be terminated with a 75 Ω resistor through a 1000 ρ F, 2KV capacitor ($C_{magterm}$) to chassis ground.
4. The center tap connection on the cable side (RJ45 side) for the secondary receive channel should be terminated with a 75 Ω resistor through a 1000 ρ F, 2KV capacitor ($C_{magterm}$) to chassis ground.
5. Only one 1000 ρ F, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.
6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXPB (pin 62) of the LAN9252 SQFN.
7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXNB (pin 63) of the LAN9252 SQFN.
8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXPB (pin 60) of the LAN9252 SQFN.
9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXNB (pin 61) of the LAN9252 SQFN.
10. When using the LAN9252 in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the Reference Material section of this document for proper magnetics.



Copper Twisted Pair RJ45 Connectors Ports A & B:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:
 - a) Pins 4 & 5 can be connected together with two 49.9 Ω resistors. The common connection of these resistors should be connected through a third 49.9 Ω to the 1000 pF, 2KV capacitor (C_{rjterm}).
 - b) For a lower component count, the resistors can be combined. The two 49.9 Ω resistors in parallel look like a 25 Ω resistor. The 25 Ω resistor in series with the 49.9 Ω makes the whole circuit look like a 75 Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75 Ω resistor in series with the 1000 pF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.
2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:
 - a) Pins 7 & 8 can be connected together with two 49.9 Ω resistors. The common connection of these resistors should be connected through a third 49.9 Ω to the 1000 pF, 2KV capacitor (C_{rjterm}).
 - b) For a lower component count, the resistors can be combined. The two 49.9 Ω resistors in parallel look like a 25 Ω resistor. The 25 Ω resistor in series with the 49.9 Ω makes the whole circuit look like a 75 Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75 Ω resistor in series with the 1000 pF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.
3. The RJ45 shield should be attached directly to chassis ground.



LAN9252 SQFN Port A Fiber Phy (100BASE-FX) Interface:

1. TXPA (pin 53); This pin is the Port A Fiber transmit positive output pin. This low voltage PECL output pin should connect to the external fiber transceiver in the design.
2. TXNA (pin 52); This pin is the Port A Fiber transmit negative output pin. This low voltage PECL output pin should connect to the external fiber transceiver in the design.
3. For Port A, Fiber Transmit Channel connection details, refer to Figure 1.
4. RXPA (pin 55); This pin is the Port A Fiber receive positive input pin. This analog input pin should connect to the external fiber transceiver in the design.
5. RXNA (pin 54); This pin is the Port A Fiber receive negative input pin. This analog input pin should connect to the external fiber transceiver in the design.
6. For Port A, Fiber Receive Channel connection details, refer to Figure 2.
7. FXSDA (pin 9); Port A Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external fiber transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.
8. FXLOSA (pin 9); Port A Fiber Loss of Signal. When FX-LOS mode is selected, this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.
9. **Architecture Note:** 100BASE-FX is a version of Fast Ethernet over optical fiber. It uses a 1300 nm near-infrared (NIR) light wavelength transmitted via two strands of optical fiber, one for receive(RX) and the other for transmit(TX). Maximum length is 412 metres (1,350 ft) for half-duplex connections (to ensure collisions are detected), and 2 kilometres (6,600 ft) for full-duplex over multi-mode optical fiber. EtherCAT® uses full-duplex mode. 100BASE-FX uses the same 4B5B encoding and NRZI line code that 100BASE-TX does. 100BASE-FX should use SC, ST, LC, MTRJ or MIC connectors with SC being the preferred option.



LAN9252 SQFN Port B Fiber Phy (100BASE-FX) Interface:

1. TXPB (pin 62); This pin is the Port B Fiber transmit positive output pin. This low voltage PECL output pin should connect to the fiber transceiver in the design.
2. TXNB (pin 63); This pin is the Port B Fiber transmit negative output pin. This low voltage PECL output pin should connect to the fiber transceiver in the design.
3. For Port B, Fiber Transmit Channel connection details, refer to Figure 1.
4. RXPB (pin 60); This pin is the Port B Fiber receive positive input pin. This analog input pin should connect to the fiber transceiver in the design.
5. RXNB (pin 61); This pin is the Port B Fiber receive negative input pin. This analog input pin should connect to the fiber transceiver in the design.
6. For Port B, Fiber Receive Channel connection details, refer to Figure 2.
7. FXSDB (pin 10); Port B Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external fiber transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.
8. FXLOSB (pin 10); Port B Fiber Loss of Signal. When FX-LOS mode is selected, this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.
9. **Architecture Note:** 100BASE-FX is a version of Fast Ethernet over optical fiber. It uses a 1300 nm near-infrared (NIR) light wavelength transmitted via two strands of optical fiber, one for receive(RX) and the other for transmit(TX). Maximum length is 412 metres (1,350 ft) for half-duplex connections (to ensure collisions are detected), and 2 kilometres (6,600 ft) for full-duplex over multi-mode optical fiber. EtherCAT® uses full-duplex mode. 100BASE-FX uses the same 4B5B encoding and NRZI line code that 100BASE-TX does. 100BASE-FX should use SC, ST, LC, MTRJ or MIC connectors with SC being the preferred option.



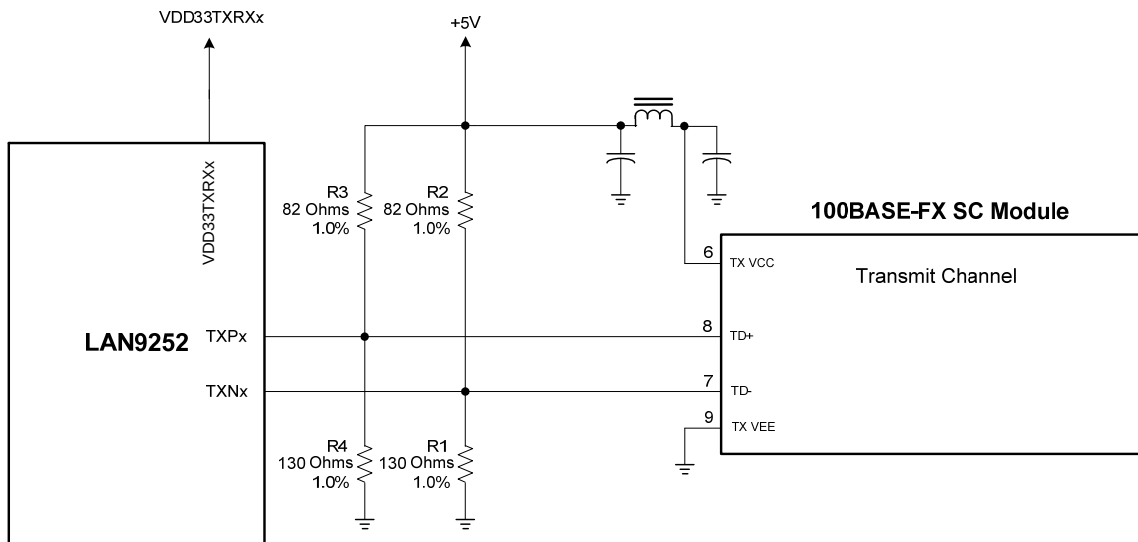


Figure 3 – Fiber Transmit Channel Connections

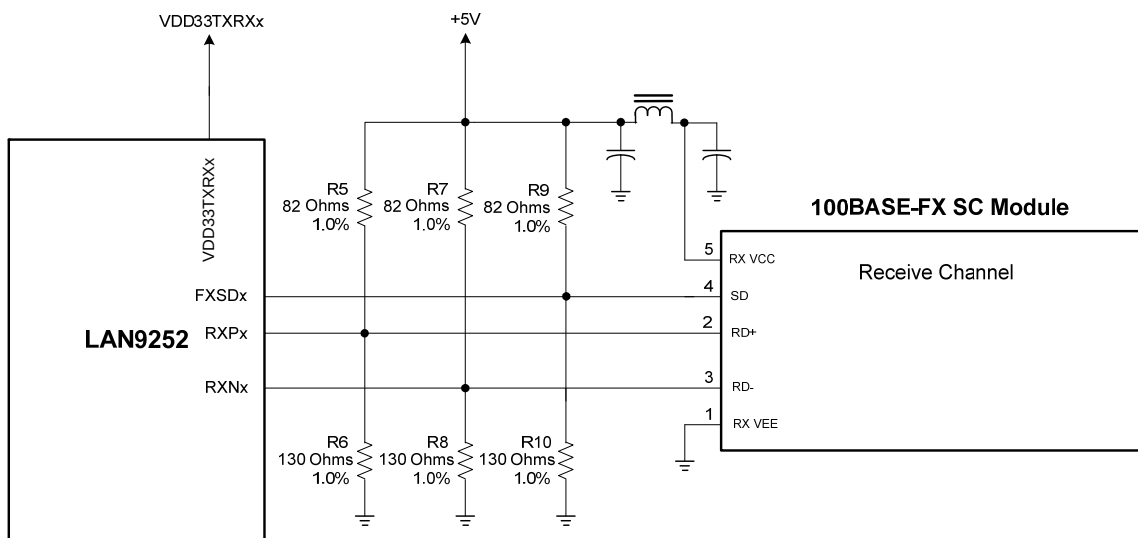


Figure 4 – Fiber Receive Channel Connections

CTP / FX-SD / FX-LOS Configuration Pins:

1. FXLOSEN (pin 8) is a tri-level configuration strap input that selects between FX-LOS and FX-SD / Copper Twisted Pair mode. The voltage levels are as follows:

Below +1 V = Selects FX-SD / Copper Twisted Pair for Ports A and B, further determined by FXSDENA and FXSDENB.

+1.5 V = Selects FX-LOS for Port A and FXSD / copper twisted pair for Port B, further determined by FXSDENB.

Above +2 V = Selects FX-LOS for Ports A and B.

A pull-up / pull-down resistor value of 10K is recommended in order to attain the required high / low voltage levels listed above. A voltage divider of two 10K resistors can be used for the middle, +1.5 V level listed above.

2. FXSDENA (pin 9), when FX-LOS mode is not selected, this configuration strap input selects between FX-SD and Copper Twisted Pair mode. When FX-LOS mode is selected, this input configuration strap is disabled.

Below +1V = Selects Copper Twisted Pair mode for Port A.

Above +1 V = Selects FX-SD fiber mode for Port A.

A pull-up / pull-down resistor value of 10K is recommended in order to attain the required high / low voltage levels listed above.

3. FXSDENB (pin 10), when FX-LOS mode is not selected, this configuration strap input selects between FX-SD and Copper Twisted Pair mode. When FX-LOS mode is selected, this input configuration strap is disabled.

Below +1V = Selects Copper Twisted Pair mode for Port B.

Above +1 V = Selects FX-SD fiber mode for Port B.

A pull-up / pull-down resistor value of 10K is recommended in order to attain the required high / low voltage levels listed above.



+3.3V Power Supply Connections:

1. The supply for the two internal regulators on the LAN9252 SQFN is pin 5 (VDD33). This pin requires a connection to +3.3V. **Note:** +3.3V must be supplied to this pin even if the internal regulators are disabled.
2. The VDD33 power pin should have one .01 μ F (or smaller) capacitor to decouple the LAN9252. The capacitor size should be SMD_0603 or smaller.
3. The analog supply (VDD33TXRX1) pin on the LAN9252 SQFN is pin 51. It requires a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
4. The VDD33TXRX1 pin should have one .01 μ F (or smaller) capacitor to decouple the LAN9252. The capacitor size should be SMD_0603 or smaller.
5. The analog supply (VDD33TXRX2) pin on the LAN9252 SQFN is pin 64. It requires a connection to +3.3V through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
6. The VDD33TXRX2 pin should have one .01 μ F (or smaller) capacitor to decouple the LAN9252. The capacitor size should be SMD_0603 or smaller.
7. VDD33BIAS (pin 58), this pin serves as the master bias voltage supply for the LAN9252. This pin requires a connection to +3.3V through a third ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
8. The VDD33BIAS pin should have one .01 μ F (or smaller) capacitor to decouple the LAN9252. The capacitor size should be SMD_0603 or smaller.

+1.8V to +3.3V Variable I/O Power Supply Connections:

1. The variable I/O supply (VDDIO) pins on the LAN9252 SQFN are 14, 20, 32, 37 & 47. They require an externally supplied voltage supply between +1.8V and +3.3V.
2. Each VDDVARIO pin should have one .01 μ F (or smaller) capacitor to decouple the LAN9252. The capacitor size should be SMD_0603 or smaller.



VDDCR:

1. VDDCR (pins 6, 24 & 38), these three pins are used to provide bypassing for the +1.2V core regulator. Each pin requires a 0.01 μ F decoupling capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 6 requires a bulk capacitor placed as close as possible to pin 6. The bulk capacitor must have a value of at least 1.0 μ F, and have an ESR (equivalent series resistance) of no more than 2.0 Ω . Microchip recommends a very low ESR ceramic capacitor for design stability. In addition, pin 6 also requires a 470 pF bypass capacitor. Other values, tolerances & characteristics are not recommended.

Caution: This +1.2V supply is for internal logic only. **Do Not** power other external circuits or devices with this supply.

2. VDD12TX1 (pin 56) and VDD12TX2 (pin 59), these pins supply power for the two Ethernet blocks. These two pins must be tied together. These two pins must be connected to VDDCR through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
3. The VDD12TX1 and VDD12TX2 pins should each have one .01 μ F (or smaller) capacitor to decouple the LAN9252. The capacitor size should be SMD_0603 or smaller.

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN9252 SQFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN9252 must be connected directly to a solid, contiguous digital ground plane.
2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.



Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9252 SQFN. For exact specifications and tolerances refer to the latest revision LAN9252 data sheet.
2. OSCI (pin 1) on the LAN9252 SQFN is the clock circuit input. This pin requires a 27 – 33 pF capacitor to digital ground. One side of the crystal connects to this pin.
3. OSCO (pin 2) on the LAN9252 SQFN is the clock circuit output. This pin requires a matching 27 – 33 pF capacitor to ground and the other side of the crystal.
4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.
5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN9252 SQFN.
6. OSCVDD12 (pin 3), this pin is supplied by one of the internal +1.2V regulators of the LAN9252 and can be left as a no-connection in this mode (REGEN = high). When REGEN = low, this pin must be supplied by an external +1.2V power supply.
7. OSCVSS (pin 4), this pin should be connected directly to digital ground for all applications.
8. **Design Verification Tip:** Microchip recommends taking advantage of the Clock Output Test Mode in the LAN9252. In order to facilitate system level validation and debug, the crystal clock can be enabled onto the IRQ pin by setting the IRQ Clock Select (IRQ_CLK_SELECT) bit of the Interrupt Configuration Register (IRQ_CFG). The IRQ pin should be set to a push-pull driver by using the IRQ Buffer Type (IRQ_TYPE) bit for the best result. Be sure to include a test pin on the IRQ pin (pin 44) and a ground pin close to the test pin. Using a high-quality, precise frequency counter with 8-digits or better will accurately determine the frequency of the 25.000 MHz in the design. Adjusting the crystal circuit load caps slightly will fine tune the frequency of the circuit.

RBIAS Resistor:

1. RBIAS (pin 57) on the LAN9252 SQFN should connect to digital ground through a 12.1K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.



Required External Pull-ups/Pull-downs:

1. IRQ (pin 44) may require an external pull-up resistor to VDDIO if configured as an Open Drain type.
2. When using the MII interface of the LAN9252 with an external Phy device on board, a pull-up resistor on the MII_MDIO signal (pin 40) is required. A pull-up resistor of 1.5K Ω to VDDIO is required for this application.

MII Interface:

1. When utilizing either an external MII Phy or an MII connector, the following table indicates the proper connections for the 14 signals.

From:		Connects To:
LAN9252 SQFN	MII Phy Device	MII Connector
RXD0 (pin 27)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 28)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 30)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 31)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 26)	RX_DV	RX_DV (contact 8)
RX_ER (pin 33)	RX_ER	RX_ER (contact 10)
RX_CLK (pin 36)	RX_CLK	RX_CLK (contact 9)
	TX_ER	TX_ER (contact 11)
TXD0 (pin 22)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 21)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 16)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 15)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin 23)	TX_EN	TX_EN (contact 13)
	TX_CLK	TX_CLK (contact 12)
	CRS	CRS (contact 19)
	COL	COL (contact 18)
MDIO (pin 40)	MDIO	MDIO (contact 2)
MDC (pin 39)	MDC	MDC (contact 3)

MII Interface:

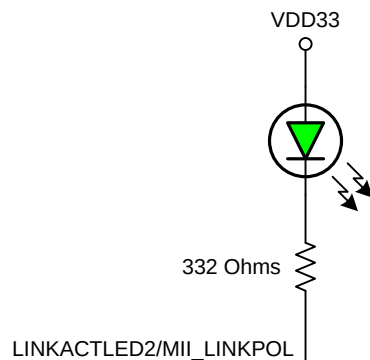
2. MII_CLK25 (pin 25) is a free-running 25 MHz clock that can be used as the clock input to the external Phy.
3. TX_CLK from the external Phy is not connected since the EtherCAT® Slave does not incorporate a TX FIFO. The TX signals from the EtherCAT® Slave may be delayed with respect to the CLK25 output by using TX shift compensation so that they align properly as if they were driven by the PHY's TX_CLK.
4. The COL and CRS outputs from the Phy are not connected since EtherCAT® operates in full-duplex mode.
5. The TX_ER input on the external Phy should be tied to digital ground as the EtherCAT® Slave will never generate any transmit errors.
6. MII_LINK (pin 49) This input pin on the LAN9252 is driven by the external Phy to indicate that a 100 Mbit/s Full Duplex link is established. The polarity is configurable via the MII_LINKPOL strap.
7. Provisions should be made for series terminations for all outputs on the MII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN9252 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependant and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 10.0 Ω .
8. TX_SHIFT1 (pin 15) & TX_SHIFT0 (pin 16), these two pins configure the value of the MII TX timing shift for the MII port of the LAN9252. The shift in timing are as follows:

00 =	0 nS
01 =	10 nS
10 =	20 nS
11 =	30 nS

See the latest version of the LAN9252 data sheet for complete details. These pins have weak internal pull-ups and can be driven low with an external 4.7K Ω resistor to digital ground. If driven, these two input configuration strap pins require an external 4.7K Ω pull-up resistor to ensure the proper high level is maintained.



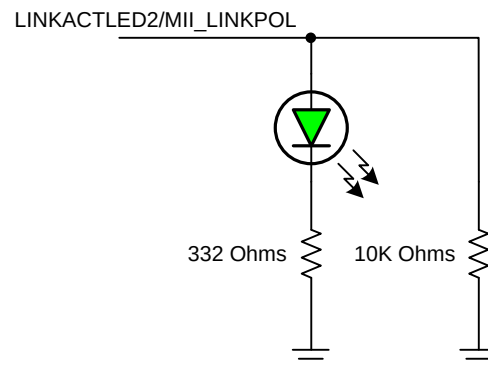
9. MII_LINKPOL (pin 29), this strap pin configures the polarity of the MII_LINK pin (pin 49). When latched low, MII_LINK low indicates a 100BASE-TX Full Duplex link has been established. When latched high, MII_LINK high indicates a 100BASE-TX Full Duplex link has been established. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.



MII_LINKPOL Bit = 1

**LED Output Signal from
LAN9252 is Active Low**

**MII_LINK High = 100BASE-TX
Full Duplex Link**



MII_LINKPOL Bit = 0

**LED Output Signal from
LAN9252 is Active High**

**MII_LINK Low = 100BASE-TX
Full Duplex Link**

Host Bus Interface (HBI) Indexed Mode pins:

1. RD (pin 31) This pin is the host bus read strobe. Normally active low, the polarity can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI Modes).
2. WR (pin 30) This pin is the host bus write strobe. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI Modes).
3. RD_WR (pin 31) This pin is the host bus direction control. Used in conjunction with the ENB pin, it indicates a read or write operation. The normal polarity is read when 1, write when 0 (R/nW) but can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI Modes).
4. ENB (pin 30) This pin is the host bus data enable strobe. Used in conjunction with the RD_WR pin it indicates the data phase of the operation. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI Modes).
5. CS (pin 28) This pin is the host bus chip select and indicates that the device is selected for the current transfer. Normally active low, the polarity can be changed via the HBI Chip Select Polarity bit of the PDI Configuration Register (HBI Modes).
6. A[4:0] (pins 27, 26, 29, 25, 33) These pins provide the address for non-multiplexed address mode. In 16-bit data mode, bit 0 is not used.
7. D[15:0] (pins 33, 15, 16, 21, 22, 23, 19, 40, 39, 36, 50, 49, 35, 12, 13, 17) These pins are the host bus data bus for non-multiplexed address mode. In 8-bit data mode, bits 15-8 are not used and their input and output drivers are disabled.



Host Bus Interface (HBI) Multiplexed Mode pins:

1. RD (pin 31) This pin is the host bus read strobe. Normally active low, the polarity can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI Modes).
2. WR (pin 30) This pin is the host bus write strobe. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI Modes).
3. RD_WR (pin 31) This pin is the host bus direction control. Used in conjunction with the ENB pin, it indicates a read or write operation. The normal polarity is read when 1, write when 0 (R/nW) but can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI Modes).
4. ENB (pin 30) This pin is the host bus data enable strobe. Used in conjunction with the RD_WR pin it indicates the data phase of the operation. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI Modes).
5. CS (pin 28) This pin is the host bus chip select and indicates that the device is selected for the current transfer. Normally active low, the polarity can be changed via the HBI Chip Select Polarity bit of the PDI Configuration Register (HBI Modes).
6. AD[15:0] (pins 33, 15, 16, 21, 22, 23, 19, 40, 39, 36, 50, 49, 35, 12, 13, 17) These pins are the host bus address / data bus for multiplexed address mode. Bits 15-8 provide the upper byte of address for single phase multiplexed address mode. Bits 7-0 provide the lower byte of address for single phase multiplexed address mode and both bytes of address for dual phase multiplexed address mode. In 8-bit data dual phase multiplexed address mode, bits 15-8 are not used and their input and output drivers are disabled.
7. ALEHI (pin 29) This pin indicates the address phase for multiplexed address modes. It is used to load the higher address byte in dual phase multiplexed address mode. Normally active low (address saved on rising edge), the polarity can be changed via the HBI ALE Polarity bit of the PDI Configuration Register (HBI Modes).
8. ALELO (pin 25) This pin indicates the address phase for multiplexed address modes. It is used to load both address bytes in single phase multiplexed address mode and the lower address byte in dual phase multiplexed address mode. Normally active low (address saved on rising edge), the polarity can be changed via the HBI ALE Polarity bit of the PDI Configuration Register (HBI Modes).



EtherCAT® Digital I/O Mode pins:

1. SOF (pin 12) This pin is the Start of Frame output and indicates the start of an Ethernet/EtherCAT® frame. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
2. EOF (pin 13) This pin is the End of Frame output and indicates the end of an Ethernet/EtherCAT® frame. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
3. WD_STATE (pin 17) This pin is the SyncManager Watchdog State output. A 0 indicates the watchdog has expired. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
4. WD_TRIG (pin 35) This pin is the SyncManager Watchdog Trigger output. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
5. LATCH_IN (pin 19) This input pin is the external data latch signal. The input data is sampled each time a rising edge of LATCH_IN is recognized.
6. OE_EXT (pin 25) This input pin is the Output Enable signal. When low, it clears the output data.
7. OUT_VALID (pin 50) This pin indicates that the outputs are valid and can be captured into external registers. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
8. DIGIO[15:0] (pins 31, 30, 28, 27, 26, 29, 33, 15, 16, 21, 22, 23, 49, 40, 39, 36) These pins are the input/output or bidirectional data. **Note:** These signals are not driven (high impedance) until the EEPROM is loaded.



Serial Peripheral Interface (SPI) Bus pins:

1. SI (pin 17) This pin is the SPI slave serial data input. SI is shared with the SIO0 pin. This input pin has an internal pull-up.
2. SO (pin 13) This pin is the SPI slave serial data output. SO is shared with the SIO1 pin. This output pin has an internal pull-up.
3. SCK (pin 19) This pin is the SPI/SQI slave serial clock input. This input pin has an internal pull-up.
4. SCS# (pin 50) This pin is the SPI/SQI slave chip select input. When low, the SPI/SQI slave is selected for SPI/SQI transfers. When high, the SPI/SQI serial data output(s) is(are) 3-stated. This input has an internal pull-up.
5. SIO[3:0] (pins 35, 12, 13, 17) These pins are the SPI/SQI slave data input and output for multiple bit I/O. These bi-directional pins have internal pull-ups. SIO0 is shared with the SI pin. SIO1 is shared with the SO pin.

GPI pins:

1. GPI[15:0] (pins 31, 30, 28, 27, 26, 29, 33, 15, 16, 21, 22, 23, 49, 40, 39, 36) These pins are the general purpose inputs and are directly mapped into the General Purpose Inputs Register. Consistency of the general purpose inputs is not provided.

GPO pins:

1. GPO[15:0] (pins 31, 30, 28, 27, 26, 29, 33, 15, 16, 21, 22, 23, 49, 40, 39, 36) These pins are the general purpose outputs and reflect the values of the General Purpose Outputs Register without watchdog protection. **Note:** These signals are not driven (high impedance) until the EEPROM is loaded.

LED pins:

1. LINKACTLED2 (pin 29) This pin is the Link/Activity LED output (off=no link, on=link without activity, blinking=link and activity) for Port 2. This pin is configured to be an open-drain/open source output. The choice of open-drain vs. open source as well as the polarity of this pin depends upon the strap value sampled at reset. **Note:** Refer to Section 12.10, "LEDs," for additional information.
2. RUNLED (pin 45) This pin is the Run LED output and is controlled by the AL Status Register. This pin is configured to be open-drain/open-source output. The choice of open-drain vs. open-source as well as the polarity of this pin depends upon the strap value sampled at reset. **Note:** Refer to Section 12.10, "LEDs," for additional information.
3. LINKACTLED1 (pin 46) This pin is the Link/Activity LED output (off=no link, on=link without activity, blinking=link and activity) for Port 1. This pin is configured to be open-drain/open-source output. The choice of open-drain vs. open-source as well as the polarity of this pin depends upon the strap value sampled at reset. **Note:** Refer to Section 12.10, "LEDs," for additional information.
4. LINKACTLED0 (pin 48) This pin is the Link/Activity LED output (off=no link, on=link without activity, blinking=link and activity) for Port 0. This pin is configured to be open-drain/open-source output. The choice of open-drain vs. open-source as well as the polarity of this pin depends upon the strap value sampled at reset. **Note:** Refer to Section 12.10, "LEDs," for additional information.

SYNC / LATCH pins:

1. SYNC1 / LATCH1 (pin 18) These pins are the Distributed Clock Sync (OUT) or Latch (IN) signals. The direction is bitwise configurable. **Note:** These signals are not driven (high impedance) until the EEPROM is loaded.
2. SYNC0 / LATCH0 (pin 34) These pins are the Distributed Clock Sync (OUT) or Latch (IN) signals. The direction is bitwise configurable. **Note:** These signals are not driven (high impedance) until the EEPROM is loaded.

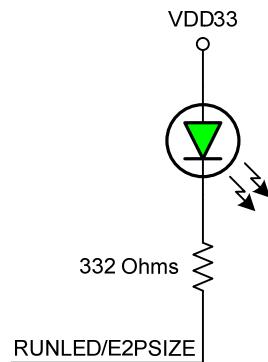


I²C EEPROM pins:

1. EESDA (pin 42) When the device is accessing an external EEPROM, this pin is the I²C serial data input/open-drain output. **Note:** This pin must be pulled-up by a 10K ohm external resistor at all times.
2. EESCL (pin 43) When the device is accessing an external EEPROM this pin is the I²C clock open-drain output. **Note:** This pin must be pulled-up by a 10K ohm external resistor at all times.
3. For EtherCAT® operation, an EEPROM is required. Please review the EEPROM Configurable Register section in the LAN9252 data sheet for what specific design functionality is loaded from the EEPROM.

Dedicated Configuration Strap Pins:

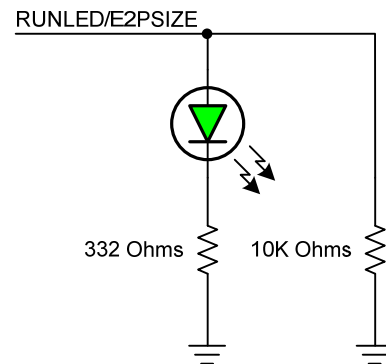
1. E2PSIZE (pin 45), this strap pin configures the I²C EEPROM size. When latched low, EEPROM sizes 128 x 8-bit (1K) through 2048 x 8-bit (16K) are supported. When latched high, EEPROM sizes 4096 x 8-bit (32K) through 512K x 8-bit (4M) are supported. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.



E2PSIZE Bit = 1

**LED Output Signal from
LAN9252 is Active Low**

**32K – 4M EEPROMs
Supported**



E2PSIZE Bit = 0

**LED Output Signal from
LAN9252 is Active High**

**1K – 16K EEPROMs
Supported**

2. CHIP_MODE1 (pin 46) & CHIP_MODE0 (pin 48), these two pins configure the number of active ports and port types of the LAN9252. The modes are as follows:

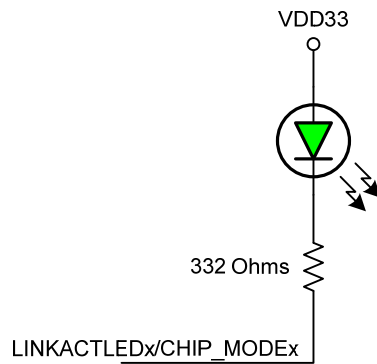
00 = 2 port mode; Ports 0 and 1 are connected to internal Phys A and B.

01 = Reserved

10 = 3 port downstream mode. Ports 0 and 1 are connected to internal PHYs A and B. Port 2 is connected to the external MII pins.

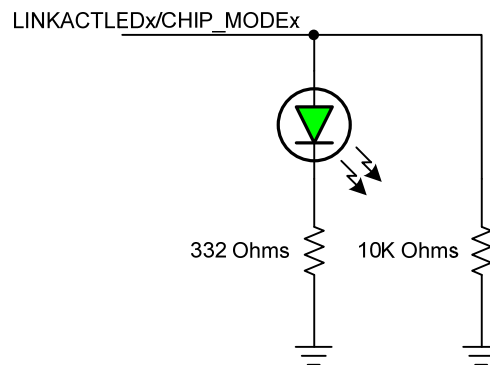
11 = 3 port upstream mode. Ports 2 and 1 are connected to internal PHYs A and B. Port 0 is connected to the external MII pins.

See the latest version of the LAN9252 data sheet for complete details. These pins have weak internal pull-ups and can be driven low with an external 1.0K Ω resistor to digital ground.



CHIP_MODEx Bit = 1

**LED Output Signal from
LAN9252 is Active Low**



CHIP_MODEx Bit = 0

**LED Output Signal from
LAN9252 is Active High**

Miscellaneous:

1. RST# (pin 11), As an input, this active low signal allows external hardware to reset the device. The device also contains an internal power-on reset circuit. Thus this signal may be left unconnected if an external hardware reset is not needed. When used this signal must adhere to the reset timing requirements as detailed in the Section 18.0, "Operational Characteristics," on page 302. As an output, this signal is driven low during POR or in response to an EtherCAT® reset command sequence from the Master Controller or Host interface.
2. REG_EN (pin 7), this pin enables / disables the two +1.2V internal regulators of the LAN9252. Refer to the latest revision of the data sheet for additional information. Connecting this pin to +3.3V will enable the regulators. Connecting this pin to digital ground will disable both regulators. This pin has no internal terminations and must be strapped accordingly.
3. The LAN9252 has an IEEE 1149.1 compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board level testing to ensure system functionality and board manufacturability. For details, see the LAN9252 data sheet.
4. TESTMODE (pin 41) This input pin must be tied to VSS to ensure proper operation.
5. IRQ (pin 44) Interrupt request output. The polarity, source and buffer type of this signal is programmable via the Interrupt Configuration Register (IRQ_CFG). For more information, refer to Section 8.0, "System Interrupts".
6. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.
7. Be sure to incorporate enough bulk capacitors (4.7 - 22 μ F caps) for each power plane.
8. Configuration strap values are typically latched on power-on reset and system reset. Microchip will guarantee that the proper high / low level will be latched in on any device pin with an internal pull-up or pull-down where the device pin is a true no-connect. However, when the configuration strap pin (typically an output pin) is connected to a load, the input leakage current associated with the input load may have an adverse effect on the high / low level ability of the internal pull-up / pull-down. In this case, it is Microchip's recommendation to include an external resistor to augment the internal pull-up / pull-down to ensure the proper high / low level for configuration strap values. Lower VDDIO voltages will further exacerbate this condition



LAN9252 SQFN QuickCheck Pinout Table:

Use the following table to check the LAN9252 SQFN shape in your schematic.

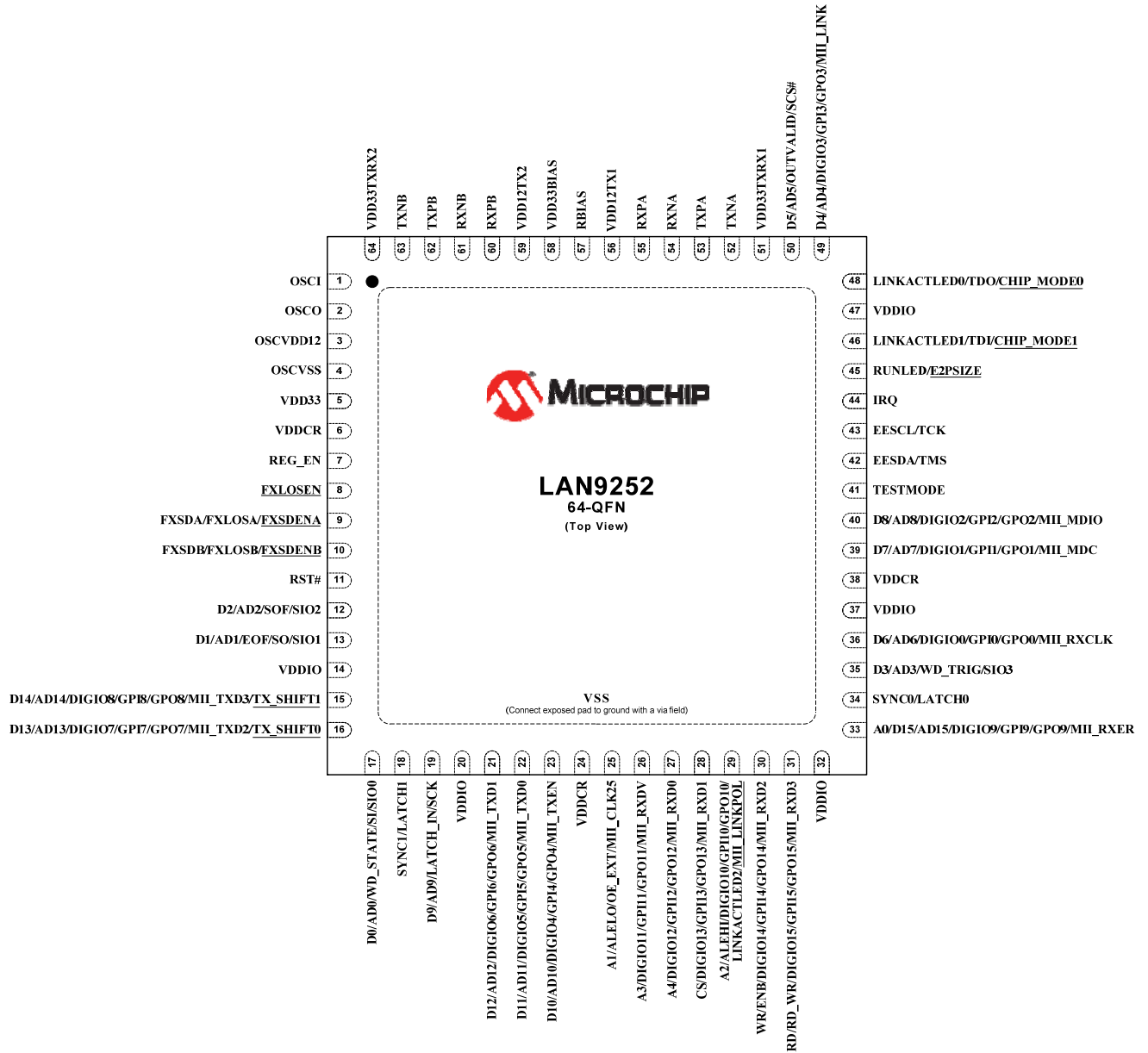
LAN9252 SQFN			
Pin No.	Pin Name	Pin No.	Pin Name
1	OSCI	33	A0 / D15 / AD15 / DIGIO9 / GPI9 / GPO9 / MII_RXER
2	OSCO	34	SYNC0 / LATCH0
3	OSCVDD12	35	D3 / AD3 / WD_TRIG / SIO3
4	OSCVSS	36	D6 / AD6 / DIGIO0 / GPI0 / GPO0 / MII_RXCLK
5	VDD33	37	VDDIO
6	VDDCR	38	VDDCR
7	REG_EN	39	D7 / AD7 / DIGIO1 / GPI1 / GPO1 / MII_MDC
8	<u>FXLOSEN</u>	40	D8 / AD8 / DIGIO2 / GPI2 / GPO2 / MII_MDIO
9	FXSDA / FXLOSA / <u>FXSDENA</u>	41	TESTMODE
10	FXSDB / FXLOSB / <u>FXSDENB</u>	42	EESDA / TMS
11	RST#	43	EESCL / TCK
12	D2 / AD2 / SOF / SIO2	44	IRQ
13	D1 / AD1 / EOF / SO / SIO1	45	RUNLED / <u>E2PSIZE</u>
14	VDDIO	46	LINKACTLED1 / TDI / <u>CHIP_MODE1</u>
15	D14 / AD14 / DIGIO8 / GPI8 / GPO8 / MII_TXD3 / <u>TX_SHIFT1</u>	47	VDDIO
16	D13 / AD13 / DIGIO7 / GPI7 / GPO7 / MII_TXD2 / <u>TX_SHIFT0</u>	48	LINKACTLED0 / TDO / <u>CHIP_MODE0</u>
17	D0 / AD0 / WD_STATE / SI / SIO0	49	D4 / AD4 / DIGIO3 / GPI3 / GPO3 / MII_LINK
18	SYNC1 / LATCH1	50	D5 / AD5 / OUTVALID / SCS#
19	D9 / AD9 / LATCH_IN / SCK	51	VDD33TXRX1
20	VDDIO	52	TXNA
21	D12 / AD12 / DIGIO6 / GPI6 / GPO6 / MII_TXD1	53	TXPA
22	D11 / AD11 / DIGIO5 / GPI5 / GPO5 / MII_TXD0	54	RXNA
23	D10 / AD10 / DIGIO4 / GPI4 / GPO4 / MII_TXEN	55	RXPA
24	VDDCR	56	VDD12TX1
25	A1 / ALELO / OE_EXT / MII_CLK25	57	RBIAS
26	A3 / DIGIO11 / GPI11 / GPO11 / MII_RXDV	58	VDD33BIAS
27	A4 / DIGIO12 / GPI12 / GPO12 / MII_RXD0	59	VDD12TX2
28	CS / DIGIO13 / GPI13 / GPO13 / MII_RXD1	60	RXPB
29	A2 / ALEHI / DIGIO10 / GPI10 / GPO10 / LINKACTLED2 / <u>MIILINKPOL</u>	61	RXNB
30	WR / ENB / DIGIO14 / GPI14 / GPO14 / MII_RXD2	62	TXPB
31	RD / RD_WR / DIGIO15 / GPI15 / GPO15 / MII_RXD3	63	TXNB
32	VDDIO	64	VDD33TXRX2
65		EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package	



Notes:



LAN9252 SQFN Package Drawing:



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

Reference Material:

1. Microchip LAN9252 Data Sheet; check web site for latest revision.
2. Microchip LAN9252 Reference Design, check web site for latest revision.
3. Microchip Reference Designs are schematics only; there are no associated PCBs.
4. EVB-LAN9252-HBI Customer Evaluation Board & Schematics
5. EVB-LAN9252-DIGIO Customer Evaluation Board & Schematics

