High-Density BGA Routing Guidelines for Microchip MPUs

AN5871

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Scope

This document is intended to facilitate designing with Microchip MPUs packaged in a high-density BGA (Ball Grid Array) package. Routing guidelines and recommendations are provided for each Microchip MPU currently available in a high-density BGA package:

- SAM9X60
- SAM9X7 Series
- SAMA7G54

Introduction

All the guidelines presented in this document are based on real working PCBs not publicly available, and are meant to serve as recommendations rather than mandatory design rules. The example routings are prone to be further densified if the PCB technology permits it while preserving the trace impedances and length matching.

Reference Documents

The following Microchip documents are available and recommended as complementary reference resources.

Table 1. Reference Documents

Type	Title	Literature Number	Available
Application note	SAM9X60 Hardware Design Considerations	DS00003311	www.microchip.com
Application note	SAM9X75 Hardware Design Considerations	DS00004962	www.microchip.com
Application note	SAMA7G54 Hardware Design Considerations	DS00004598	www.microchip.com

1. Document Layout

The document is organized as follows:

- Introduction
- SAM9X60: design recommendations for the SAM9X60 MPU
- SAM9X7 Series: design recommendations for the SAM9X75, SAM9X72 and SAM9X70 MPUs
- SAMA7G54: design recommendations for the SAMA7G54 MPU

2. SAM9X60

The SAM9X60-V/6GW MPU is available in a 256-ball Thin Fine-Pitch Ball Grid Array (TFBGA) package with a 9x9 mm body size and a 0.5 mm ball pitch.

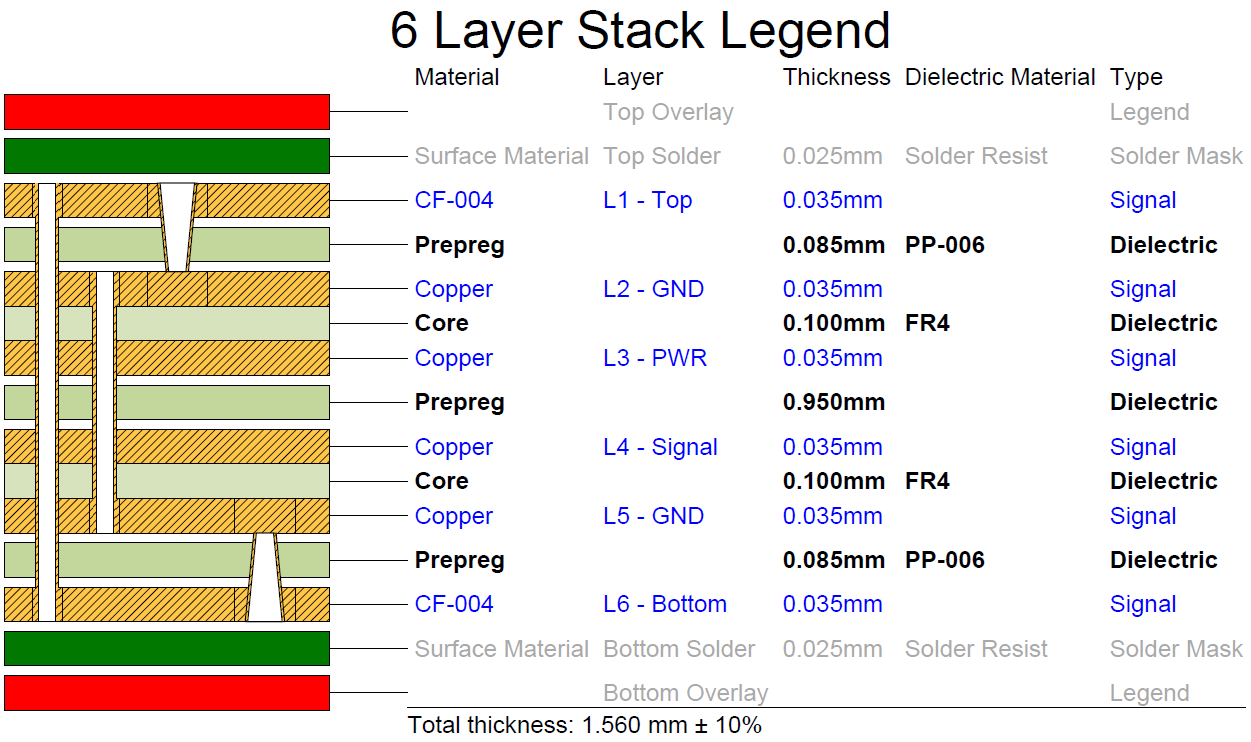
2.1 PCB Stack-Up

A minimum of six layers is required to ensure proper connectivity for signals and power. The following figure shows an example of a 6-layer stack-up.

Each layer can be assigned as follows:

- Layer 1 (Top) – Signal
- Layer 2 (Inner) – Ground
- Layer 3 (Inner) – Power
- Layer 4 (Inner) – Signal
- Layer 5 (Inner) – Ground
- Layer 6 (Bottom) – Signal

Figure 2-1. SAM9X60 6-Layer PCB Stack-Up Example



2.2 HDI PCB Rules

The high-density BGA package featured by SAM9X60 requires HDI (High-Density Interconnect) PCB features such as blind and buried vias, and small trace width and clearance. It also requires the via-in-pad feature.

The following design rules are recommended for the PCB area below and near the MPU package:

- Blind and buried vias: 0.25 mm diameter and 0.125 mm hole size
- BGA land size: 0.25 mm diameter with 0.05 mm solder mask expansion
- Trace width/clearance: 0.075/0.087 mm

Further away from the MPU package (clearance larger than 5 to 10 mm), more relaxed rules can be adopted, such as:

- Through hole vias: 0.4 mm diameter and 0.2 mm hole size
- Trace width/clearance: 0.1/0.1 mm

2.3 Escape Pattern

The figures below illustrate various escape pattern designs.

Figure 2-2. SAM9X60 Top Layer Example - Signal

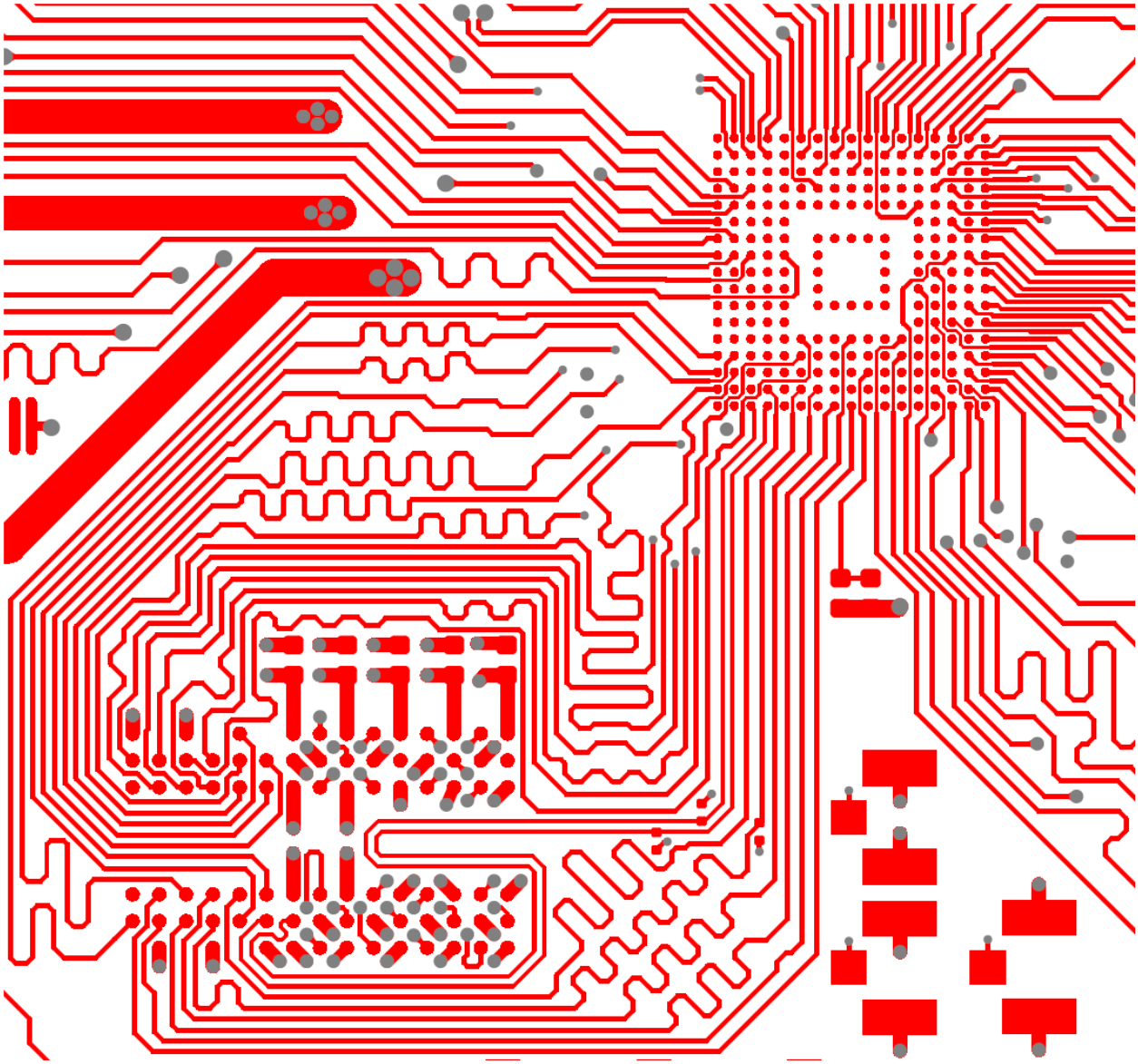


Figure 2-3. SAM9X60 Layer 2 Example - Ground

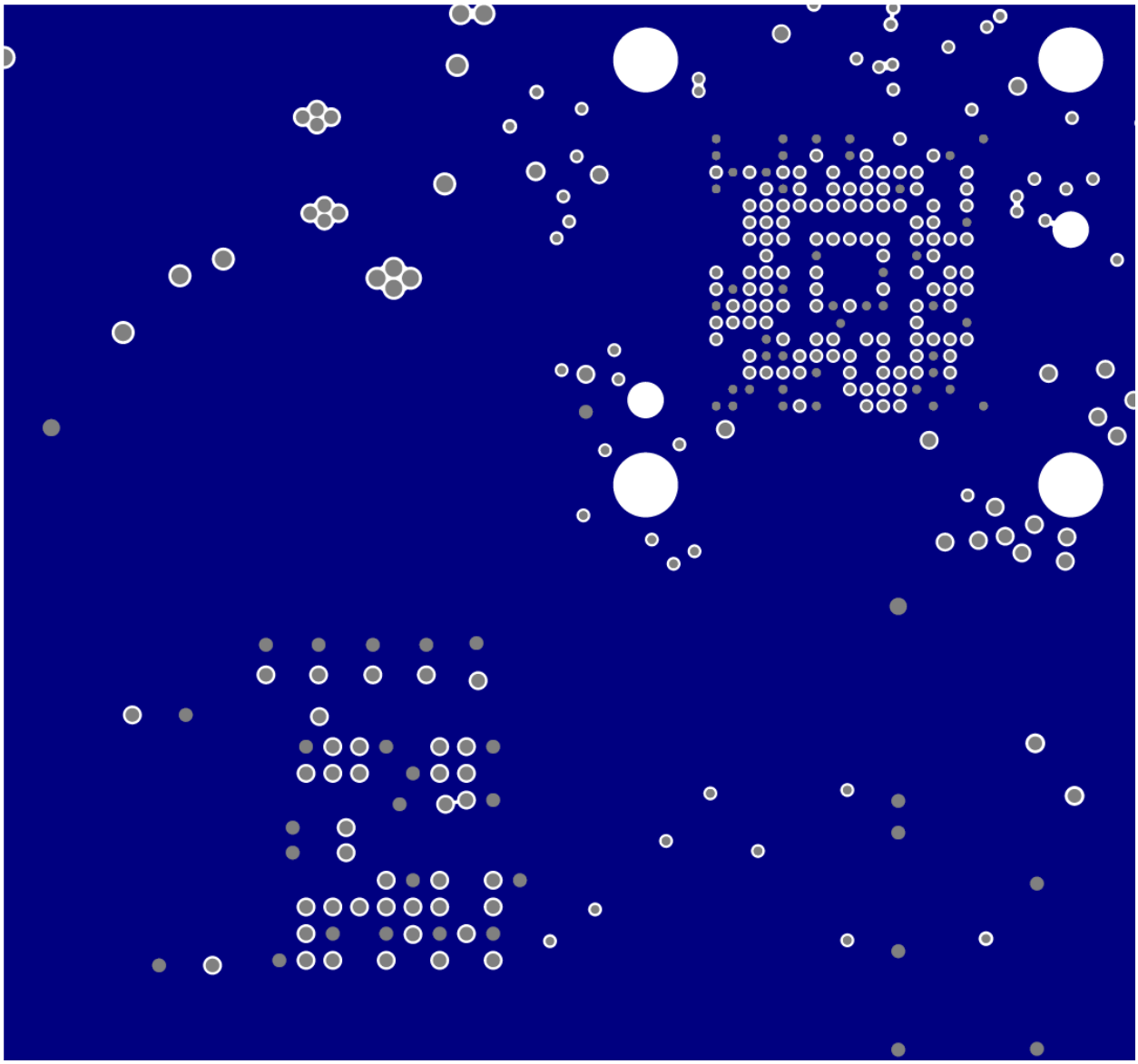


Figure 2-4. SAM9X60 Layer 3 Example - Power

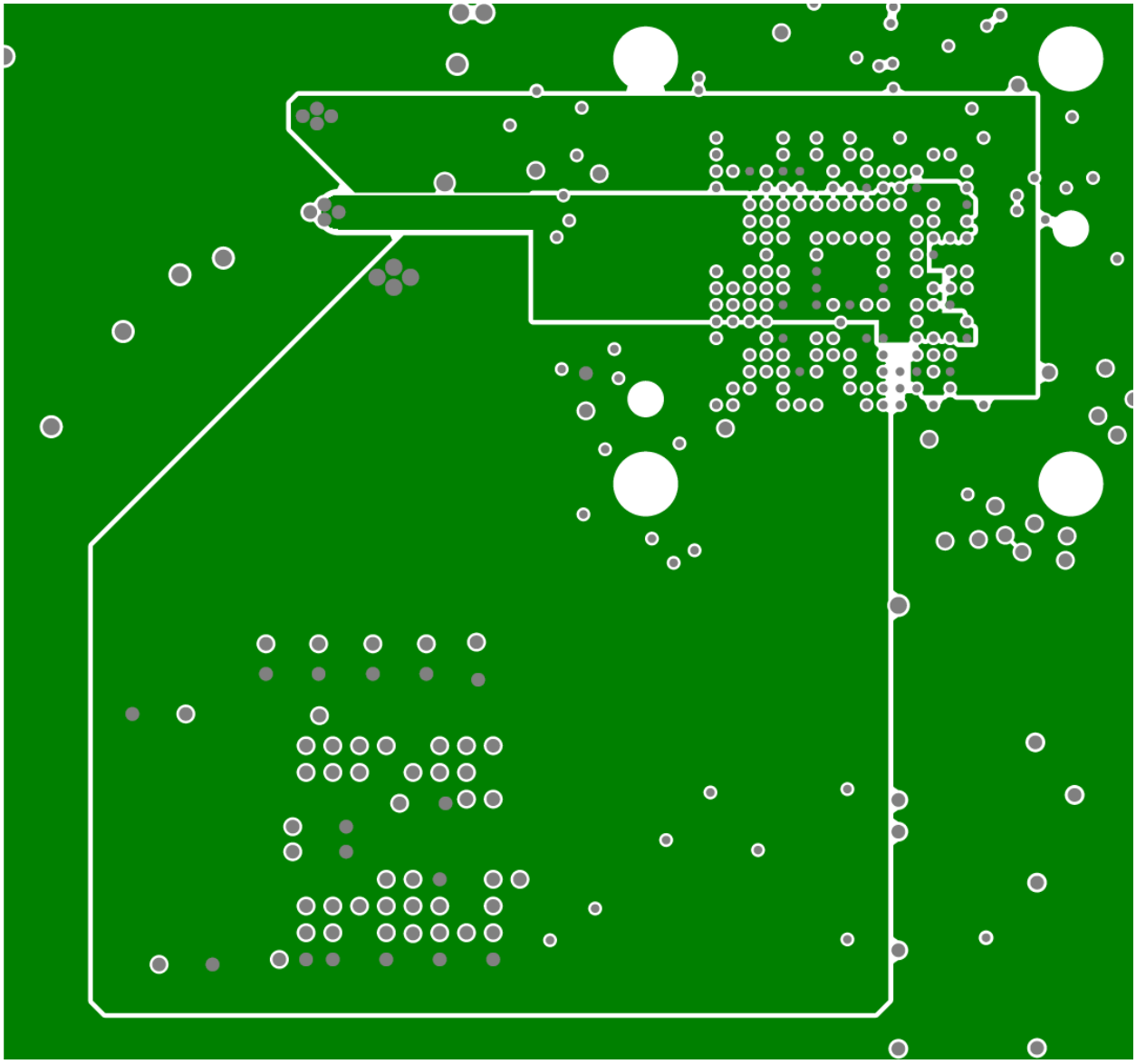


Figure 2-5. SAM9X60 Layer 4 Example - Signal

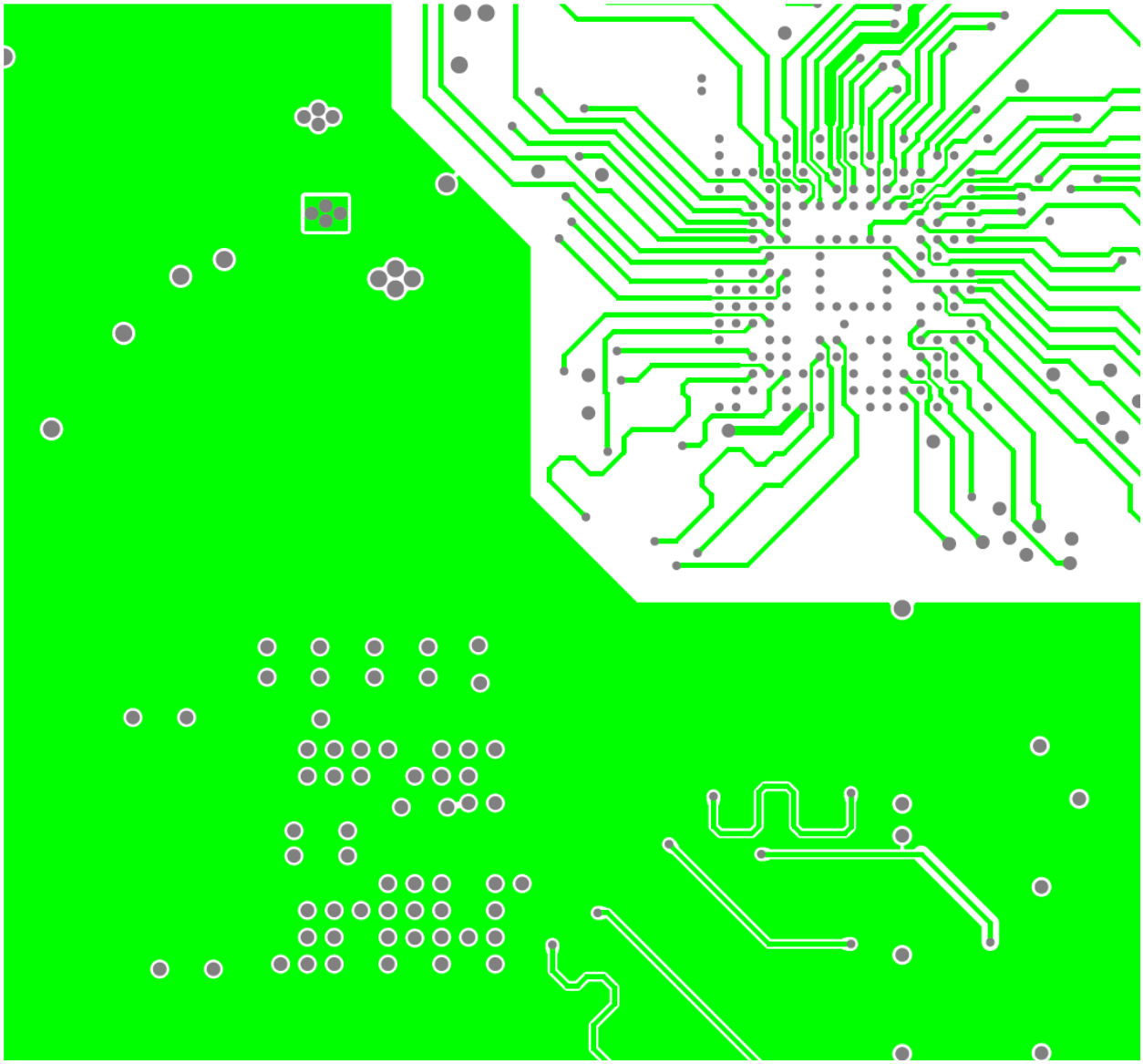


Figure 2-6. SAM9X60 Layer 5 Example - Ground

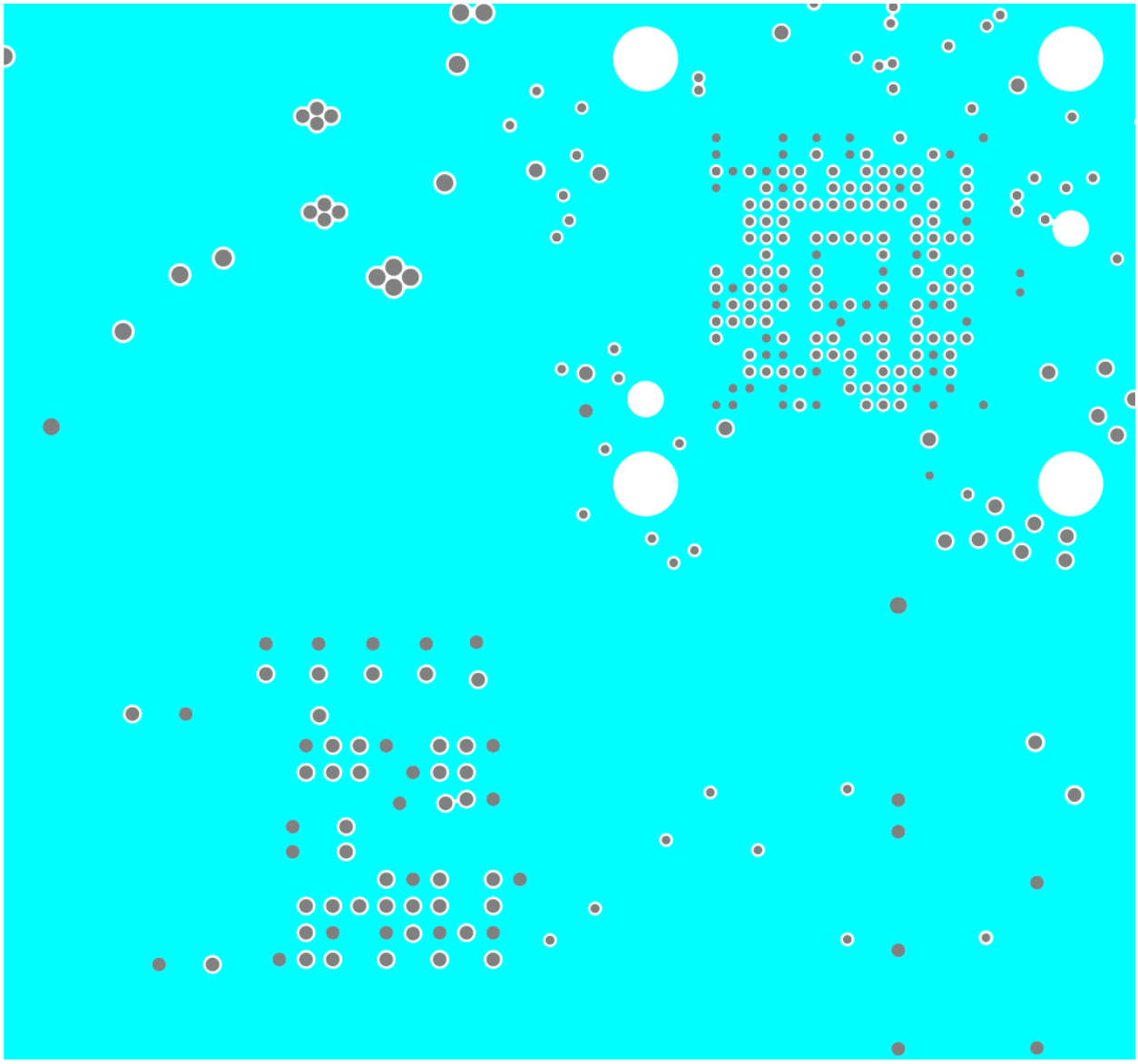
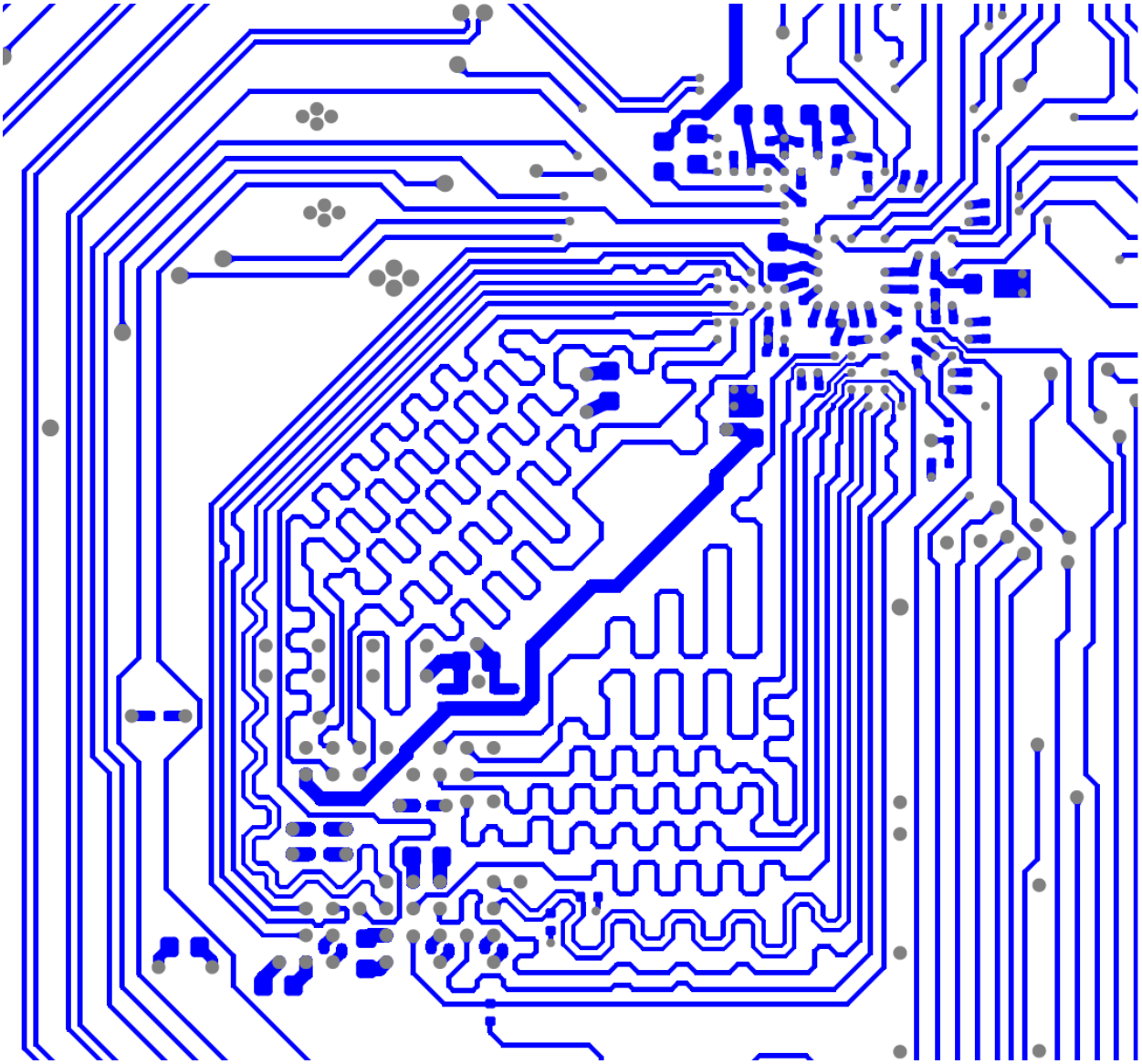
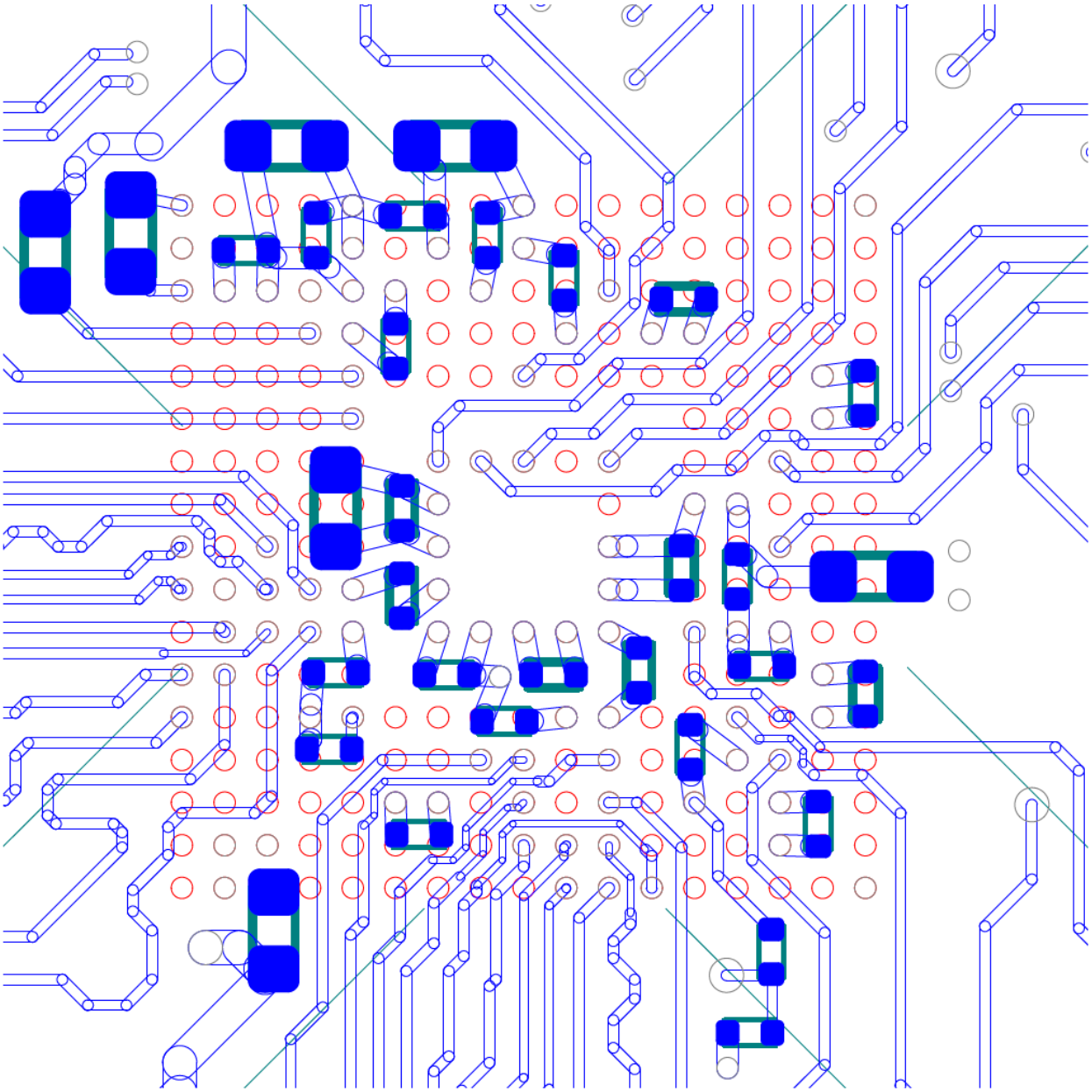


Figure 2-7. SAM9X60 Bottom Layer Example - Signal



The decoupling capacitors should be placed on the bottom, as close as possible to the vias connecting the power pins of the MPU. An example of such placement can be seen in the following figure.

Figure 2-8. SAM9X60 Decoupling Capacitors Placement Example



3. SAM9X7 Series

The SAM9X75-V/6GW, SAM9X72-V/6GW and SAM9X70-V/6GW MPUs are available in a 256-ball Thin Fine-Pitch Ball Grid Array (TFBGA) package with a 9x9 mm body size and a 0.5 mm ball pitch.

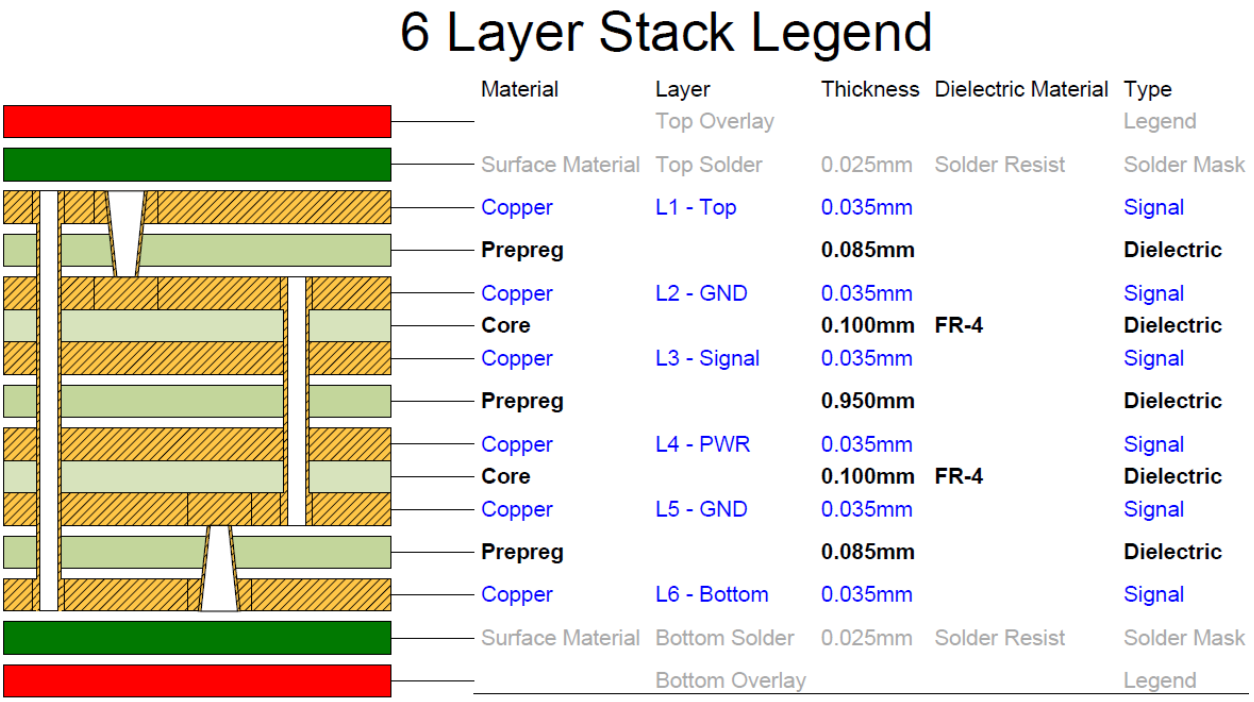
3.1 PCB Stack-Up

A minimum of six layers is required to ensure proper connectivity for signals and power. The following figure shows an example of a 6-layer stack-up.

Each layer can be assigned as follows:

- Layer 1 (Top) – Signal
- Layer 2 (Inner) – Ground
- Layer 3 (Inner) – Signal
- Layer 4 (Inner) – Power
- Layer 5 (Inner) – Ground
- Layer 6 (Bottom) – Signal

Figure 3-1. SAM9X7 Series 6-Layer PCB Stack-Up Example



3.2 HDI PCB Rules

The high-density BGA package featured by the SAM9X7 Series MPUs requires HDI (High-Density Interconnect) PCB features such as blind and buried vias, and small trace width and clearance. It also requires the via-in-pad feature.

The following design rules are recommended for the PCB area below and near the MPU package:

- Blind and buried vias: 0.25 mm diameter and 0.125 mm hole size
- BGA land size: 0.25 mm diameter with 0.05 mm solder mask expansion
- Trace width/clearance: 0.075/0.087 mm

Further away from the MPU package (clearance larger than 5 to 10 mm), more relaxed rules can be adopted, such as:

- Through hole vias: 0.4 mm diameter and 0.2 mm hole size
- Trace width/clearance: 0.1/0.1 mm

3.3 Escape Pattern

The figures below illustrate various escape pattern designs.

Figure 3-2. SAM9X7 Series Top Layer Example - Signal

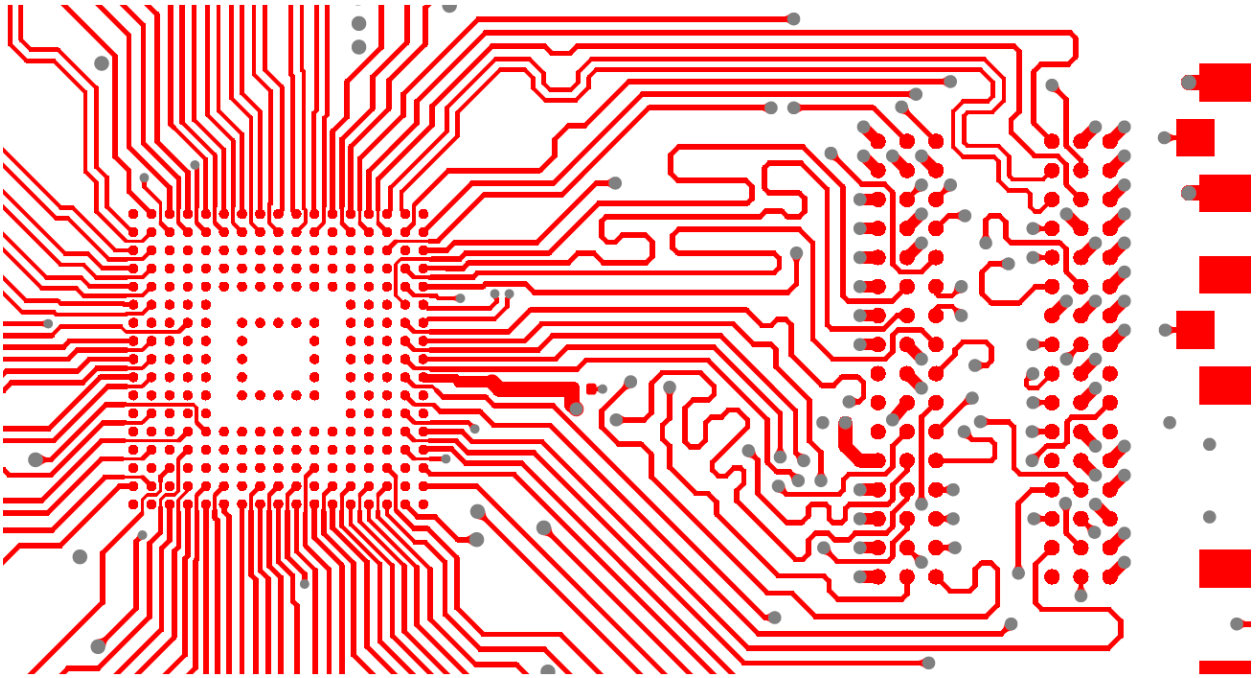


Figure 3-3. SAM9X7 Series Layer 2 Example - Ground

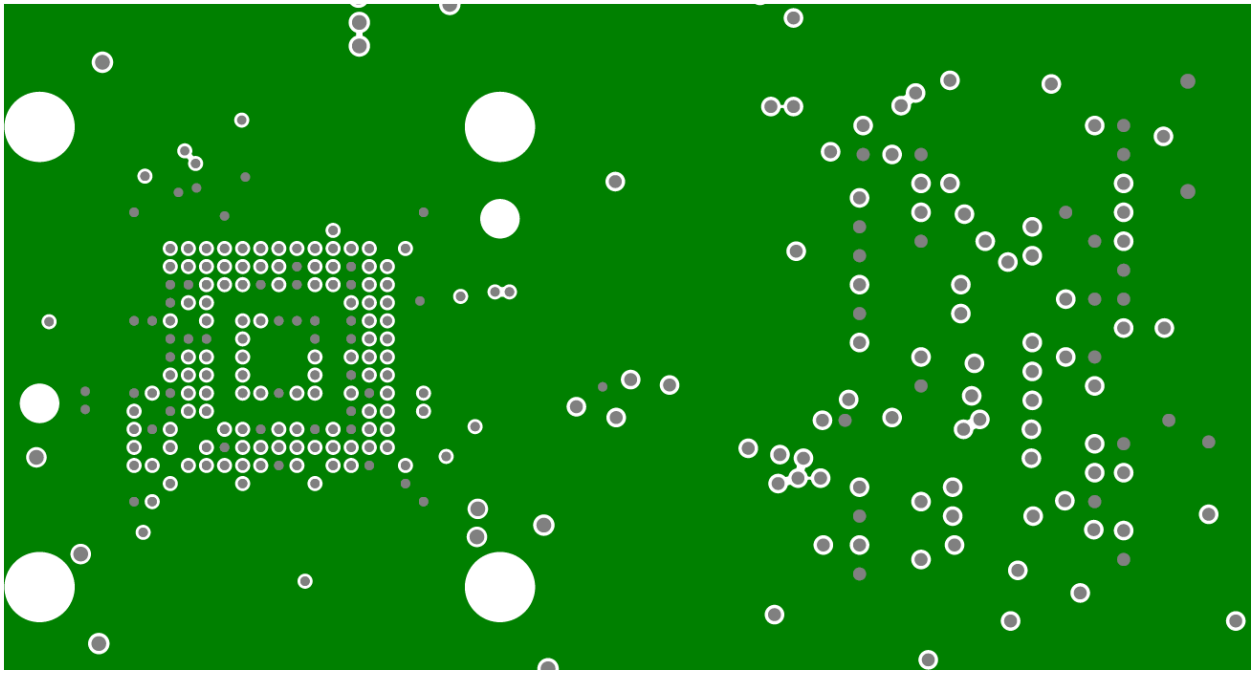


Figure 3-4. SAM9X7 Series Layer 3 Example - Signal

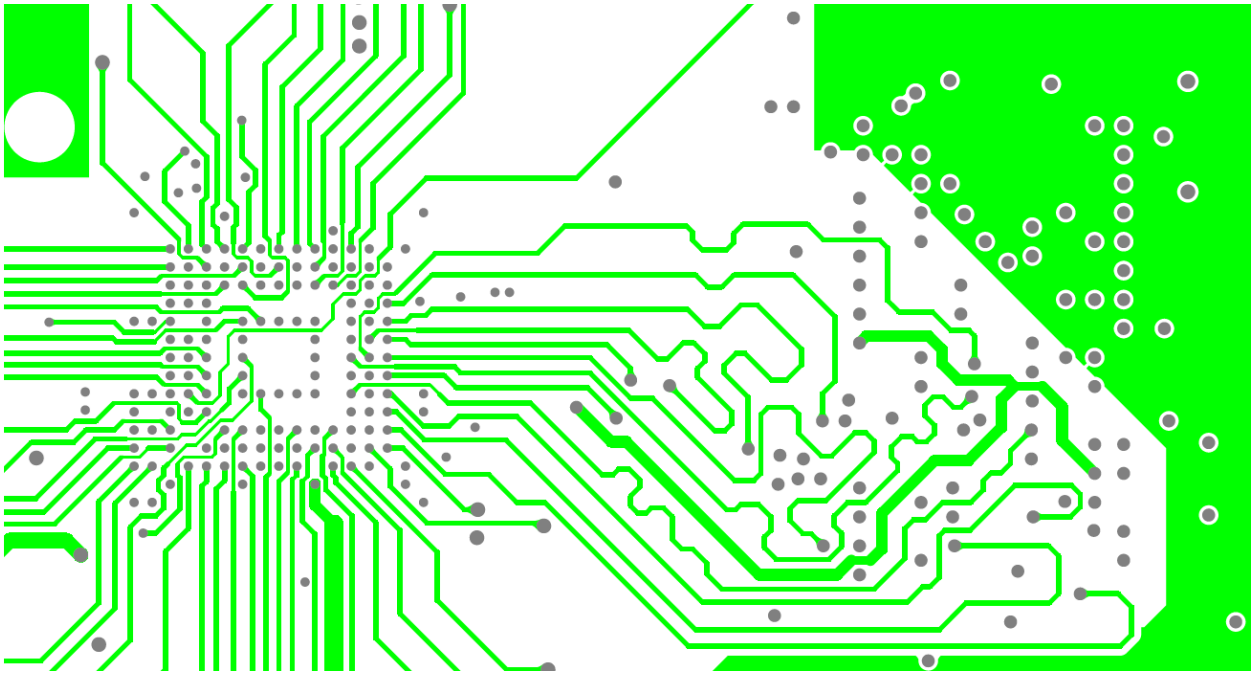


Figure 3-5. SAM9X7 Series Layer 4 Example - Power

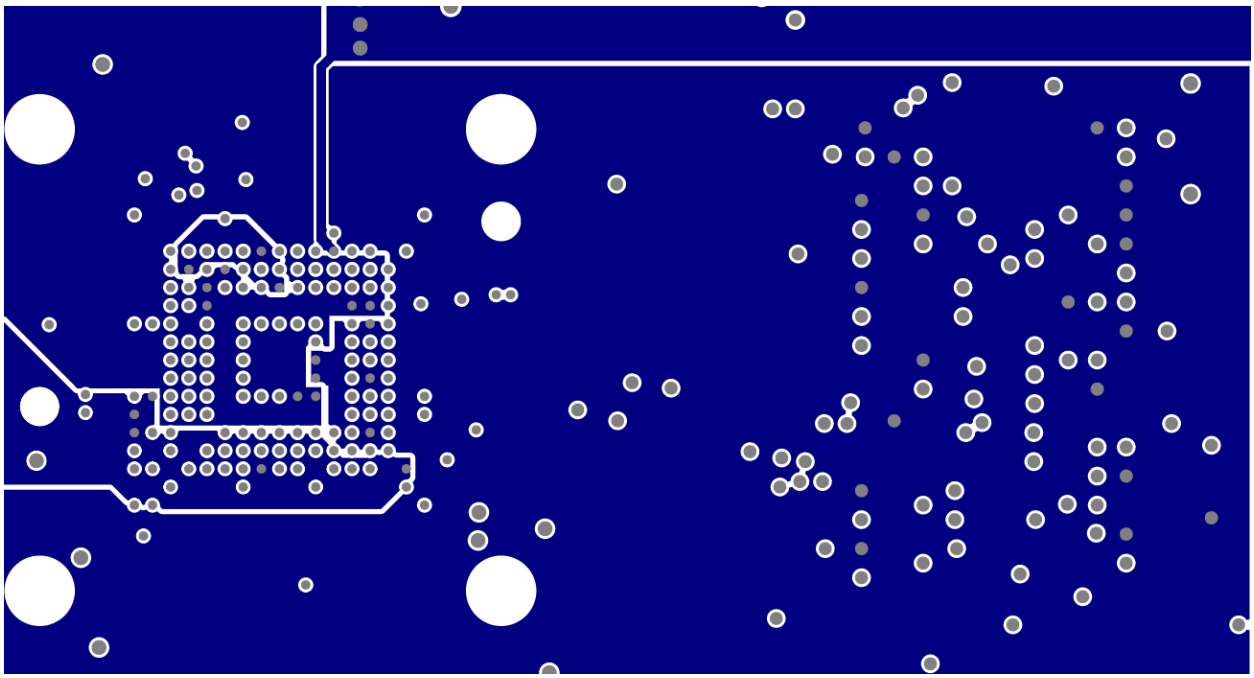


Figure 3-6. SAM9X7 Series Layer 5 Example - Ground

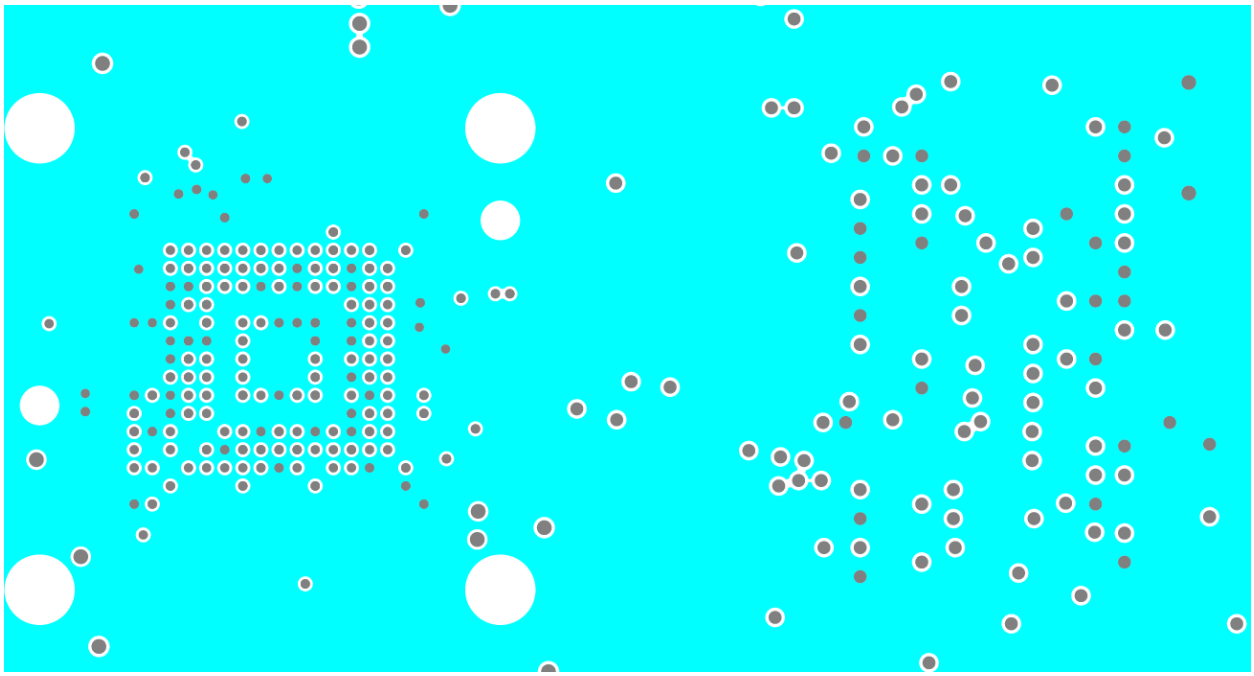
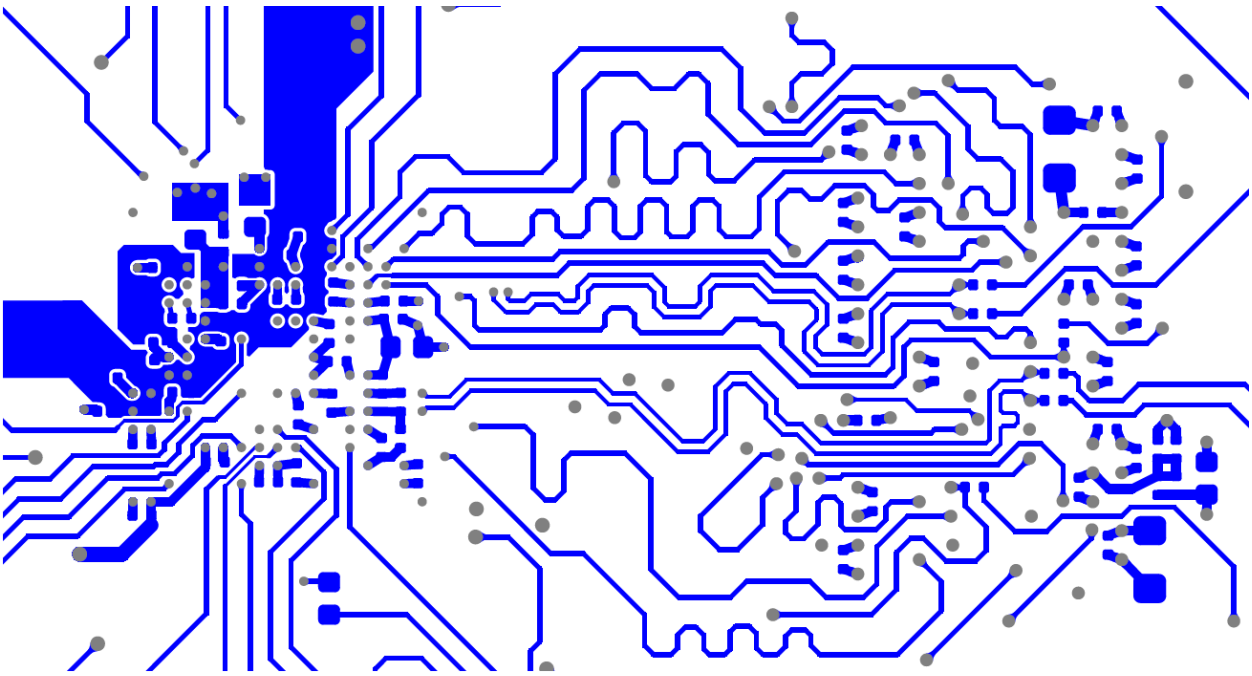
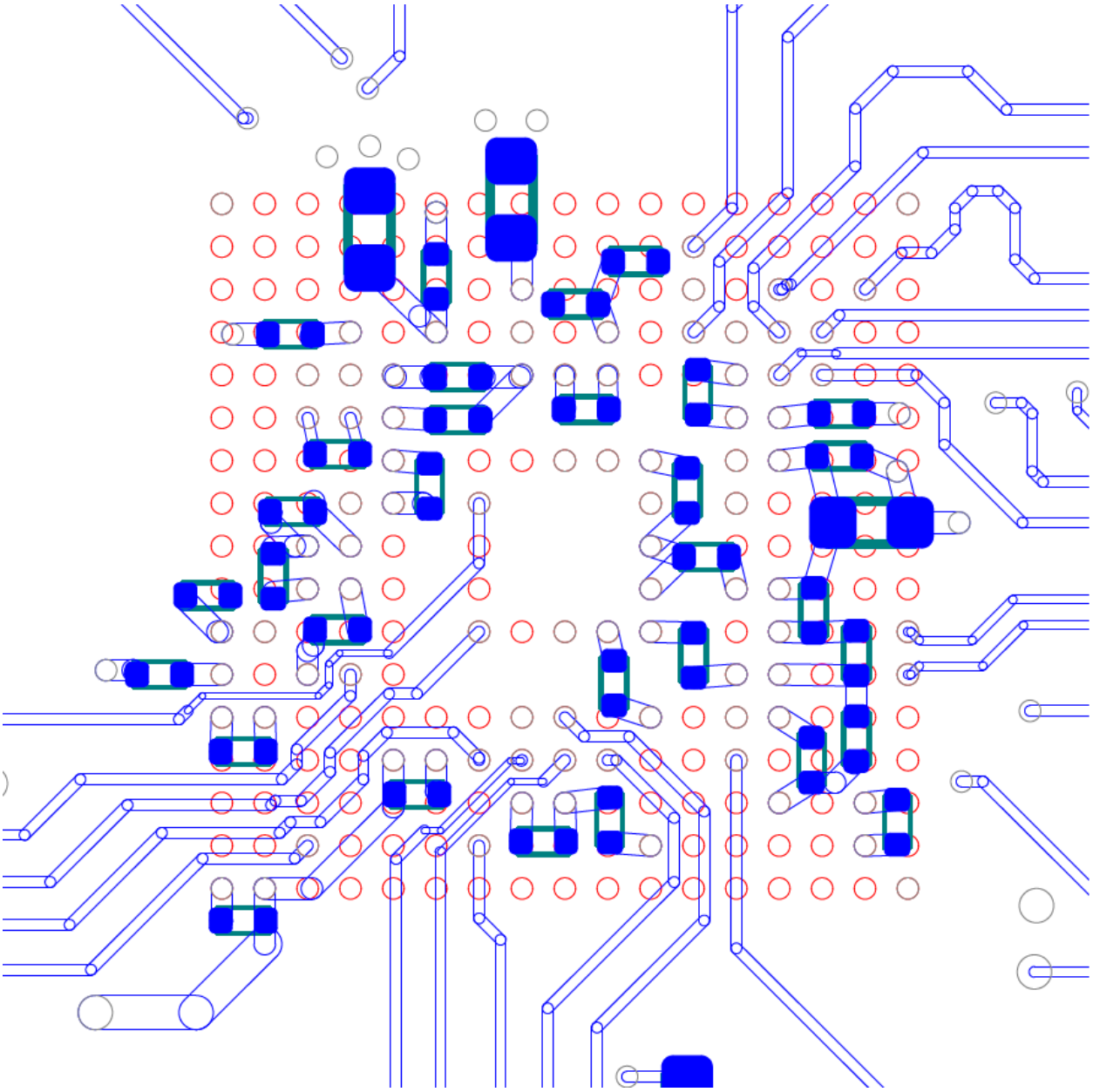


Figure 3-7. SAM9X7 Series Bottom Layer Example - Signal



The decoupling capacitors should be placed on the bottom, as close as possible to the vias connecting the power pins of the MPU. An example of such placement can be seen in the following figure.

Figure 3-8. SAM9X7 Series Decoupling Capacitors Placement Example



4. SAMA7G54

The SAMA7G54-V/7EW MPU is available in a 375-ball Thin Fine-Pitch Ball Grid Array (TFBGA) package with a 9x9 mm body size and a 0.4 mm ball pitch.

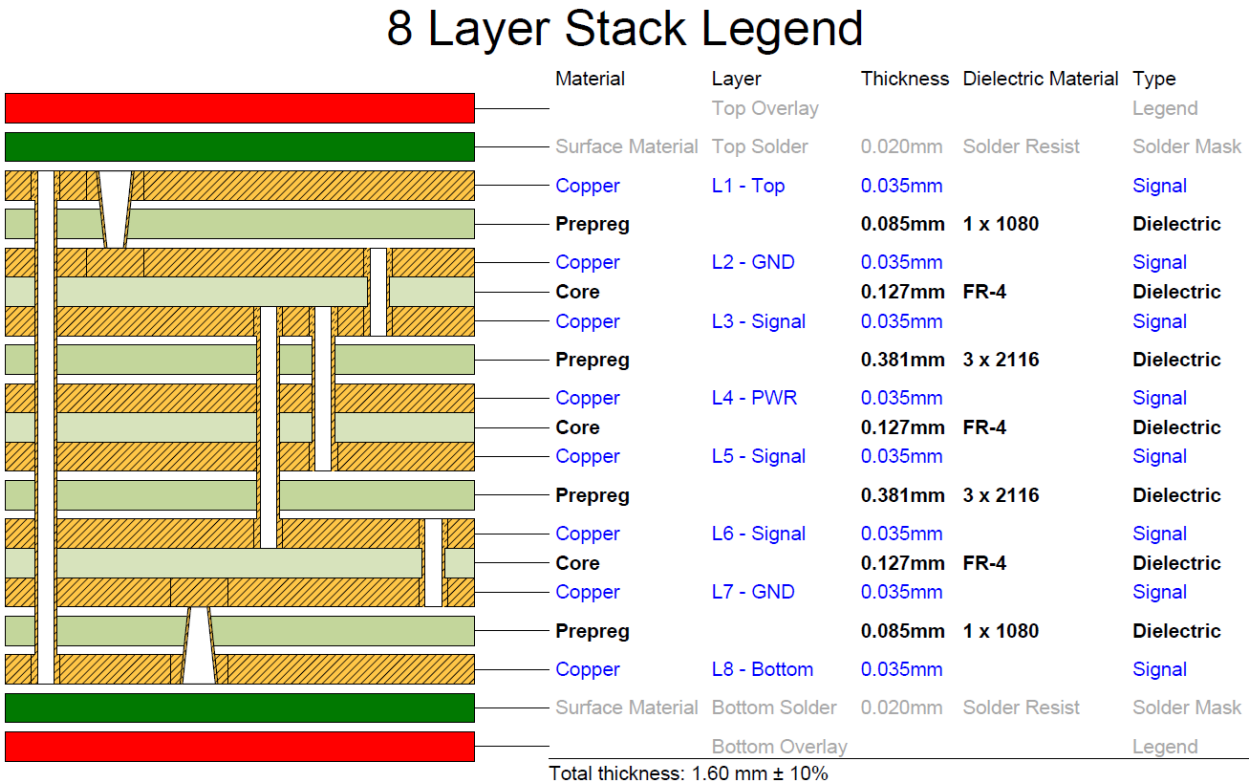
4.1 PCB Stack-Up

A minimum of eight layers is required to ensure proper connectivity for signals and power. The following figure shows an example of an 8-layer stack-up.

Each layer can be assigned as follows:

- Layer 1 (Top) – Signal
- Layer 2 (Inner) – Ground
- Layer 3 (Inner) – Signal
- Layer 4 (Inner) – Power
- Layer 5 (Inner) – Signal
- Layer 6 (Inner) – Signal
- Layer 7 (Inner) – Ground
- Layer 8 (Bottom) – Signal

Figure 4-1. SAMA7G54 8-Layer PCB Stack-Up Example



4.2 HDI PCB Rules

The high-density BGA package featured by SAMA7G54 requires HDI (High-Density Interconnect) PCB features such as blind and buried vias, and small trace width and clearance. It also requires the via-in-pad feature.

The following design rules are recommended for the PCB area below and near the MPU package:

- Blind and buried vias: 0.25 mm diameter and 0.1 mm hole size
- BGA land size: 0.25 mm diameter with 0.04 mm solder mask expansion
- Trace width/clearance: 0.01/0.087 mm

Further away from the MPU package (clearance larger than 5 to 10 mm), more relaxed rules can be adopted, such as:

- Through hole vias: 0.4 mm diameter and 0.2 mm hole size
- Trace width/clearance: 0.1/0.1 mm

4.3 Escape Pattern

The figures below illustrate various escape pattern designs.

Figure 4-2. SAMA7G54 Top Layer Example - Signal

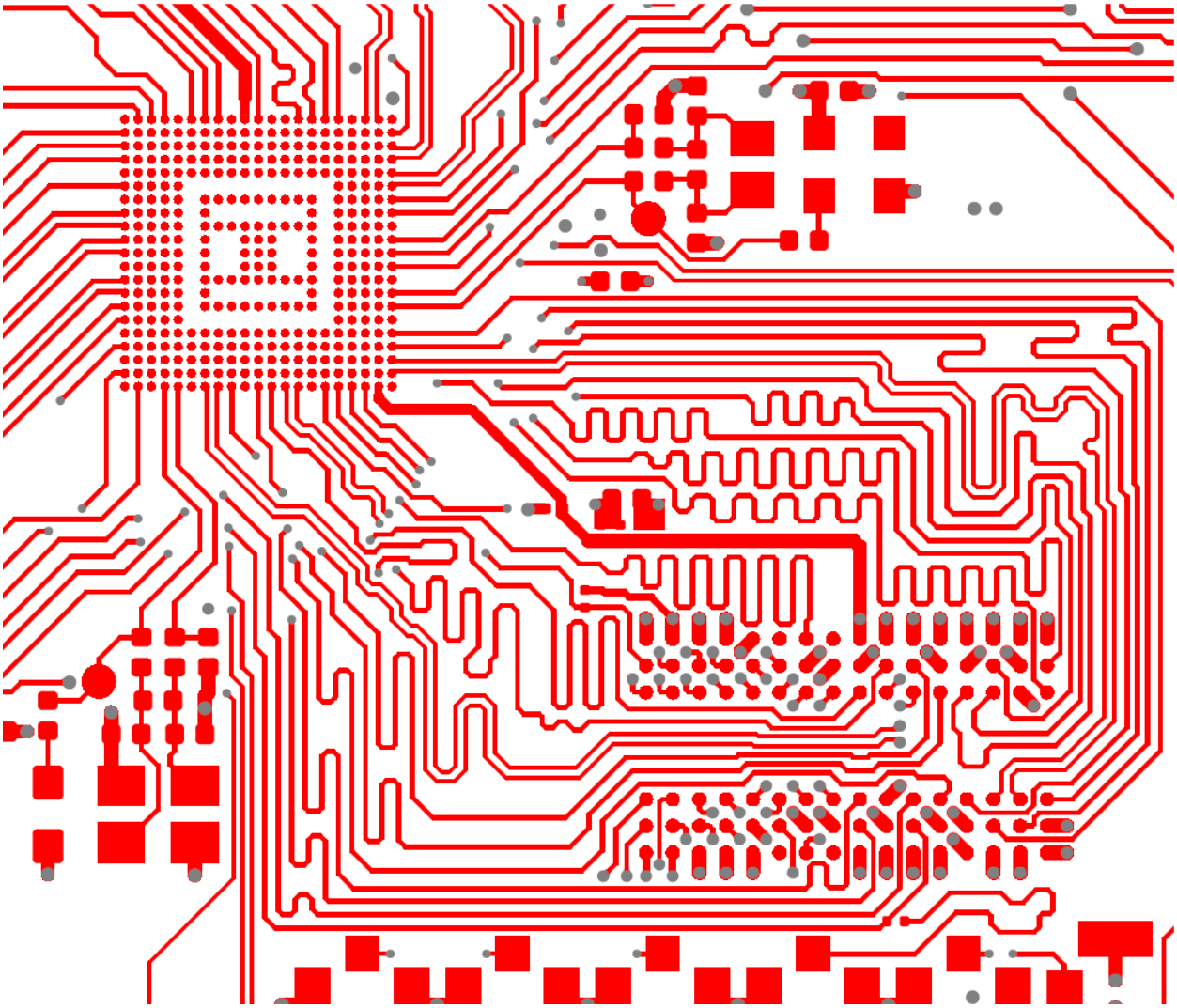


Figure 4-3. SAMA7G54 Layer 2 Example - Ground

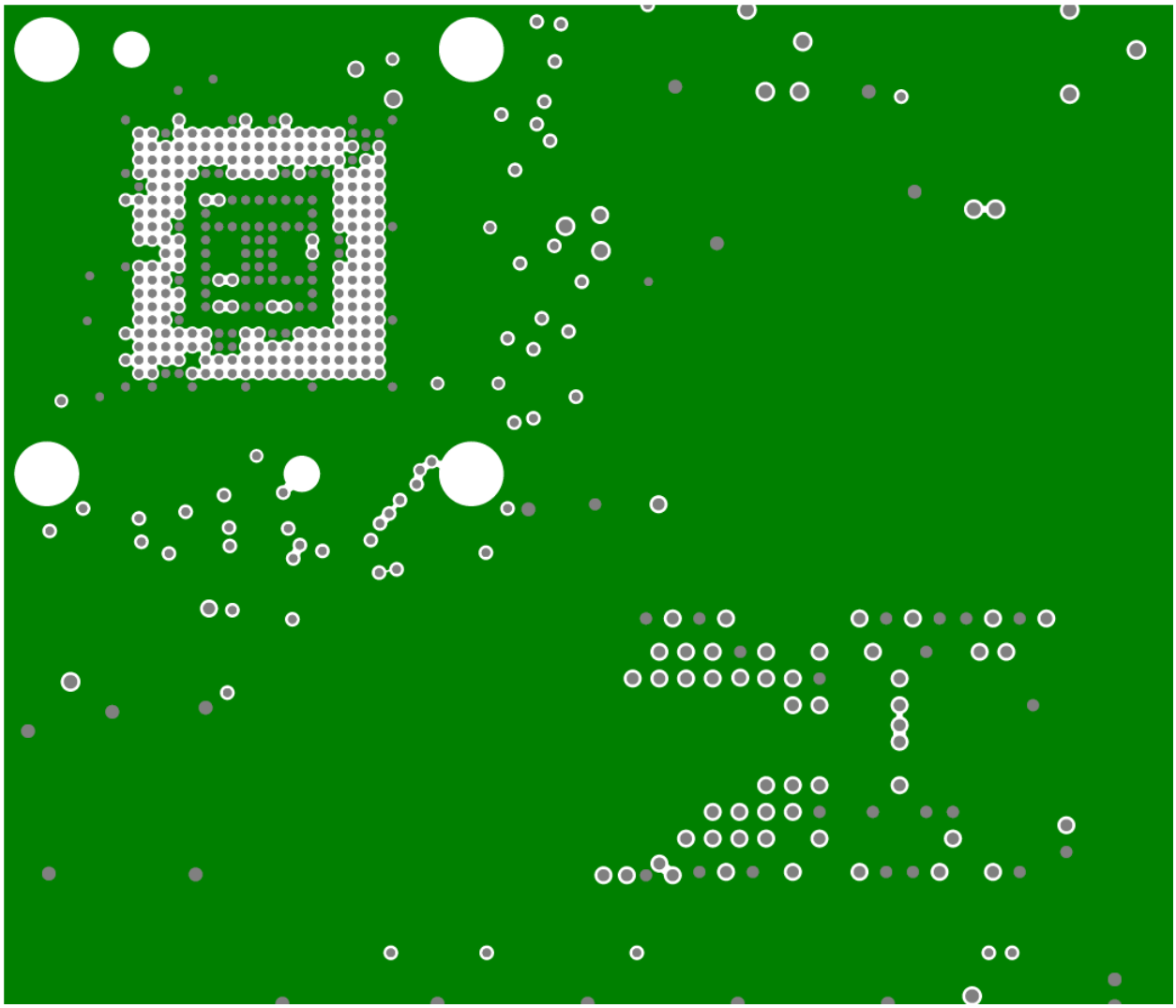


Figure 4-4. SAMA7G54 Layer 3 Example - Signal

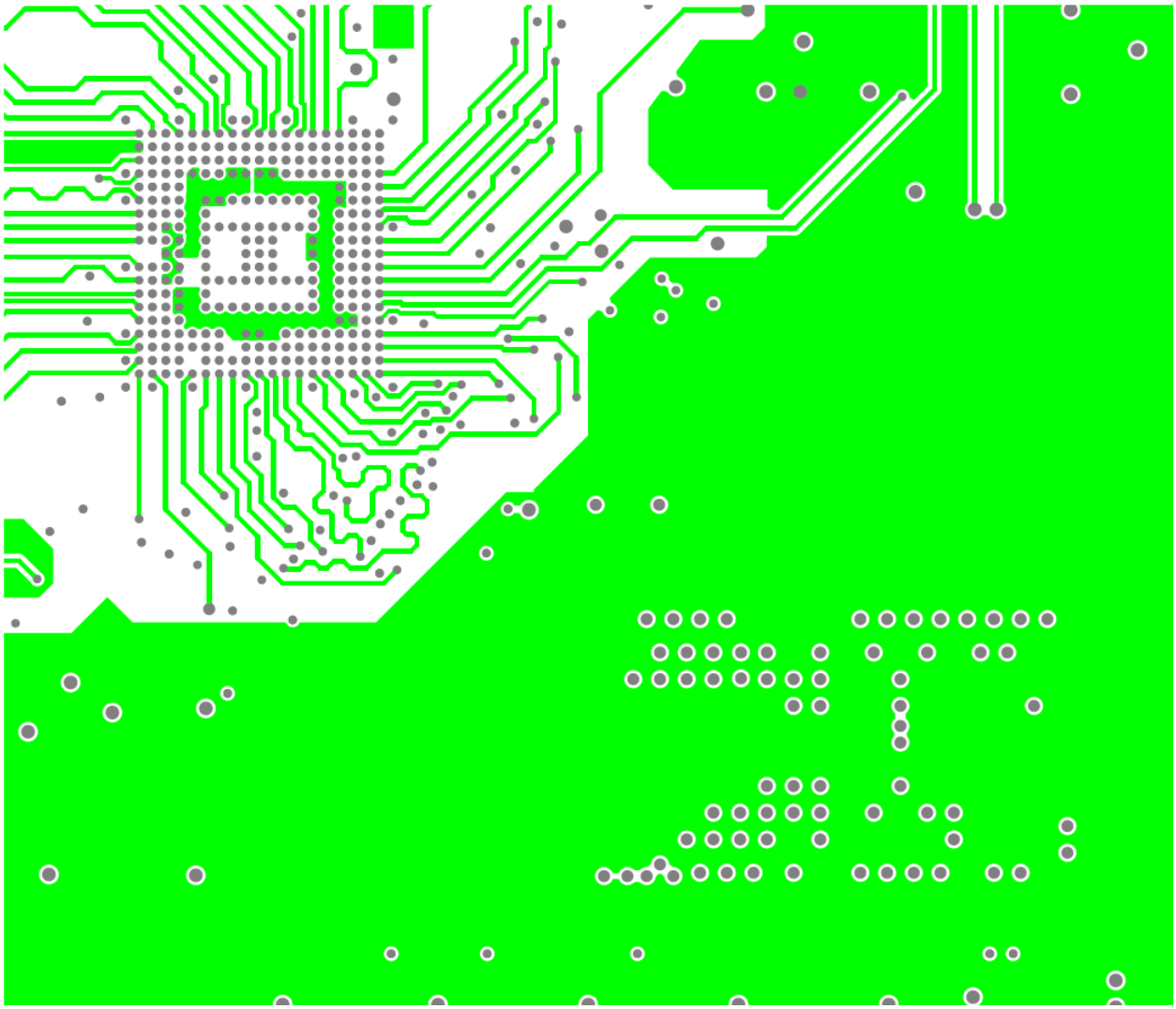


Figure 4-5. SAMA7G54 Layer 4 Example - Power

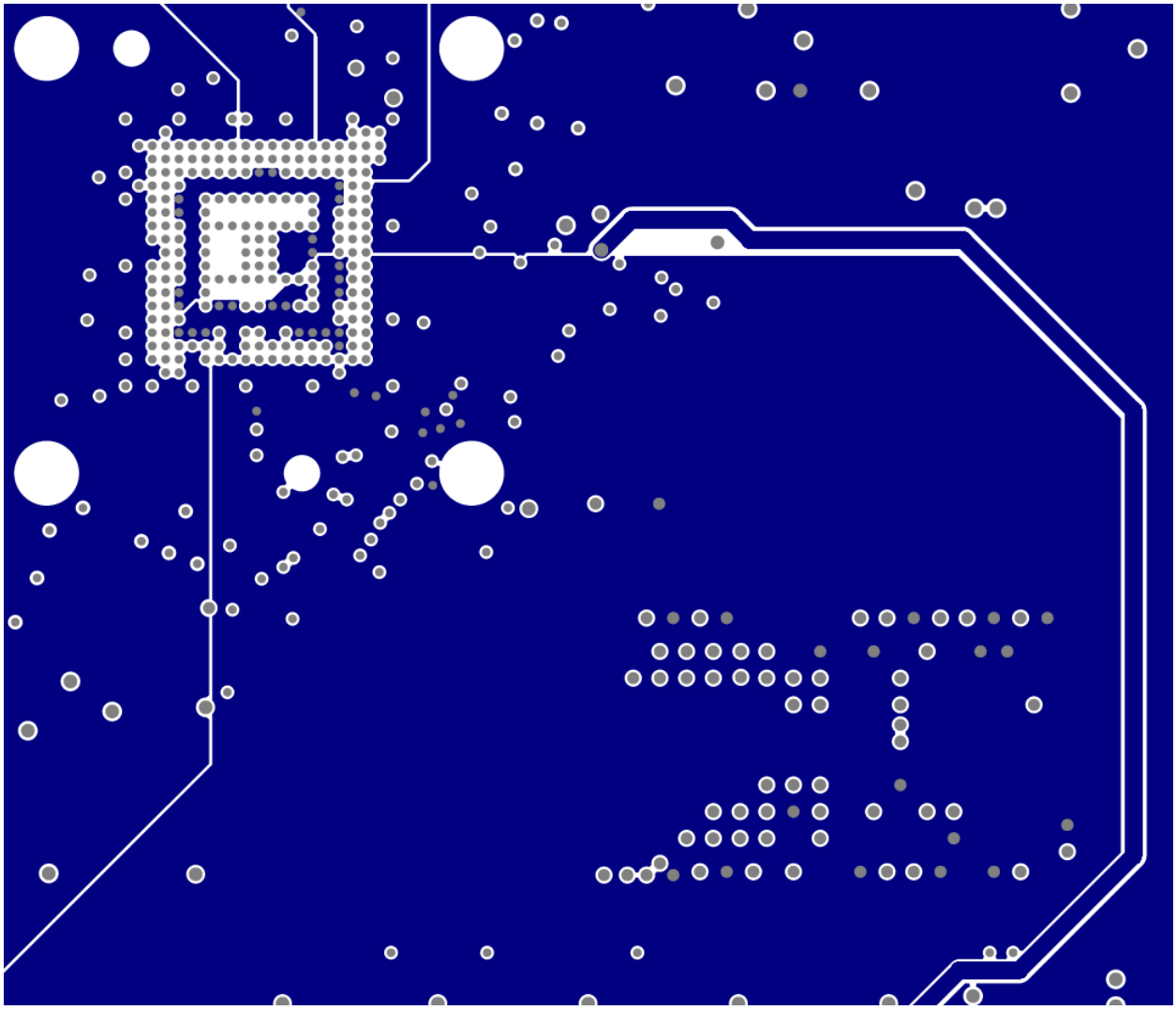


Figure 4-6. SAMA7G54 Layer 5 Example - Signal

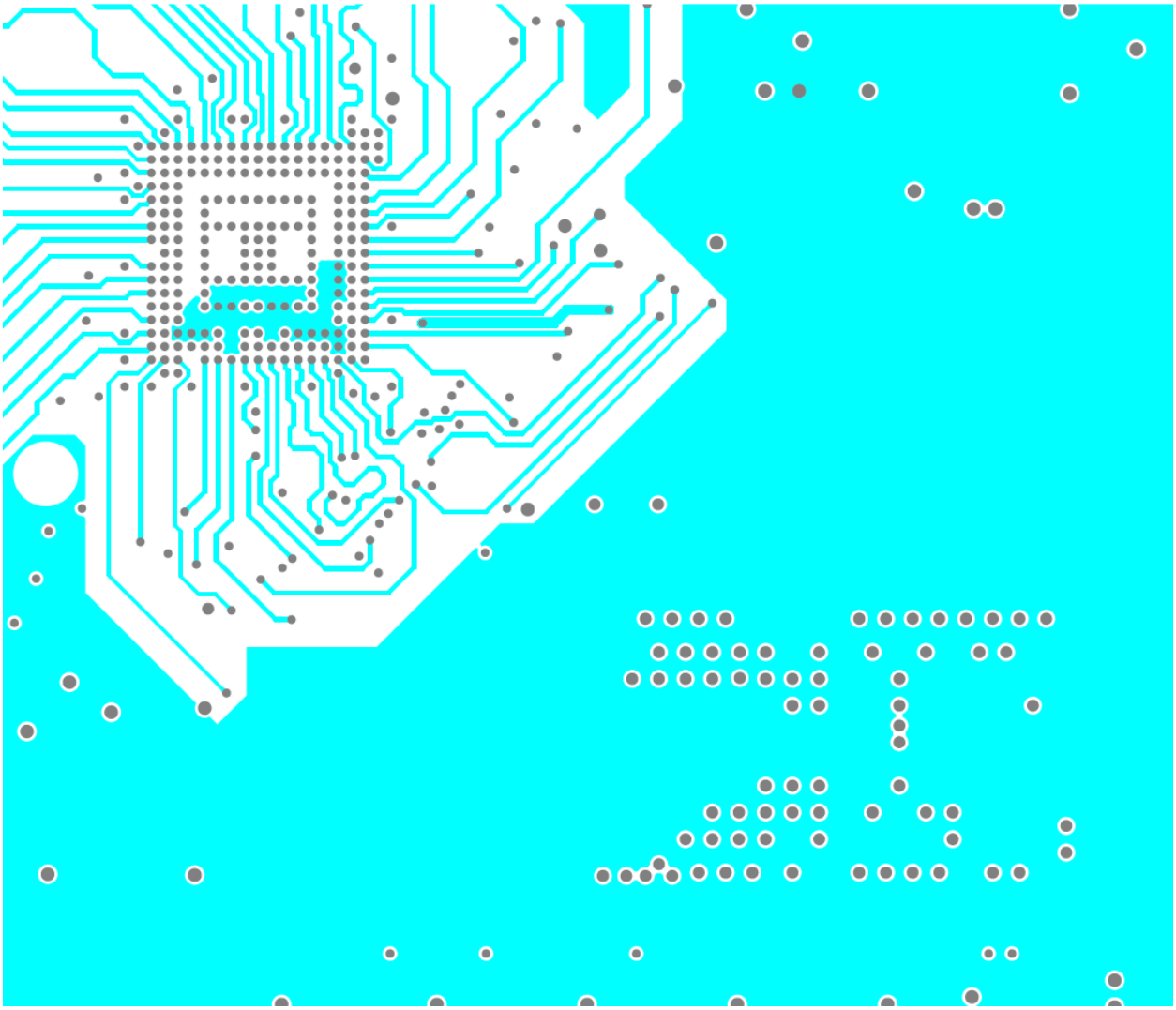


Figure 4-7. SAMA7G54 Layer 6 Example - Signal

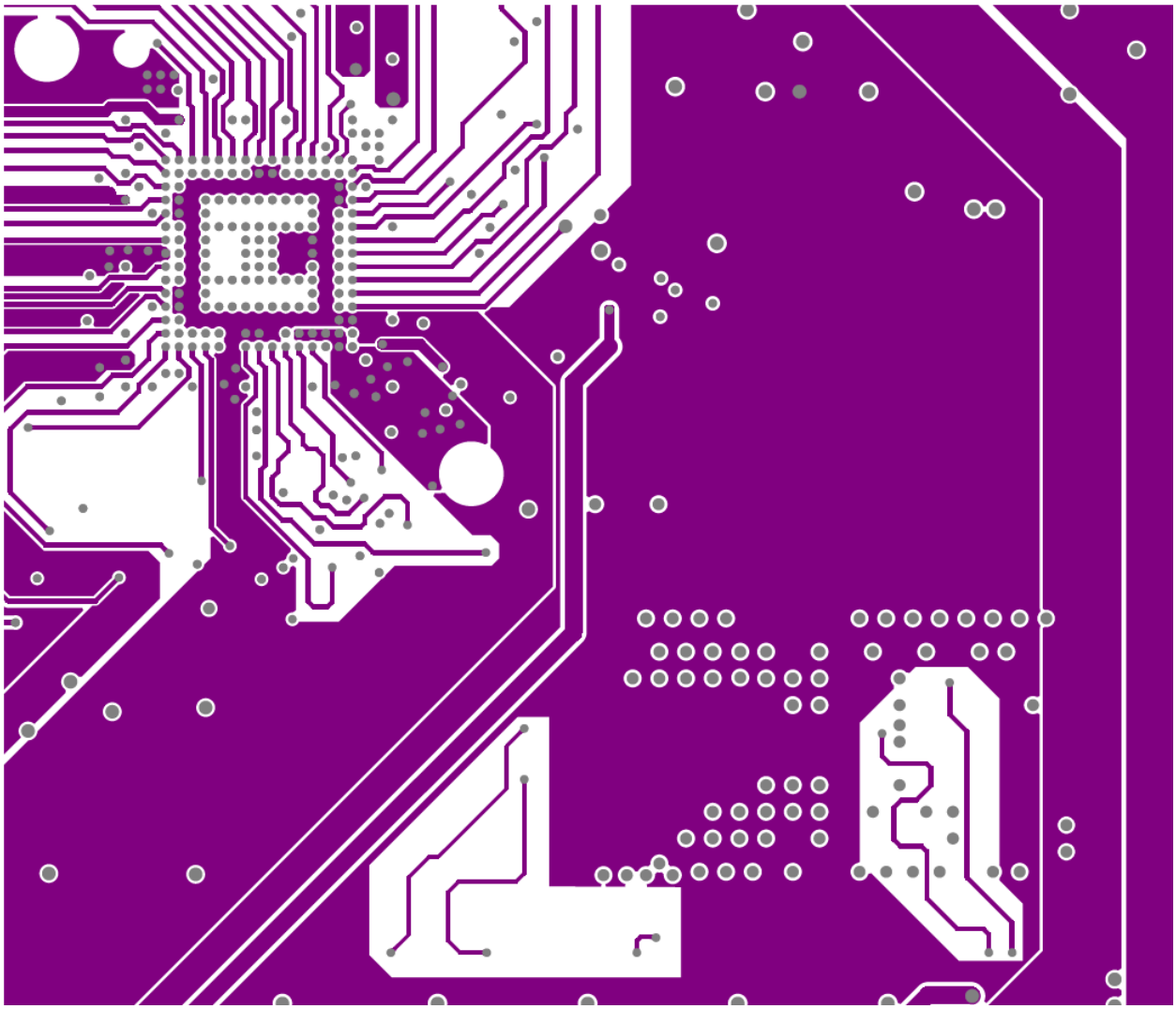


Figure 4-8. SAMA7G54 Layer 7 Example - Ground

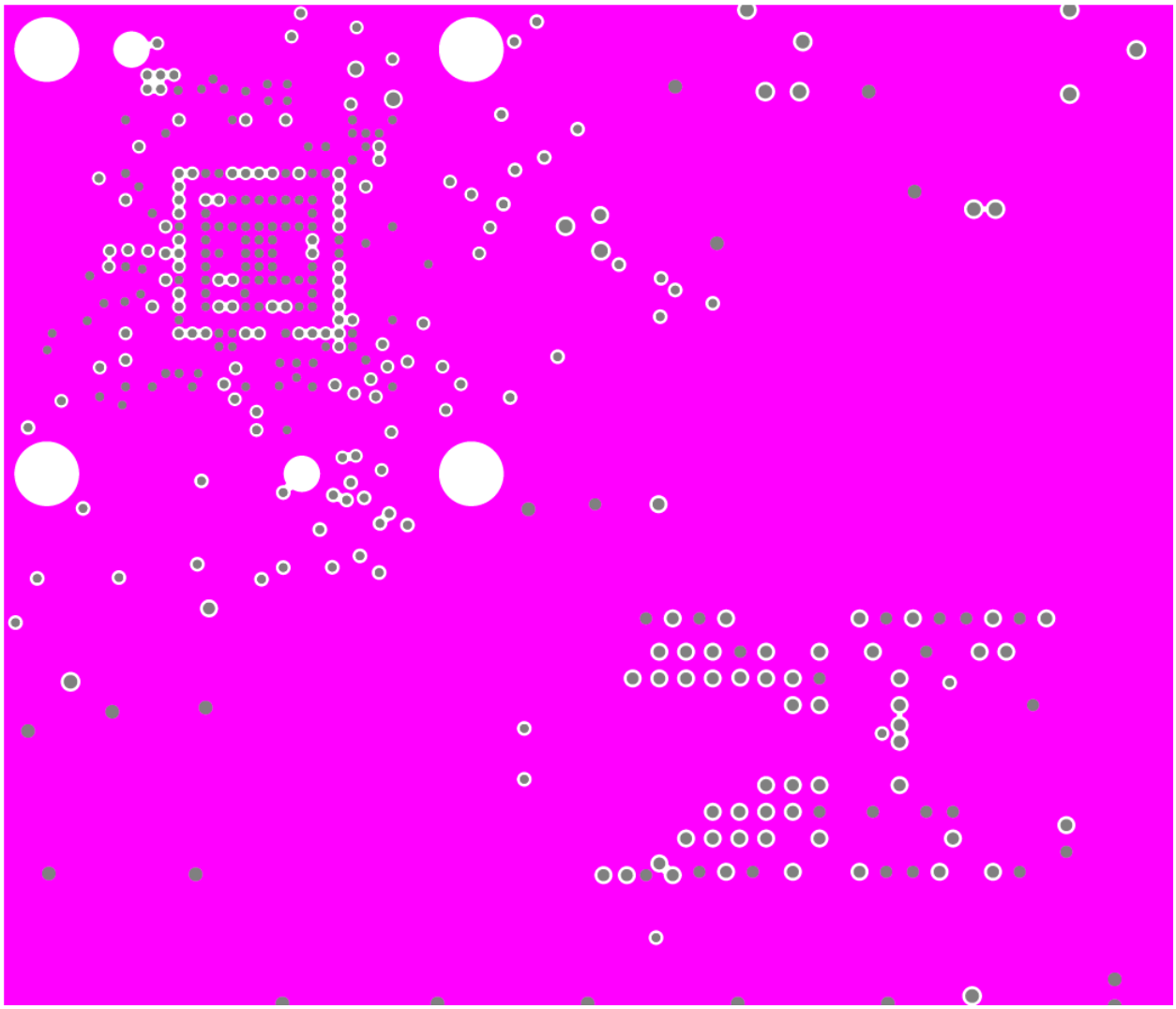
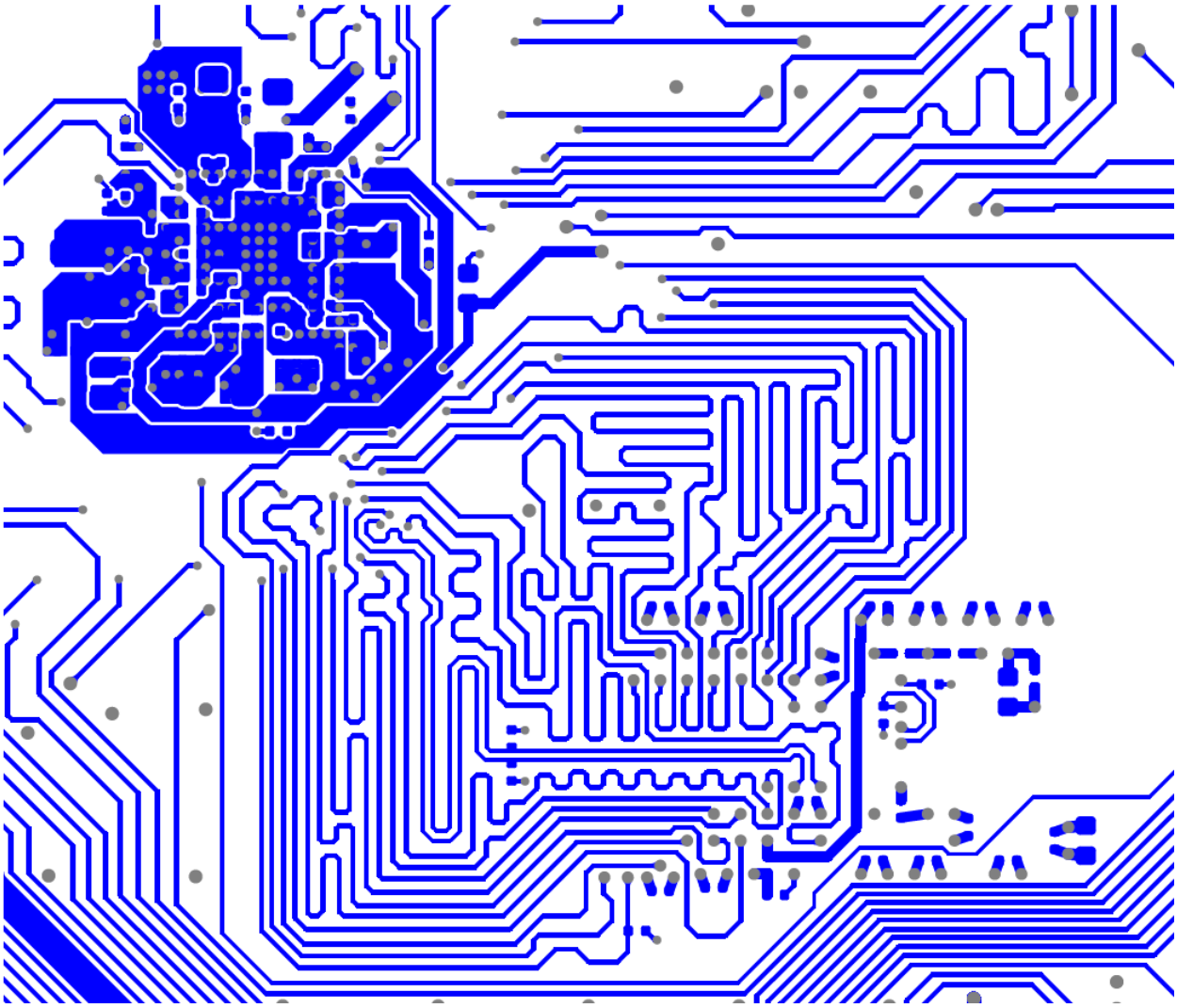
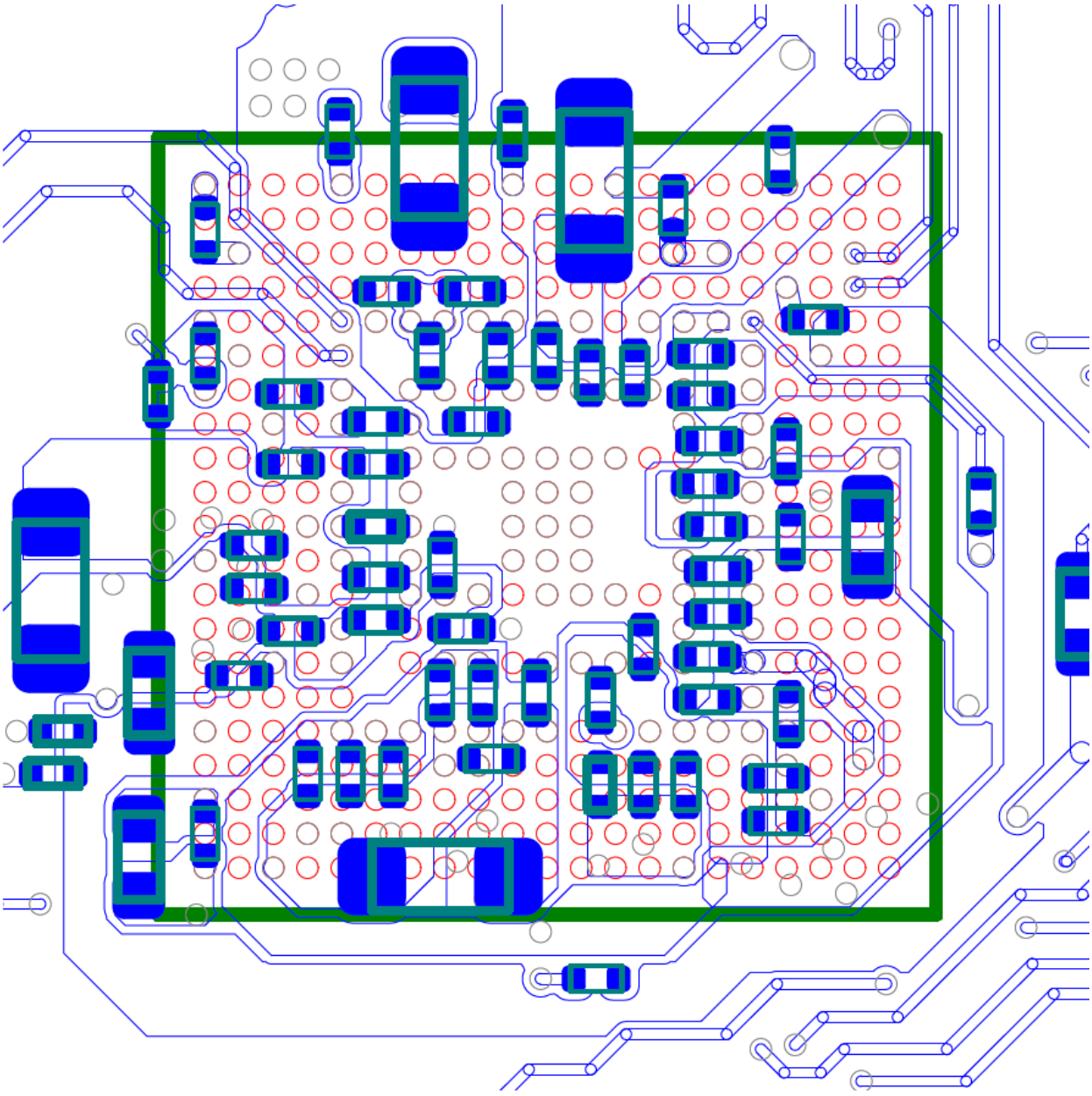


Figure 4-9. SAMA7G54 Bottom Layer Example - Signal



The decoupling capacitors should be placed on the bottom, as close as possible to the vias connecting the power pins of the MPU. An example of such placement can be seen in the following figure.

Figure 4-10. SAMA7G54 Decoupling Capacitors Placement Example



5. Revision History

5.1 Rev. A - 03/2025

Initial Release.

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