



SST25VF040B to SST25PF040C Migration

1.0 INTRODUCTION

The Serial Flash 25 Series family features a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. SPI serial flash memory is manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell

design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

This document lists all the firmware and hardware changes required to migrate from SST25VF040B to SST25PF040C. Refer to the SST25VF040B (DS20005051) and SST25PF040C data sheets (DS20005397) for more information.

TABLE 1-1: SUMMARY OF CHANGES REQUIRED FOR ALL PART NUMBERS AND PACKAGES

Current Part	Recommended Upgrade	Board Layout/ Footprint Change	Firmware Change
SST25VF040B-50-4I-SAE/SAF (8-lead SOIC, 150 mm body)	SST25PF040C-40I/SN (8-lead SOIC)	No	Yes
SST25VF040B-50-4I-S2AE/S2AF (8-lead SOIC, 200 mm body)	SST25PF040C-40I/SN (8-lead SOIC)	Yes	Yes
SST25VF040B-50-4I-QAE/QAF (8-contact WSON)	SST25PF040C-40I/MF (8-contact WDFN)	No	Yes

**TABLE 1-2: PIN LAYOUT COMPARISON,
8-CONTACT PACKAGE**

Pin No.	SST25VF040B	SST25PF040C
1	CE#	CE#
2	SO	SO/SIO1
3	WP#	WP#
4	VSS	VSS
5	SI	SI/SIO0
6	SCK	SCK
7	HOLD#	HOLD#
8	VDD	VDD

SST25VF040B TO SST25PF040C

2.0 MIGRATION CONSIDERATIONS

The following topics should be considered when migrating from SST25VF040B to SST25PF040C.

2.1 Protection at Power-Up

SST25VF040B powers up with the memory protected. This protection must be removed, by clearing the protection bits in the status register, before executing Program or Erase operations.

The SST25VF040B status register has BP0, BP1, BP2, BP3, and BPL protection bits. To clear all protection set these bits to '0', see [Table 2-1](#). These protection bits are volatile and are set to '1' after power up.

Similarly, SST25PF040C offers BP0, BP1, BP2, BPL, and TB as protection bits in the status register, see [Table 2-2](#). However, these protection bits are non-volatile, and the state of protection will remain same before and after a power cycle. Similar to SST25VF040B, the SST25PF040C can execute Program or Erase commands after clearing the protection bits.

TABLE 2-1: SOFTWARE STATUS REGISTER – SST25VF040B

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 2-3)	1	R/W
3	BP1	Indicate current level of block write protection (See Table 2-3)	1	R/W
4	BP2	Indicate current level of block write protection (See Table 2-3)	1	R/W
5	BP3	Indicate current level of block write protection (See Table 2-3)	0	R/W
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are read/writable	0	R/W

TABLE 2-2: SOFTWARE STATUS REGISTER –SST25PF040C

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0 ¹	Indicate current level of block write protection (See Table 2-4)	0 or 1	R/W
3	BP1 ¹	Indicate current level of block write protection (See Table 2-4)	0 or 1	R/W
4	BP2 ¹	Indicate current level of block write protection (See Table 2-4)	0 or 1	R/W
5	TB ¹	1 = 1/8, 1/4, or 1/2 Bottom Memory Blocks are protected (See Table 2-4) 0 = 1/8, 1/4, or 1/2 Top Memory Blocks are protected	0 or 1	R/W
6	RES	Reserved for future use	0	N/A
7	BPL ¹	1 = BP0, BP1, BP2, TB, and BPL are read-only bits 0 = BP0, BP1, BP2, TB, and BPL are read/writable	0 or 1	R/W

1. BP0, BP1, BP2, TB, and BPL bits are non-volatile memory bits.

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The protection bits for SST25PF040C offer both upper and lower memory-block protection. The memory-block protection for SST25VF040B is shown in [Table 2-3](#) and the protection for SST25PF040C is shown in [Table 2-4](#).

TABLE 2-3: SOFTWARE STATUS REGISTER BLOCK PROTECTION– SST25VF040B¹

Protection Level	Status Register Bit ²				Protected Memory Address
	BP3	BP2	BP1	BP0	4 Mbit
None	X	0	0	0	None
Upper 1/8 Top Memory Block Protected	X	0	0	1	070000H-07FFFFH
Upper 1/4 Top Memory Block Protected	X	0	1	0	060000H-07FFFFH
Upper 1/2 Top Memory Block Protected	X	0	1	1	040000H-07FFFFH
All Blocks	X	1	0	0	000000H-07FFFFH
All Blocks	X	1	0	1	000000H-07FFFFH
All Blocks	X	1	1	0	000000H-07FFFFH
All Blocks	X	1	1	1	000000H-07FFFFH

1. X = Don't Care (RESERVED) default is "0"

2. Default at power-up for BP2, BP1, and BP0 is '111'. (All Blocks Protected)

TABLE 2-4: SOFTWARE STATUS REGISTER BLOCK PROTECTION –SST25PF040C

Protection Level	Status Register Bit				Protected Memory Address
	TB	BP2	BP1	BP0	
0 (Full Memory Array unprotected)	X	0	0	0	None
T1 (1/8 Top Memory Block protected)	0	0	0	1	070000H-07FFFFH
T2 (1/4 Top Memory Block protected)	0	0	1	0	060000H-07FFFFH
T3 (1/2 Top Memory Block protected)	0	0	1	1	040000H-07FFFFH
B1 (1/8 Bottom Memory Block protected)	1	0	0	1	000000H-00FFFFH
B2 (1/4 Bottom Memory Block protected)	1	0	1	0	000000H-01FFFFH
B3 (1/2 Bottom Memory Block protected)	1	0	1	1	000000H-03FFFFH
4 (Full Memory Block protected)	X	1	X	X	000000H-07FFFFH

2.2 JEDEC Device ID

The JEDEC Device ID for SST25VF040B is BF258DH.

The JEDEC Device ID for SST25PF040C is 620613H.

2.3 Communication Protocol

Both SST25VF040B and SST25PF040C use SPI protocol. SST25PF040C also supports Dual-Output Read and Dual-I/O Read.

SST25VF040B supports a maximum clock frequency of 50 MHz while SST25PF040C supports a maximum clock frequency of 40 MHz.

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2.4 Commands Compatibility

Most operation commands of SST25VF040B are compatible with SST25PF040C with minimal changes required. See [Table 2-5](#).

TABLE 2-5: OPERATION COMMAND COMPATIBILITY

SST25VF040B Device Operation Instructions	OpCode	Compatible with SST25PF040C	Comments
Read	03H	Yes	
High-Speed Read	0BH	Yes	
4 KByte Sector-Erase	20H	Yes	
32KByte Block Erase	52H	Change Required	This command is not supported by SST25PF040C.
64KByte Block Erase	D8H	Yes	
Chip-Erase	60H or C7H	Yes	
Byte-Program	02H	Yes	
AAI Word-Program	ADH	Change Required	SST25PF040C does not support AAI Word-Program. Instead, perform page programming using the 02H command.
RDSR	05H	Yes	
EWSR	50H	Change Required	Not supported by SST25PF040C
WRSR	01H	Yes	
WREN	06H	Yes	
WRDI	04H	Yes	
RDID	90H or ABH	Change Required	90H command is not supported by SST25PF040C. However, ABH is supported.
JEDEC-ID	9FH	Change Required	Device ID is different between two parts.
EBSY	70H	Change Required	SST25PF040C does not support Hardware End-of-Write detection. Therefore, the device does not support the 70H command.
DBSY	80H	Change Required	SST25PF040C does not support Hardware End-of-Write detection. Therefore, the device does not support the 80H command.

New operation commands that need to be developed are listed in [Table 2-6](#).

TABLE 2-6: NEW OPERATION COMMANDS

Instruction	OpCode
Required Instruction	
Page Programming	02
Instructions to Add Capability (optional)	
Deep Power-Down Mode	B9H
Release DPD Mode	ABH
Fast Read Dual Output	3BH
Fast Read Dual I/O	BBH

2.4.1 32-KBYTE BLOCK ERASE NOT SUPPORTED

SST25PF040C does not support 32-KByte Block Erase and thus the firmware must be modified to instead make use of either 4-KByte Sector Erase or 64-KByte Block Erase.

2.4.2 PAGE PROGRAMMING SUPPORTED

SST25VF040B allow Byte Program and AAI Word Program instructions for programming. SST25PF040C allow Page Program instruction for programming.

Byte Program and AAI Word Program allow programming one and two bytes of data respectively, while the Page Program instruction allows programming one to 256 bytes of data at a time.

For SST25VF040B, the maximum time to program one byte of data using Byte Program instruction, or two bytes of data using AAI-word Program instruction, is 10 μ s. For SST25PF040C, the maximum time to pro-

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gram 256 bytes of data, using Page Program instruction, is 5 ms. If less than 256 bytes of data is programmed, it would take less than the 5 ms maximum time. Before proceeding to the next instruction,

the controller can either wait the maximum program time or keep reading the status register to detect end of programming.

The Byte Program, AAI Word-Program, and Page-Program instructions are shown in Figures 2-1 –2-3.

FIGURE 2-1: BYTE PROGRAM SST25VF040B

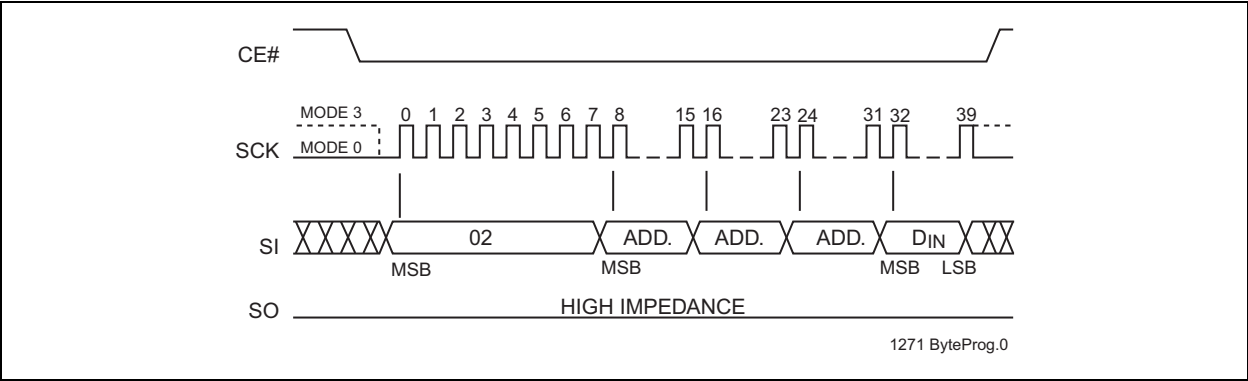
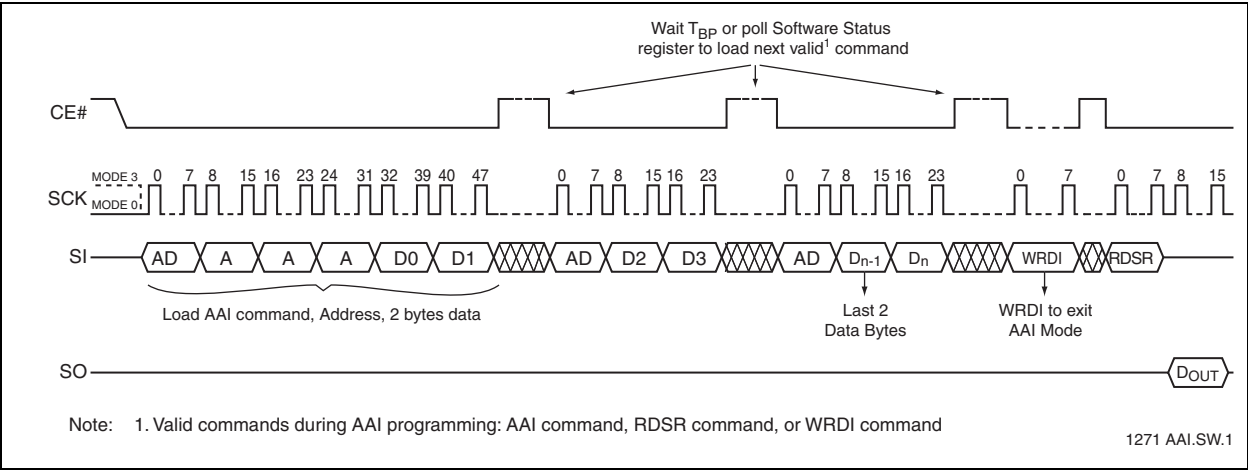
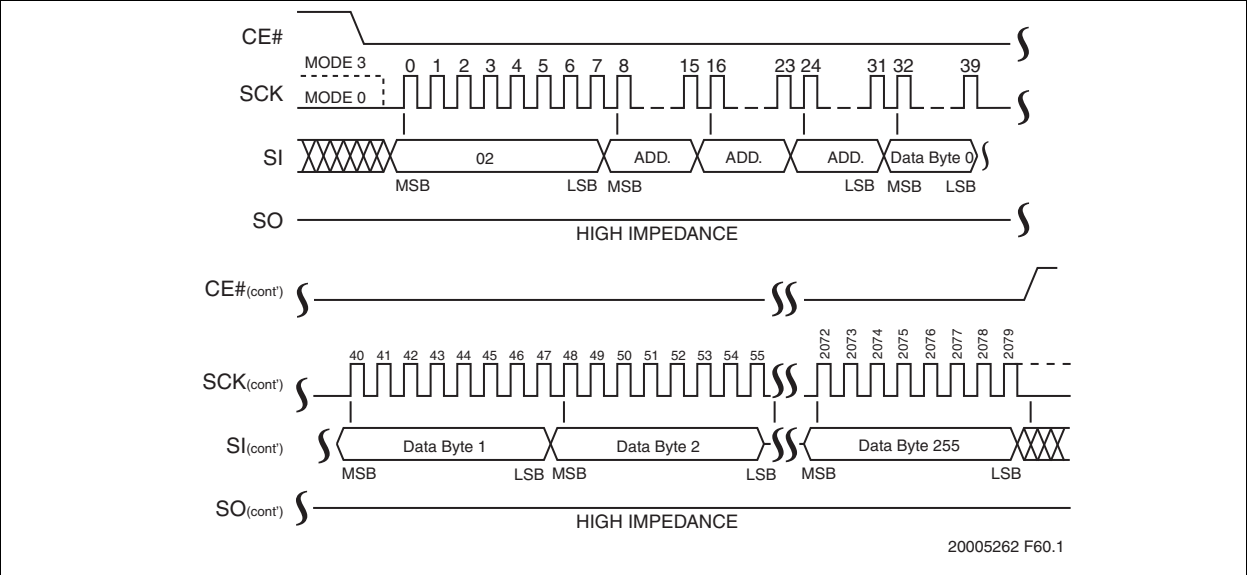


FIGURE 2-2: AAI WORD PROGRAM SST25VF040B



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FIGURE 2-3: PAGE PROGRAM INSTRUCTION SST25PF040C

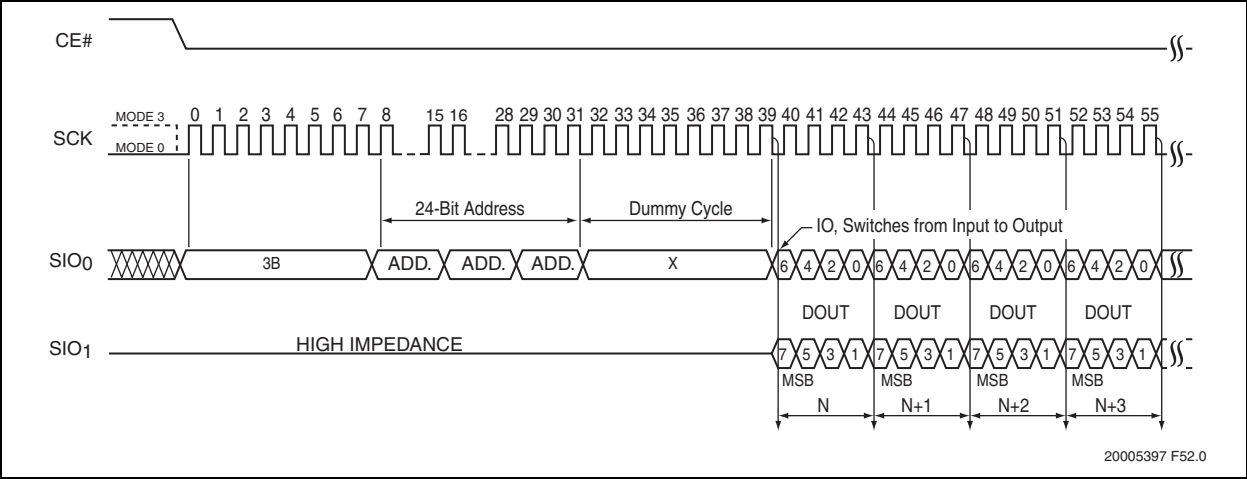


2.4.3 SPI DUAL-OUTPUT READ AND SPI DUAL I/O READ COMMANDS

SST25PF040C supports SPI Dual-Output Read and SPI Dual-I/O Read commands. If the host controller can support these two commands then the Read performance

can be doubled when compared to SST25VF040B. See [Figure 2-4](#) for SPI Dual-Output Read command operation and [Figure 2-5](#) for SPI Dual-I/O Read command operation.

FIGURE 2-4: SPI DUAL-OUTPUT READ SST25PF040C



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ISBN: 978-1-5224-0478-1

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