

$V_{DS(on)}$, $V_{CE(sat)}$ Measurement in a High Voltage, High Frequency System

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INTRODUCTION: The designer of switch mode power conversion system needs to know the total losses of the system, and particularly the proportion of conduction and switching losses.

Measuring the $V_{DS(on)}$ (MOSFET) or $V_{CE(sat)}$ (IGBT) seems easy at first glance, but due to the difference between off-state voltage (400V to 1000V) and on-state saturation voltage (some hundreds of mV to some Volts) and the necessity to keep good resolution, the oscilloscope amplifier input is over driven, causing distortion of the signal.

For the purpose of the illustration, tests were run using the APT50M75JLLU2 power MOSFET as the switch in a boost configuration, but the instrumentation circuits proposed here are also well adapted to IGBTs. The $R_{DS(on)}$ of the switch used for the measurements is 66 m Ω at $T_J = 25^\circ\text{C}$. The mean current is 36A with a peak of 40A at switch turn off. Voltage probes used:

1/10 passive probe (10 M Ω , 9.6 pF)

1/20 differential Probe (8 M Ω , 15 pF) LECROY or PEWATRON. All measurements are made at $T_J = 25^\circ\text{C}$.

1) Example of Scope Input Amplifier Overdriven

The measurement error level is proportional to the ratio between the off-state voltage and the on-state saturation voltage. Fig 1, 2, and 3 show the $V_{DS(on)}$ signal at respectively 100V, 200V, and 400V power supply voltage (at the same switching current).

At $V_{BUS} = 100\text{V}$ the $V_{DS(on)}$ measurement is correct. At 200V the measured $V_{DS(on)}$ is 1.9V too high. Between 200V and 400V the scope input amplifier is substantially overdriven, and the results are definitely wrong.

Fig. 1: Measurement at $V_{BUS} = 100\text{V}$
($V_{DS(on)}$ typical = 2.36V, $V_{DS(on)}$ measured = 2.27V)

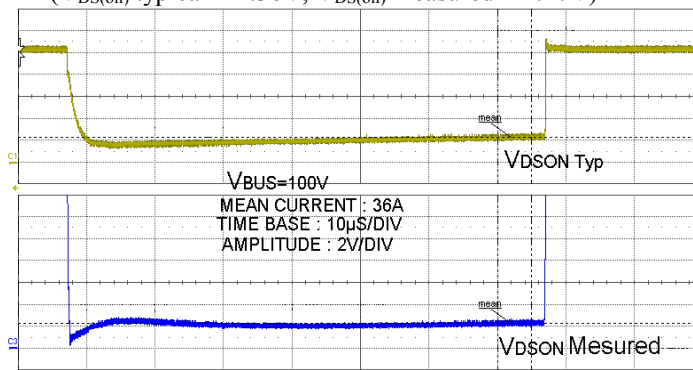


Fig. 2: Input Overdriven at $V_{BUS} = 200\text{V}$
($V_{DS(on)}$ typical = 2.36V, $V_{DS(on)}$ measured = 4.19V)

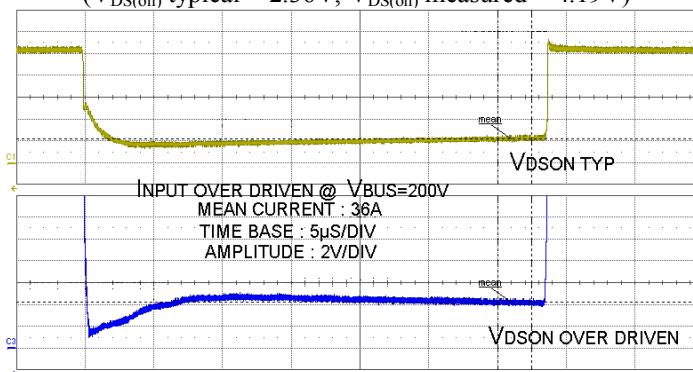
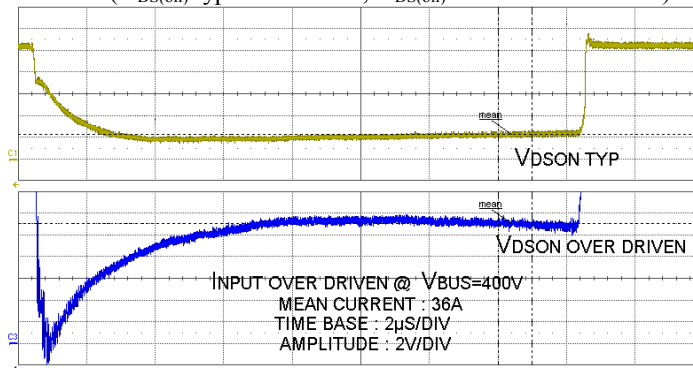


Fig. 3: Input Overdriven at $V_{BUS} = 400\text{V}$
($V_{DS(on)}$ typical = 2.36V, $V_{DS(on)}$ measured = 11.03V)



2) Simple Voltage Clamping Circuit with Zener Diode

The following simple circuit allows making reliable measurements up to 20 kHz switching frequency.

The zener diode clamps the high voltage when the transistor is turned-off. A non inductive and relatively high value resistor is necessary to limit the current through the clamping circuit. With a 400V power supply, a 100kΩ, 2W metal film resistor is a good

compromise between current value and the RC time constant created with the input capacitance of the voltage probe (close to 10pF). This RC time constant explains the frequency limitation of this simple circuit.

In addition a diode is necessary to cancel the effect of the zener diode junction capacitance.

Due to the high input impedance of the probes, the resistor divider introduced by the 100kΩ resistor and the probe impedance does not lead to significant measurement error.

Fig. 4: Zener Clamping Circuit Block Diagram

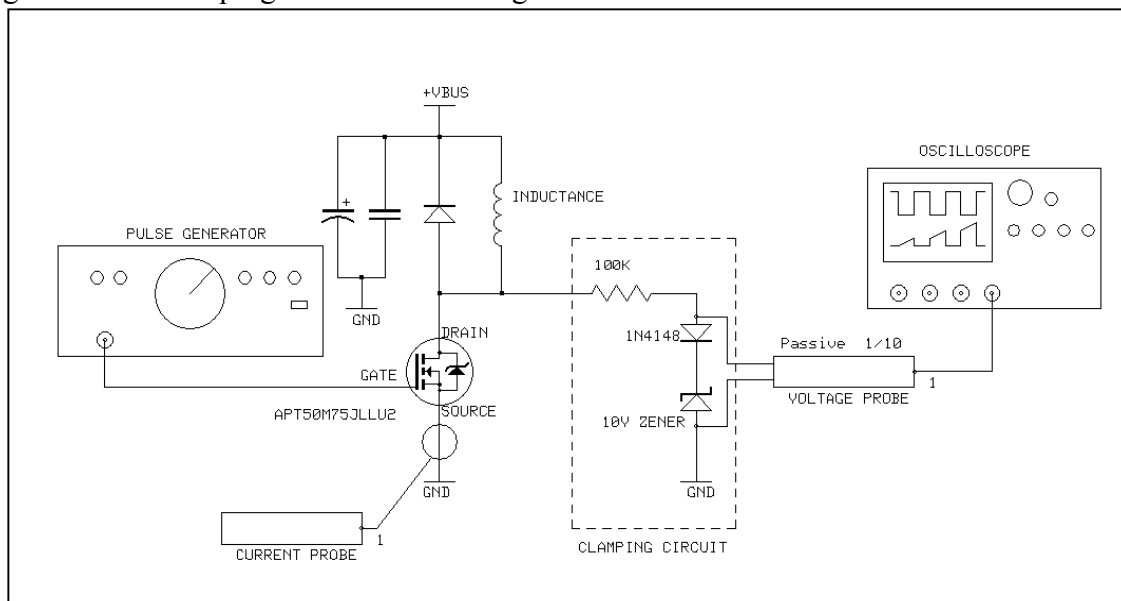
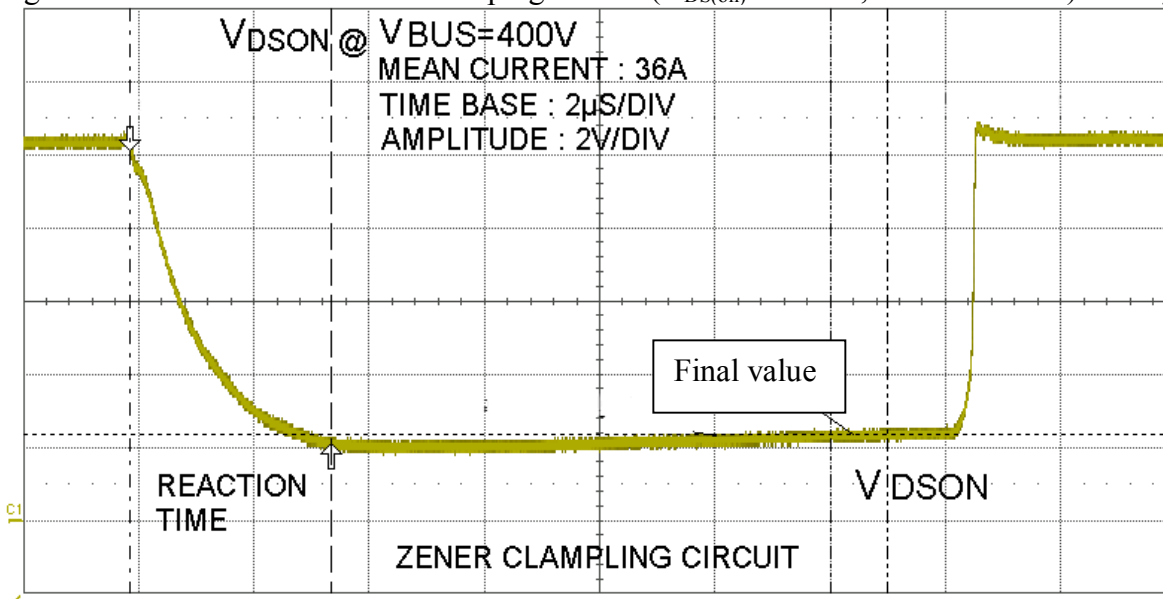


Fig. 5: Measurement with Zener Clamping Circuit ($V_{DS(on)} = 2.34V$, $VBUS = 400V$) Delay 3.5 μs



3) Differential Voltage Clamping Circuit with RF Transistors (Fmax ~ 20kHz in PWM mode)

This circuit must be used when floating measurement is required, such as the top switch in a bridge circuit for example. In all cases the saturation voltage measurement requires well calibrated probes.

Take particular care with the offset of the differential probes (offset null with inputs shorted together).

If there is no possible adjustment, the offset must be subtracted from the results.

The RF transistor used is a ZTX325 from Zetex, but others ultra-fast transistors may be used.

Only base emitter junctions of these transistors are used. One in the forward direction as a conventional diode the other one in reverse direction as a zener diode.

Fig. 6: Block Diagram of RF Transistor Clamping Circuit

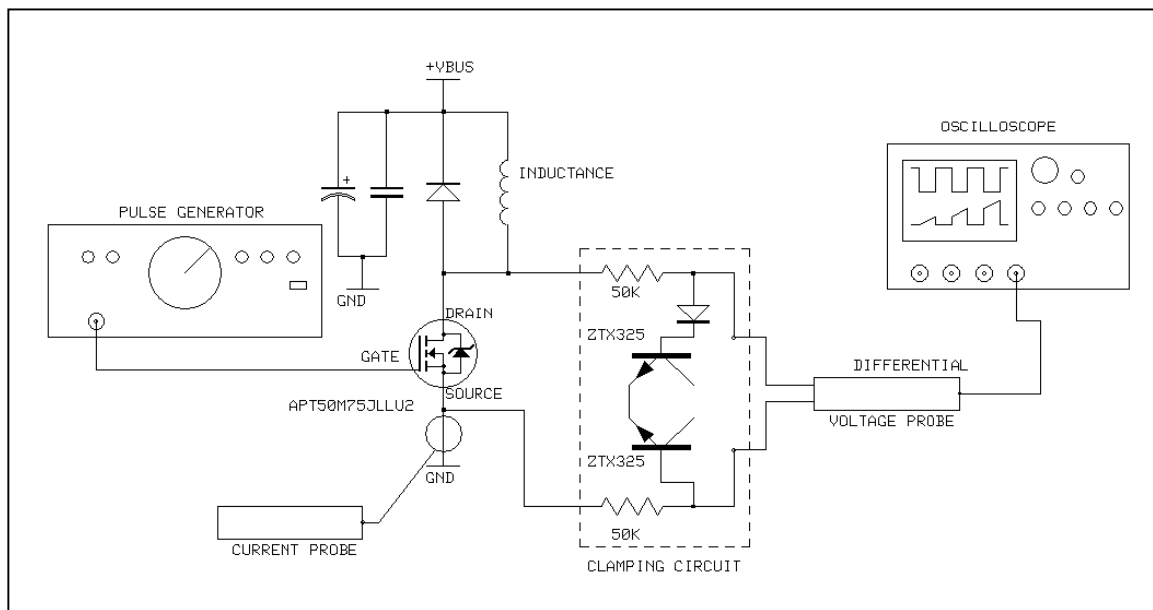
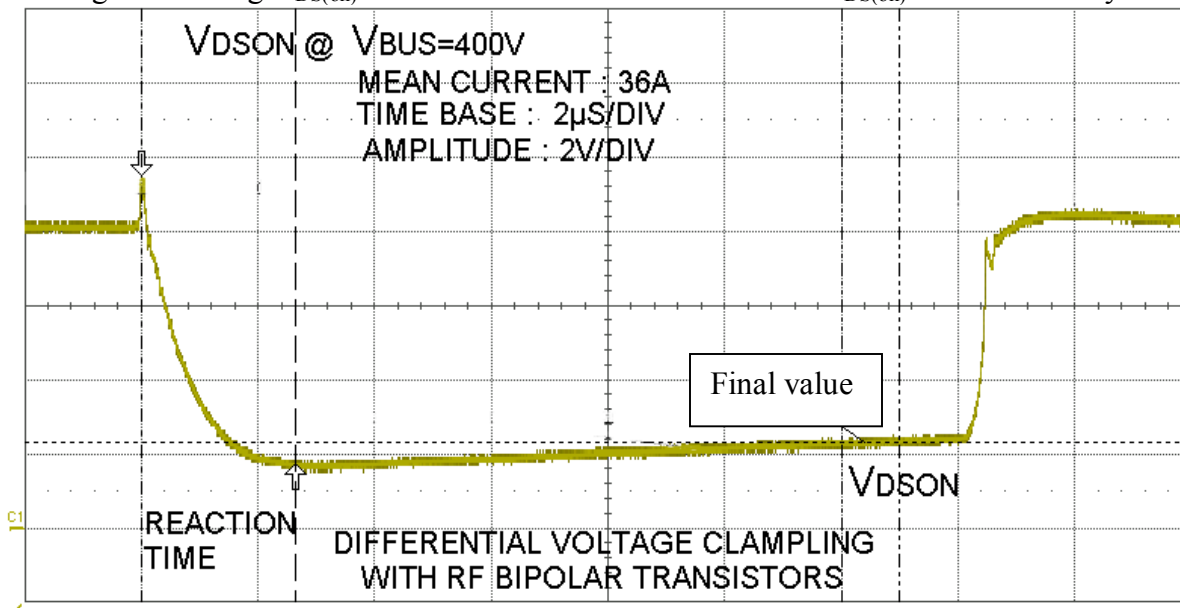


Fig. 7: Floating $V_{DS(on)}$ Measurement in Differential Mode $V_{DS(on)} = 2.32V$ Delay close to $2.5 \mu s$



4) Flash Voltage Clamping Circuit (up to 100kHz)

As already mentioned, the frequency limitation is due to the current limiting resistor (see zener clamping circuit). In the following proposal, JFET (N-Channel) current generators cells are used instead of the current limiting resistors (example: MMBF4392 from ON Semiconductor). The equivalent resistor value is close to 3k Ω during the $V_{DS(on)}$ measurement and 100k Ω at full voltage.

The number of cells depends on the VBUS value and the maximum V_{DS} of the JFET transistor.

In differential mode it is necessary to connect the same number of cells on each side of the clamping component.

It may be necessary to adjust the 560 Ω resistors (labelled 560R in Fig. 8) in order to equalize the voltage of each cell. The spike during the reaction time (see Fig. 9) is due to the JFET clamping circuit and should be ignored.

Fig. 8: Block Diagram of Flash Voltage Clamping Circuit

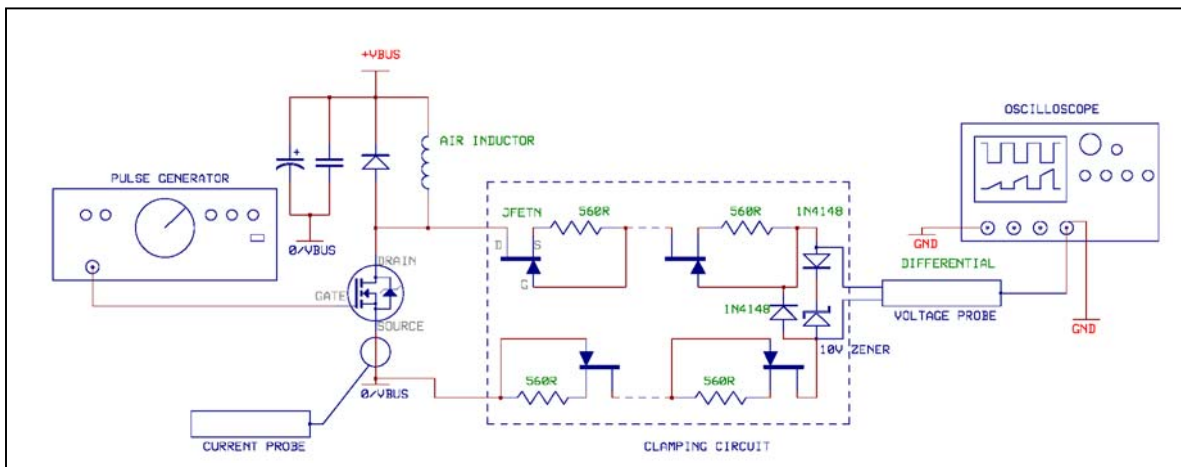
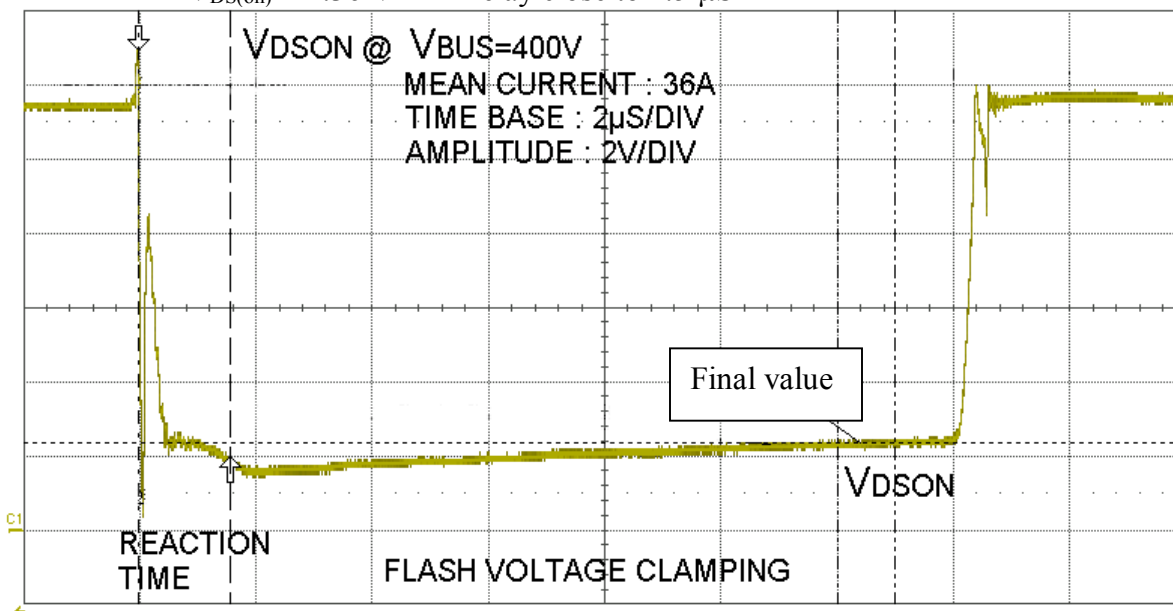


Fig. 9: Floating $V_{DS(on)}$ Measurement in Differential Mode
 $V_{DS(on)} = 2.36 \text{ V}$ Delay close to 1.5 μs



5) Conclusions and Safety Issues

This $V_{CE(sat)} / V_{DS(on)}$ low cost measurement method allows checking the real value of the on-state saturation voltage in a complete system, taking into account all variables such as output current, heat sink and junction temperature, etc.

The flash voltage clamping circuit combined with differential voltage probe ensures a safe measurement.

Disclaimer:

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