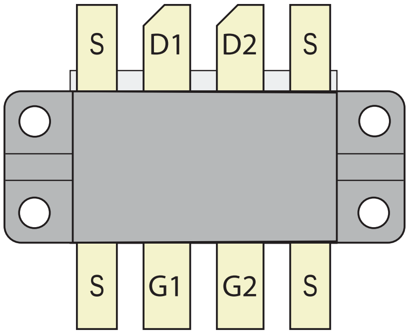
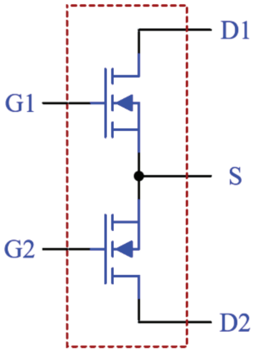
165 V, 100 MHz, 400 W RF Power MOSFET

ARF477FL

Product Overview

The ARF477FL is a matched pair of RF power transistors in a common source configuration. It is designed for high-voltage push-pull or parallel operation in ISM and MRI power amplifiers up to 100 MHz.





Features

- Specified 150 V, 65 MHz characteristics:
  - Output power = 400 W peak
  - Gain = 15 dB (Class AB)
  - Efficiency = 50% minimum
- High-performance push-pull RF package
- High-voltage breakdown and large SOA for superior ruggedness
- Low thermal resistance
- Isolated backside to 500 V
- RoHS compliant

1. Device Specifications

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device. T_C = 25 °C unless otherwise specified.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-source voltage	500	V
V_{DGO}	Drain-gate voltage	500	
I_D	Continuous drain current (each device)	15	A
V_{GS}	Gate-source voltage	±30	V
P_D	Total power dissipation	750	W

1.2 Thermal and Mechanical Characteristics

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance		0.18	0.20	°C/W
$R_{\theta JHS}$	Junction-to-sink thermal resistance (Use high-efficiency thermal grease and planar heat sink surface.)		0.30	0.32	
T_J, T_{STG}	Operating and storage junction temperature	–55		175	°C
T_L	Lead temperature: for 10 seconds			300	
Wt	Weight		5.6		g

ESD practices should comply with JESD-625.

1.3 Electrical Performance

The following table shows the static characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 500 µA	500			V
$V_{DS(ON)}$	On-state drain voltage[1]	$I_{D(ON)}$ = 7.5 A, V_{GS} = 10 V		2.9	4	
I_{DSS}	Zero-gate voltage drain current	V_{DS} = V_{DSS}, V_{GS} = 0 V			45	µA
		V_{DS} = 50 V, V_{GS} = 0 V, T_C = 125 °C			250	
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 7.5 A	3.5	5.6	8	S
g_{fs1}/g_{fs2}	Forward transconductance match ratio	V_{DS} = 15 V, I_D = 5 A	0.9		1.1	
$V_{GS(th)}$	Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = 50 mA	3		5	V
$DV_{GS(th)}$	Gate threshold voltage match	V_{DS} = V_{GS}, I_D = 50 mA			0.2	V

Note:

1. Pulse test: Pulse width <380 µs, Duty Cycle < 2%.

The following table shows the dynamic characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-4. Dynamic Characteristics (per Section)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 150 V, f = 1 MHz		1200	1400	pF
C_{oss}	Output capacitance			150	180	
C_{rss}	Reverse transfer capacitance			60	75	
$t_{d(on)}$	Turn-on delay time	V_{GS} = 15 V, V_{DD} = 250 V, $I_D = I_{D[Cont.]}$ at 25 °C, R_G = 1.6 Ω		7		ns
t_r	Rise time			6		
$t_{d(off)}$	Turn-off delay time			20		
t_f	Fall time			4		

The following table shows the functional characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-5. Functional Characteristics

Parameter	Characteristic	Test Conditions	Min	Typ	Max	Unit
G_{PS}	Common source amplifier power gain	f = 65 MHz, V_{DD} = 150 V, I_{DQ} = 0 mA, P_{out} = 400 W	14	16		dB
η	Drain efficiency		50	55		%
Ψ	Electrical ruggedness VSWR 10:1		No degradation in output power			

1.4 Typical Performance Curves

This section shows the typical performance curves of this device per transistor section unless otherwise specified.

Figure 1-1. Output Characteristics

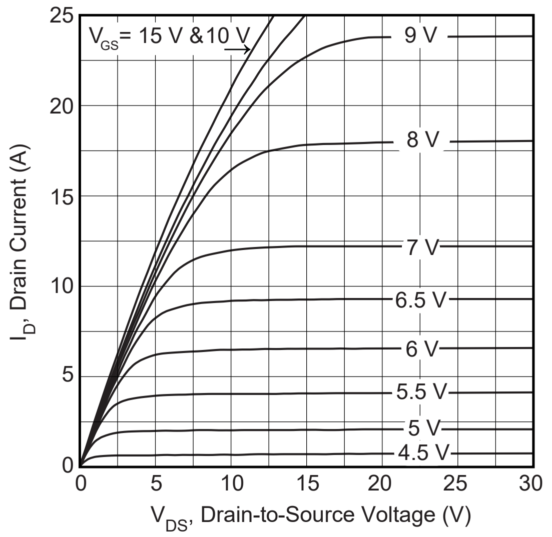


Figure 1-2. Capacitance vs. Drain-to-Source Voltage

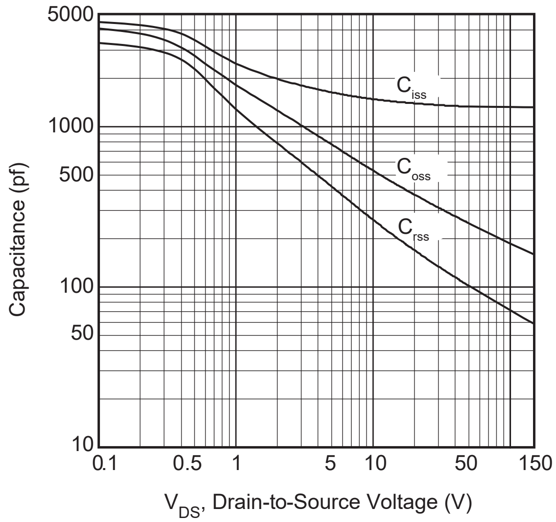


Figure 1-3. Transfer Characteristics

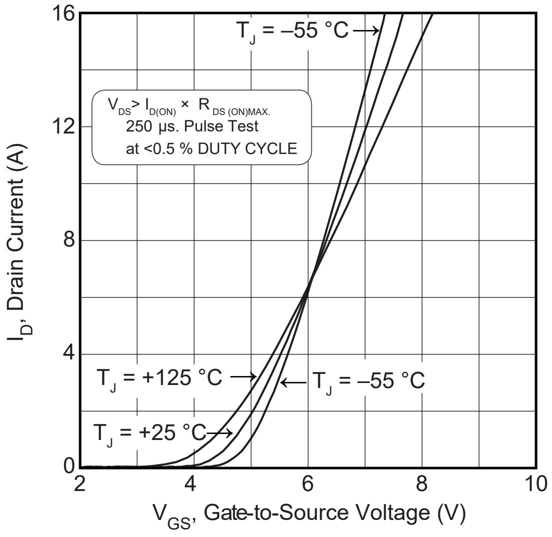


Figure 1-4. Maximum Safe Operating Area

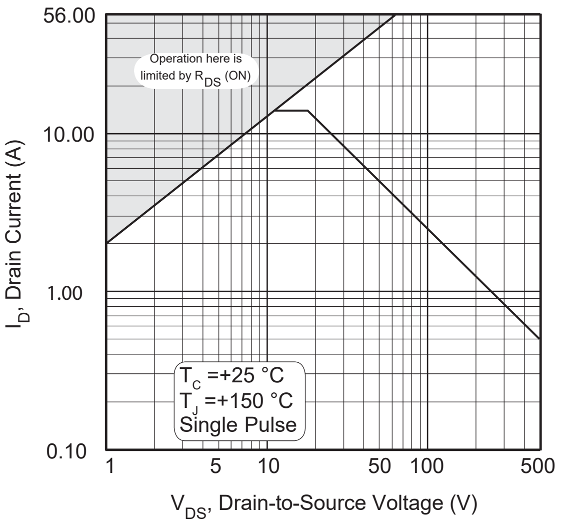


Figure 1-5. Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

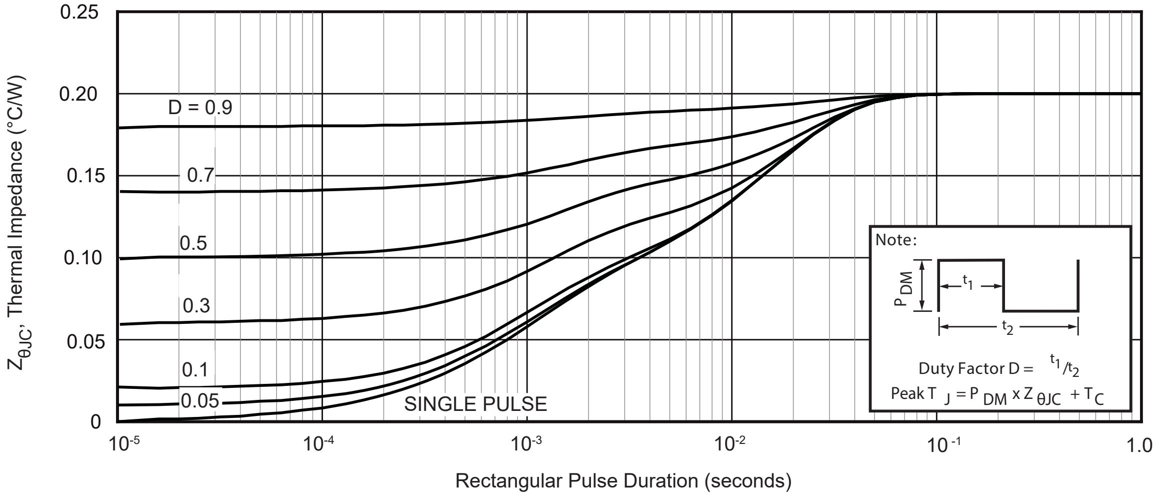
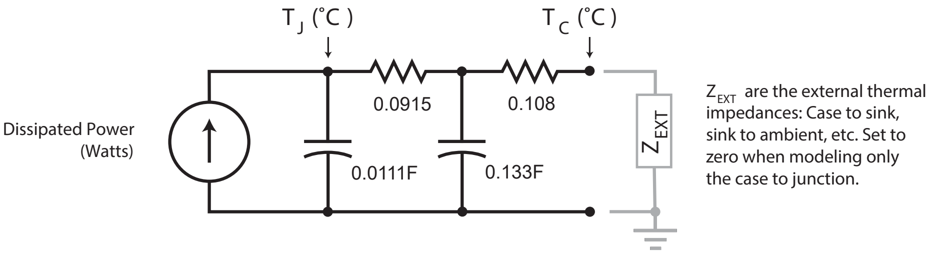


Figure 1-6. Transient Thermal Impedance Model



Z_{EXT} are the external thermal impedances: Case to sink, sink to ambient, etc. Set to zero when modeling only the case to junction.

The following table shows the typical Class AB large signal input-output impedance for this device.

Table 1-6. Typical Class AB Large Signal Input–Output Impedance

Frequency (MHz)	Z_{in} (Ω) Gate-to-Gate	Z_{out} (Ω) Drain-to-Drain
40	1.5 – j 10	24 – j 37
60	1.9 – j 1.3	13 – j 29
80	2.2 – j 0.82	7.9 – j 24

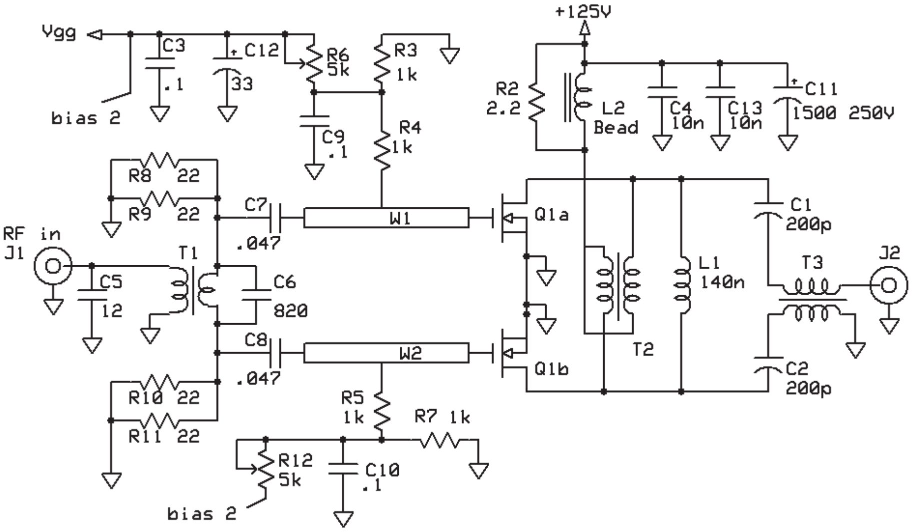
Notes:

- Z_{in} — Gate shunted with 100 Ω
- I_{DQ} = 0 mA each side
- Z_{out} — Conjugate of optimum load for 400 W peak output at V_{dd} = 125 V

2. Test Circuits

The following figure shows the test circuits of this device.

Figure 2-1. 65 MHz Test Circuit



C6 — ATC 100B type	T2 = 6t #22 bifilar on FairRite 5961000301
L1 — 4.5t #18 enam. 0.312” dia.	T3 = 2t RG316 on FairRite 2861010002
L2 — 2t #18 on FairRite 2643800302 bead	Q1a/b ARF477FL
R8-R11 — 22 Ω 1 W SMT	W1, W2 – 1.4” × 0.2”
TL = 4:1 2t #20 1t 1.5” braid on 2861001502	PWB = FR-4 fiberglass er = 4.6
V_{gg} = 5 V	

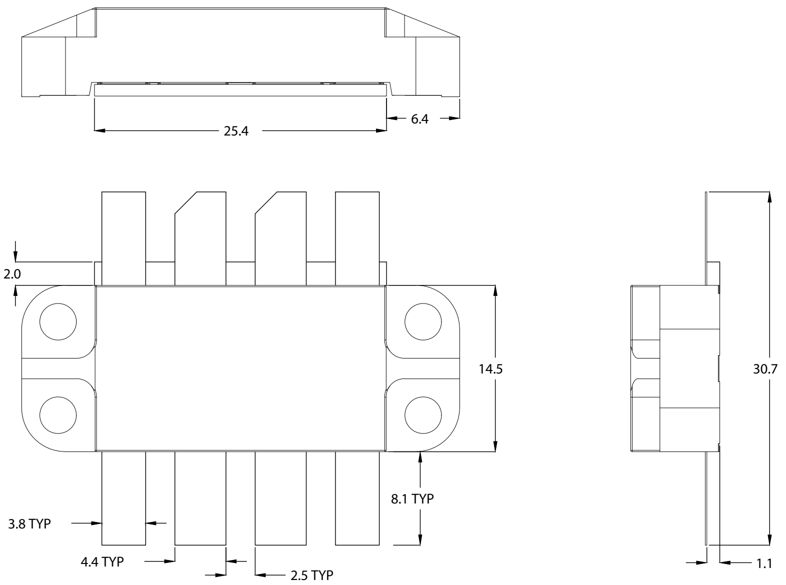
3. Package Specification

This section shows the package specification of this device.

3.1 Package Outline Drawing

The following figure illustrates the package outline of this device. The dimensions in the figure below are in millimeters.

Figure 3-1. Package Outline Drawing



CAUTION

Hazardous Material Warning!
The white ceramic portion of the device between leads and mounting flange is beryllium oxide, BeO. Beryllium oxide dust is highly toxic when inhaled. Care must be take during handling and mounting to avoid damage to this area. These devices must never be thrown away with general industrial or domestic waste.

Note: These devices are sensitive to electrostatic discharge. Proper handling procedures should be followed.

Thermal Considerations and Package Mounting

The rated power dissipation is only available when the package mounting surface is at 25 °C and the junction temperature is 175 °C. The thermal resistance between junctions and case mounting surface is 0.20 °C/W. When installed, an additional thermal impedance of 0.07 °C/W between the package base and the mounting surface is typical. Ensure that the mounting surface is smooth and flat. Thermal joint compound must be used to reduce the effects of small surface irregularities. Use the minimum amount necessary to coat the surface. The heat sink should incorporate a copper heat spreader to obtain best results.

The package design clamps the ceramic base to the heat sink. A clamped joint maintains the required mounting pressure while allowing for thermal expansion of both the base and the heat sink. Four M3 screws provide the required mounting torque. T = 0.4 N·m.

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	09/2024	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00005559A, which replaces the previous Microsemi literature number 050-4952.
Initial releases (Microsemi Revisions A–C)	07/2009 – 07/2014	Initial releases.

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