PIC32CM32/64 JH00 Family Silicon Errata and Data Sheet Clarifications

PIC32CM32/64 JH00

PIC32CM32/64 JH00 Family

The PIC32CM32/64 JH00 family of devices that you have received conforms functionally to the current Device Data Sheet (DS60001880**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table.

The errata described in this document will be addressed in future revisions of the PIC32CM32/64 JH00 family of devices.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. PIC32CM32/64 JH00 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])
		A0
PIC32CM3204JH00032	0x11060x1D	0x7
PIC32CM6408JH00032	0x11060x1C	0x7
PIC32CM3204JH00048	0x11060x1B	0x7
PIC32CM6408JH00048	0x11060x1A	0x7
PIC32CM3204JH00064	0x11060x19	0x7
PIC32CM6408JH00064	0x11060x18	0x7

Note:

1. Refer to the *"Device Service Unit"* chapter in the current Device Data Sheet (DS60001880**A**) for a detailed information on Device Identification and Revision IDs for a specific device.

Silicon Errata Summary

Module	Feature	Errata Number	Issue Summary	Affected Revisions
				A0
AC	INTREF	1.1.1	For AC reference voltage do not use the INTREF.	X
OSC48M	Start-Up	1.2.1	In some very rare cases, the OSC48M internal oscillator may not start at power-up or may not re-start during runtime after having been turned off manually or automatically by the system.	X
OSCCTRL	FDPLL Unlock	1.3.1	Spurious DPLL unlocks may be detected during operation.	X
OSCCTRL	FDPLL ONDEMAND	1.3.2	The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby Sleep mode.	X
SERCOM I²C	Repeated Start	1.4.1	For Host Write operations (excluding High-Speed mode) in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.	X
SERCOM I²C	Repeated Start	1.4.2	For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.	X
SERCOM I²C	NACK and Repeated Start	1.4.3	For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.	X
SERCOM I²C	RXNACK	1.4.4	The RXNACK status bit is invalid during the first DRDY interrupt.	X
SERCOM USART	LIN Host Delays	1.5.1	In SERCOM USART LIN Host mode, when break, sync, and identifier fields are automatically transmitted when data is written with the identifier, the LIN Host Header Delay between the sync and the ID transmission fields is not correct.	X
SERCOM USART	Two stop bits mode in LIN Host	1.5.2	Two stop bits mode is not supported in SERCOM USART LIN Host mode when break, sync, and identifier fields are automatically transmitted when data is written with the identifier.	X

Table of Contents

1. Silicon Errata Issues

The following issues apply to the PIC32CM32/64 JH00 family of devices.

1.1 AC

1.1.1 INTREF

When using the AC module, do not use the INTREF (AC.COMPCTRLx.MUXNEG = INTREF) as an internal reference voltage.

Workaround

Use the DAC (AC.COMPCTRLx.MUXNEG = DAC) for the internal reference of the AC module.

Affected Silicon Revisions

A0			
X			

1.2 OSC48M

1.2.1 Start-Up

In some very rare cases, the OSC48M internal oscillator may not start at power-up or may not re-start during runtime after having been turned off manually or automatically by the system.

Workaround

Failures at power-up can be solved by power cycling the unit.

Failures at runtime can be addressed by keeping the OSC48M always enabled (OSC48MCTRL.ENABLE = 1, OSC48MCTRL.ONDEMAND = 0, OSC48MCTRL.RUNSTDBY = 1).

Affected Silicon Revisions

A0			
X			

1.3 OSCCTRL

1.3.1 FDPLL Unlock

When using FDPLL at temperatures below 25°C, spurious DPLL unlocks (OSCCTRL.DPLLSTATUS.LOCK = 0) may be detected while the FDPLL still adheres to the electrical characteristics metrics defined in section 43.16 of the data sheet. During these unlock periods, the DPLL output clock is halted and then restarts.

Workaround

When using FDPLL at temperatures below 25°C, enable the lock bypass (OSCCTRL.DPLLCTRLB.LBYPASS = 1) to avoid losing FDPLL clock output during a false unlock status. The workaround does not avoid false unlock indications, but it disables the gating of the FDPLL clock output by the lock status; therefore, the clock is issued even if the FDPLL status shows unlocked.

Pseudo Code

Set OSCCTRL.DPLLCTRLB.LBYPASS = 1

Set DPLLCTRLA.ENABLE = 1

Wait (OSCCTRL.DPLLSTATUS.CLKRDY = 1)

Set Source for GCLK with DPLL

Affected Silicon Revisions

A0			
X			

1.3.2 FDPLL ONDEMAND

The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby Sleep mode.

Workaround

Set the DPLLCTRLA.ONDEMAND = 0 which makes the FDPLL96M always run in Standby Sleep mode.

Affected Silicon Revisions

A0			
X			

1.4 SERCOM I^2C

1.4.1 Repeated Start

For Host Write operations (excluding High-Speed mode) in 10-bit Addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.

Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate a Repeated Start.

Affected Silicon Revisions

A0			
X			

1.4.2 Repeated Start

For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

A0			
X			

1.4.3 NACK and Repeated Start

For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

A0			
X			

1.4.4 RXNACK

The RXNACK Status bit is invalid during the first DRDY interrupt.

Workaround

Use a software flag to track when to ignore RXNACK and reset this flag in the I2CS_AMATCH interrupt handler (The workaround is not applicable when AACKEN = 1).

Affected Silicon Revisions

A0			
X			

1.5 SERCOM USART

1.5.1 LIN Host Delays

In SERCOM USART LIN Host mode (CTRLA.FORM = 0x2), when break, sync, and identifier fields are automatically transmitted when data is written with the identifier (CTRLB.LINCMD = 0x2). The LIN Host deader delay between the sync and the ID transmission fields is not correct for the following cases:

- CTRLC.HDRDLY = 0x2: Where the delay between sync and ID transmission fields is 8-bit time instead of 4-bit time.
- CTRLC.HDRDLY = 0x3: Where the delay between sync and ID transmission fields is 14-bit time instead of 4-bit time.

Workaround

None.

Affected Silicon Revisions

A0			
X			

1.5.2 Two stop bits mode in LIN Host

Two Stop Bits mode (CTRLB.SBMODE = 0x1) is not supported in SERCOM USART LIN Host mode (CTRLA.FORM = 0x2) when break, sync, and identifier fields are automatically transmitted when data is written with the identifier (CTRLB.LINCMD = 0x2). One stop bit is only supported.

Workaround

None.

Affected Silicon Revisions

A0			
X			

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device data sheet (DS60001880**A**):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no data sheet clarifications to report.

3. Revision History

Revision A – 02/2025

This is the initial release of the document.

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