

# PIC32CM16/32 GV00 Family Silicon Errata and Data Sheet Clarifications

## PIC32CM16/32 GV00 Family



### PIC32CM16/32 GV00 Family

The PIC32CM16/32 GV00 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001881A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables.

The errata described in this document will be addressed in future revisions of the PIC32CM16/32 GV00 family silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in *Data Sheet Clarifications*, following the discussion of silicon issues.

**Table 1.** SAM D20 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.Revision[3:0])
		A0
PIC32CM1602GV00032	0x10001x17	0x7
PIC32CM3204GV00032	0x10001x16	
PIC32CM1602GV00048	0x10001x15	
PIC32CM3204GV00048	0x10001x14	
PIC32CM1602GV00064	0x10001x13	
PIC32CM3204GV00064	0x10001x12	

**Note:** Refer to the “Device Service Unit” chapter in the current device data sheet (DS60001881A) for a detailed information on Device Identification and Revision IDs for your specific device.

### Silicon Errata Summary

Module	Feature	Errata Number	Summary	Affected Silicon Revisions
				A0
BOD	Hysteresis	1.1.1	BOD33 hysteresis failure upon reset while in the hysteresis window.	X
Device	Clock Failure Detection	1.2.1	After a clock failure detection (INTFLAG.CFD = 1), if INTFLAG.CFD is cleared while the clock is still broken, the system is stuck.	X
Device	Incorrect SYSTICK Calibration Value	1.2.2	The SYSTICK calibration value is incorrect.	X
DAC	Standby Sleep Mode	1.3.1	When DAC.CTRLA.RUNSTDBY = 0 and DATABUF is written (not empty), if the device goes to Standby Sleep mode before a Start Conversion event, DAC.INTFLAG.EMPTY will be set after exit from Standby Sleep mode.	X
EIC	Edge Configuration	1.4.1	When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.	X

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# 1. PIC32CM16/32 GV00 Errata Issues

The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

## 1.1 Brown-out Detection (BOD)

### 1.1.1 Hysteresis

The BOD33 Hysteresis does not work if either an external reset or watchdog reset occurs during the time where the supply voltage is between VBOD(min) and VBOD(max). If one of those resets occur, the device will start operating if the supply voltage is below VBOD(max) but above VBOD(min) and the reset condition is lifted.

#### Workaround

Disable the BOD33 hysteresis (SYSCTRL.BOD33.HYST = 0), and create a virtual hysteresis by configuring:

1. The BOD33 threshold level at power on (BOD33 LEVEL) in the NVM User Row (bits 13:8) as the upper BOD threshold (VBOD(max)).
2. The SYSCTRL.BOD33.LEVEL bit field as the lower BOD threshold (VBOD(min)).

#### Affected Silicon Revisions

A0			
X			

## 1.2 Device

### 1.2.1 Clock Failure Detection

After a clock failure detection (INTFLAG.CFD = 1), if INTFLAG.CFD is cleared while the clock is still broken, the system is stuck.

#### Workaround

After a clock failure detection, do not clear INTFLAG.CFD or perform a system reset.

#### Affected Silicon Revisions

A0			
X			

### 1.2.2 Incorrect SYSTICK Calibration Value

The SYSTICK calibration value is incorrect.

#### Workaround

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the *Arm® Cortex®-M0+ documentation*.

#### Affected Silicon Revisions

A0			
X			

## 1.3 Digital-to-Analog Converter (DAC)

### 1.3.1 Standby Sleep Mode

When DAC.CTRLA.RUNSTDBY = 0 and DATABUF is written (not empty), if the device goes to Standby Sleep mode before a Start Conversion event, DAC.INTFLAG.EMPTY will be set after exit from Standby Sleep mode.

#### Workaround

After waking from Standby Sleep mode, ignore and clear the flag DAC.INTFLAG.EMPTY.

#### Affected Silicon Revisions

A0			
X			

## 1.4 External Interrupt Controller (EIC)

### 1.4.1 Edge Configuration

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.

#### Workaround

Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

#### Affected Silicon Revisions

A0			
X			

## 2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the revision “**A**” of the device data sheet (DS60001881**A**).

**Note:** Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no new Data Sheet Clarifications to report at this time.

### 3. Revision History

#### Revision A - February 2025

Initial Document release.

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