Low-Noise Chip-Scale Atomic Clock (LN-CSAC) SA65-LN User's Guide

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legalinformation/microchip-trademarks.

ISBN:

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXXXXA", where "XXXXXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics, to open a list of available online help files.

PURPOSE OF THIS GUIDE

The LN-CSAC user's guide provides basic recommendations for designing products to use Microchip's Low-Noise Chip-Scale Atomic Clock (LN-CSAC) SA65-LN. The guidelines in the document are generic because specific product requirements vary from one application to the other.

This material consists of a brief description of the LN-CSAC design supported by block diagrams, description of environmental issues, installation guidelines, and unit operation.

WHO SHOULD READ THIS GUIDE

This document is intended for engineers and telecommunications professionals who are designing, installing, operating, or maintaining time, frequency, and synchronization systems having a requirement for a low profile and highly precise frequency generator.

To use this document effectively, you should have a good understanding of digital telecommunications technologies and analog frequency generation and synthesis techniques.

DOCUMENT LAYOUT

This guide contains the following sections:

- **Chapter 1. "Product Overview"**: Provides an overview of the product, describes the major hardware and software features, and lists the system specifications.
- **Chapter 2. "Functional Description"**: Contains the Principle of Operation, Start-Up Sequence, and aspects related to first power-up.
- **Chapter 3. "Programmer's Reference"**: Provides an overview of the telemetry interface and command structure.

- **Chapter 4. "Developer's Kit"**: Describes the package contents and evaluation board information.
- **Chapter 5. "Design Guide"**: Contains information about disciplining, heat sinking, soldering, and additional notes about the evaluation board.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

WARNINGS, CAUTIONS, RECOMMENDATIONS, AND NOTES

Warnings, Cautions, Recommendations, and Notes attract attention to essential or critical information in this guide. The types of information included in each are displayed in a style consistent with the examples below.

WARNING

To avoid serious personal injury or death, do not disregard warnings. All warnings use this style. Warnings are installation, operation, or maintenance procedures, practices, or statements that, if not strictly observed, may result in serious personal injury or even death.

CAUTION

To avoid personal injury, do not disregard cautions. All cautions use this style. Cautions are installation, operation, or maintenance procedures, practices, conditions, or statements, that if not strictly observed, may result in damage to, or destruction of, the equipment. Cautions are also used to indicate a long-term health hazard.

Note: All notes use this style. Notes contain installation, operation, or maintenance procedures, practices, conditions, or statements that alert you to important information, which may make your task easier or increase your understanding.

WHERE TO FIND ANSWERS TO PRODUCT AND DOCUMENT QUESTIONS

For additional information about the products described in this guide, please contact your Microchip representative or your local sales office. You can also contact us on the web at www.microchip.com/csac

When this manual is updated the latest version will be available for downloading from Microchip's web site. Manuals are provided in PDF format for ease of use. After downloading, you can view the manual on a computer or print it using Adobe Acrobat Reader.

Manual updates are available at: www.microchip.com/csac

See your Microchip representative or sales office for a complete list of available documentation.

CUSTOMER SERVICE AND TECHNICAL SUPPORT

To order any accessory, contact the Microchip Sales Department. If you encounter any difficulties installing or using the product, contact Microchip FTS Services and Support:

North and South America

Microchip Technology Inc.
Frequency and Time Systems Group
3870 North First St.
San Jose, CA 95134-1702

Toll-free in North America:	1-888-367-7966, Option 3
Telephone:	408-428-7907

Fax:	408-428-7998
Email:	SJO-FTD.Support@microchip.com
Internet:	https://microchipsupport.force.com/s/

Europe, Middle East, and Africa (EMEA)

Microchip FTS EMEA
Altlaufstrasse 42
85635 Hoehenkirchen-Siegertsbrunn
Germany

Telephone:	+49 700 3288 6435
Email:	FTS.EMEASupport@microchip.com
Internet:	https://microchipsupport.force.com/s/

Asia

Microchip Operations (Malaysia) SDN BHD
Level 15.01, 1 First Avenue,
2A Dataran Bandar Utama,
Damansara 47800 Petaling Jaya,
Selangor, Malaysia

Email:	SJO-FTD.Support@microchip.com
Internet:	https://microchipsupport.force.com/s/

Microchip FTS Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microchip FTS Products. They spend a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:
http://www.microchip.com/support.

DOCUMENT REVISION HISTORY

Revision A (December 2024)

- Initial release of this document as Microchip DS50003805A.

NOTES:

Table of Contents

Chapter 1. Product Overview

1.1 INTRODUCTION

The Microchip Model SA65-LN Low-Noise Chip-Scale Atomic Clock (LN-CSAC) combines the world's lowest power atomic clock with a high-performance ovenized crystal oscillator to realize both long-term atomic stability and exceptional phase noise performance. This user's guide provides the basic guidelines and recommendations for designing products with the LN-CSAC. These guidelines are generic and should be tailored for each application.

This document is intended for engineers, technicians, and technologists who are designing, installing, operating or maintaining time, frequency, and synchronization systems. To use this document effectively, an understanding of digital communication technologies is required. It is advantageous to have a background in frequency generation and synthesis techniques.

1.2 SA65-LN OVERVIEW

The Microchip LN-CSAC provides the accuracy and stability of atomic clock technology with reduced size, weight, and power consumption. The small size (less than 32 cc) and low power consumption of the LN-CSAC (less than 300 mW) enable atomic timing accuracy in portable, battery-powered applications.

FIGURE 1-1: *Microchip SA65-LN Low-Noise Chip Scale Atomic Clock.*

The LN-CSAC provides a 10 MHz sine wave and 1 PPS outputs. It can accept a 1 PPS input to synchronize the output to within 100 ns of a reference clock. It can also discipline its phase and frequency to within 1 ns and 1×10^{-12} of the reference clock, respectively.

This user's guide provides engineering information for use of the LN-CSAC. It also provides supporting information for use of the Developer's Kit (p/n 990-00565-00x).

The design details of the developer's kit can be used to assist with host system design (for example, power conditioning or signal buffering). This guide must be used in conjunction with the current data sheet for LN-CSAC which is available on the Microchip website at www.microchip.com.

CAUTION

To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the LN-CSAC.

1.3 PACKAGING

Retain the original LN-CSAC ESD-safe packaging material in the event that the device needs to be returned to Microchip for service.

1.4 MECHANICAL INTERFACE AND MOUNTING CONSIDERATIONS

The physical dimensions of the LN-CSAC are 2.1" × 2.1" × 0.5" H. Figure 1-2 shows the detailed dimensions of the LN-CSAC. The LN-CSAC baseplate and cover are 80% nickel-iron magnetic alloy per ASTM A753, Type 4 (Mu-Metal or Hy-Mu80™).

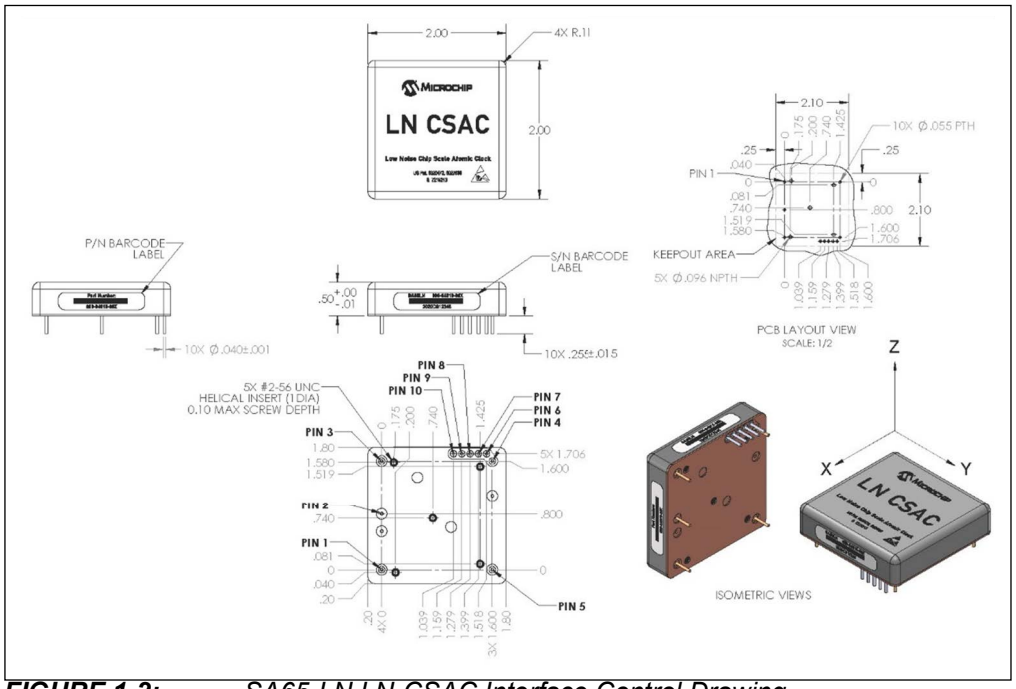
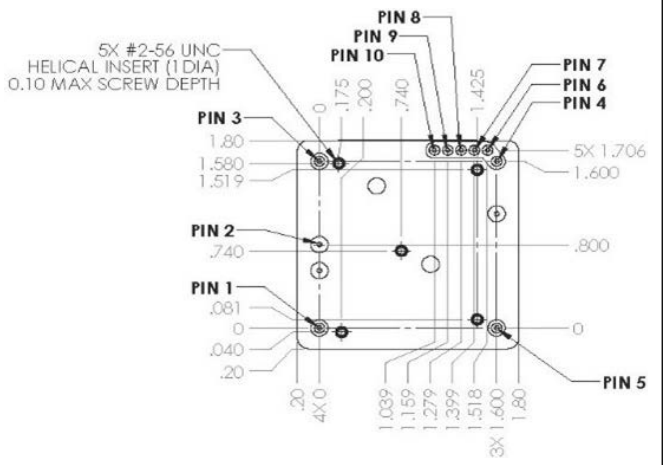


FIGURE 1-2: *SA65-LN LN-CSAC Interface Control Drawing.*

Table 1-1 shows the pinout of the LN-CSAC.

TABLE 1-1: LN-CSAC SA65-LN PINOUT

Pin	Function	Pinout Diagram
1	NO CONNECTION	
2	CHASSIS GND	
3	10 MHz SINE OUT	
4	CHASSIS GND	
5	VCC	
6	BITE	
7	TX	
8	RX	
9	1 PPS IN	
10	1 PPS OUT	

1.5 RECOMMENDED OPERATING CHARACTERISTICS

The LN-CSAC pinout is shown in Table 1-1. The electrical function of each pin is shown in Table 1-2. See the SA65-LN data sheet for updated parameters.

TABLE 1-2: RECOMMENDED OPERATING CHARACTERISTICS

Pin	Function	Level	Reference Section
2, 4	Ground	—	—
3	RF Out	AC Coupled Sine Wave from -1.5V to +1.5V	**Section 2.4 "RF Output Characteristics"**
5	VCC	3.3V ±0.1V	—
6	Built-in Test Equipment (BITE) (Note 1)	LogicH > 2.8V LogicL < 0.3V	**Section 2.3 "Built-in Test Equipment (BITE)"**
7, 8	Serial Communication	2.8V < LogicH < 3.0V 0V < LogicL < 0.3V	**Chapter 3. "Programmer's Reference"**
9	1 PPS In (Note 2)	2.5V < LogicH < 3.3V 0V < LogicL < 0.5V	—
10	1 PPS OUT (Note 3, Note 4)	LogicH > 2.8V LogicL < 0.3V	**Section 2.7 "1 PPS Output"**

Note 1: Built-In Test Equipment: 0 = Normal operation, 1 = Unlock condition

2: Timing reference is rising edge of input pulse on pin 9.

3: Output 1 PPS pulse duration is adjustable from 10 µs to 500,000 µs in increments of 10 µs

4: Timing reference is the rising edge of pin 10. Rise time <10 ns at a load capacitance of 10 pF.

NOTES:

Chapter 2. Functional Description

The following is a functional description of the LN-CSAC.

2.1 PRINCIPLE OF OPERATION

The LN-CSAC is a passive atomic clock, incorporating the interrogation technique of coherent population trapping (CPT) and operating on the D1 optical resonance of atomic cesium. A complete description of passive atomic clocks, CPT, and the LN-CSAC architecture is beyond the scope of this user's guide. The following illustration shows a simplified block diagram of the LN-CSAC.

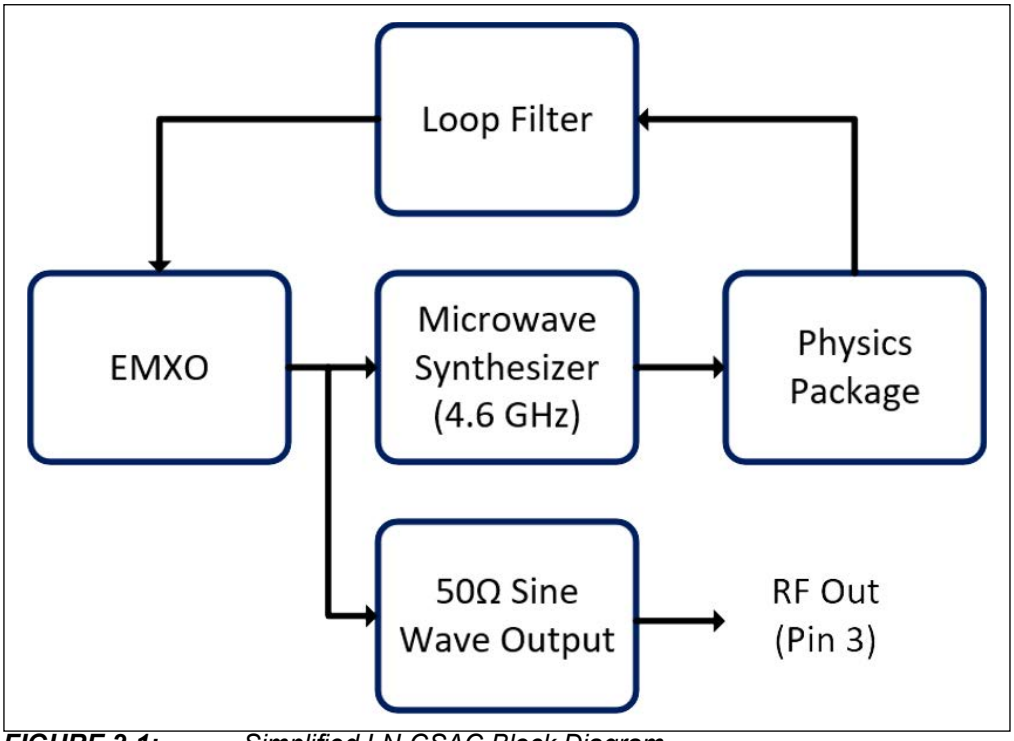


FIGURE 2-1: *Simplified LN-CSAC Block Diagram.*

The principal RF output from the LN-CSAC is provided by an evacuated miniature crystal oscillator (EMXO). In normal operation, the frequency of the EMXO is continuously compared and corrected to the ground state hyperfine frequency of the cesium atoms, contained within the physics package, which thereby improves the long-term stability and environmental sensitivity of the EMXO. In addition to the EMXO and the physics package (Note 1), the essential components of the LN-CSAC are the microwave synthesizer and the microprocessor (Note 2). The microwave synthesizer generates 4596.3 MHz with tuning resolution of approximately 1×10^{-12}. The microprocessor serves multiple functions, including implementation of the frequency-lock loop filter for the EMXO, optimization of physics package operation, state-of-health monitoring, and command and control through the serial communications port.

When the LN-CSAC is initially powered on, it performs an acquisition sequence, which includes stabilizing the temperature of the physics package, optimizing physics package operating parameters, and acquiring frequency lock to the atomic resonance. The acquisition process may be monitored through the status field of the telemetry (see **Section 3.3.1 "Telemetry (6 and ^)"**). On power-up, the status begins at 8 (oven warm-up). The status value decrements numerically through the acquisition until normal operation (status = 0) is achieved. On rare occasions, the status countdown will reset during the acquisition. This is normal behavior if it does not disrupt the time-to-lock specification.

Note 1: R. Lutwak, et. al., The Chip-Scale Atomic Clock - Low-Power Physics Package, Proceedings of the 36th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting, December 7–9, 2004, Washington, DC.

2: R. Lutwak, et. al., The MAC - A Miniature Atomic Clock, Proceedings of the 2005 Joint IEEE International Frequency Control Symposium and Precise Time & Time Interval Systems & Applications Meeting, August 29–31, 2005, Vancouver, BC.

2.2 START-UP SEQUENCE

CAUTION

To avoid severe damage to the unit, do not apply power to the incorrect terminals. The LN-CSAC does not have reverse voltage protection.

When power is connected to pin 5 the LN-CSAC unit begins its warm-up cycle. 10 MHz and 1 PPS output signals appear immediately upon power-up, but the output signals are not stable until the atomic control loop is locked (indicated CMOS low on the BITE pin and also by the "status" telemetry field).

Within 3 minutes at 25°C, the LN-CSAC achieves Lock and BITE = 0 (**Section 2.3 "Built-in Test Equipment (BITE)"**). Power consumption during warm-up is greater than during normal operation; as specified on the LN-CSAC data sheet.

It is recommended to always allow the LN-CSAC to remain powered on for >120 seconds after it acquires LOCK, after which the LN-CSAC will store the recently acquired set points to memory. Allowing the LN-CSAC to periodically store its set points minimizes the possibility of the LN-CSAC subsequently powering on with obsolete set points. Otherwise, upon the next power up, the unit may need to reacquire its set points and time-to-lock may be out of specification.

2.3 BUILT-IN TEST EQUIPMENT (BITE)

While the preferred method for monitoring LN-CSAC state of health is with the "status" parameter, it can also be monitored electronically on pin 6 (BITE) of the LN-CSAC. Frequency lock is indicated both by status = 0 in the status field of telemetry and by the electrical state of the BITE output pin, which is high (logic 1) upon initial power-on and whenever status ≠ 0. The BITE pin is a high impedance CMOS logic output.

Note: When not locked, BITE = 1 and status ≠ 0 in the status field of the telemetry output string.

At the conclusion of the acquisition sequence (status = 0), BITE remains high for an additional 5 seconds to avoid false indication in the event of acquisition failure. Subsequently, BITE provides an immediate (within 2 seconds) indication of lock failure or alarm.

2.4 RF OUTPUT CHARACTERISTICS

The sine wave output is provided on pin 3 of the LN-CSAC. The output series impedance is 50Ω. For reference, the output driver circuit of the LN-CSAC is shown in the following illustration.

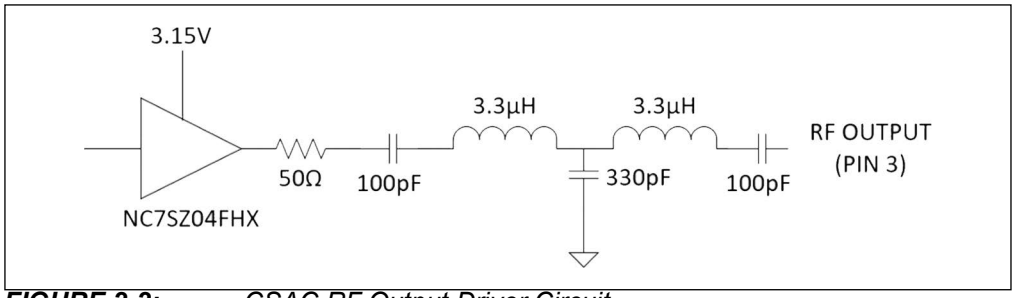


FIGURE 2-2: *CSAC RF Output Driver Circuit.*

The RF output appears on pin 3 after the LN-CSAC is powered ON and is always present, regardless of the lock status. When the LN-CSAC is out of lock (BITE = 1, status ≠ 0), the output frequency is provided by the free-running TCXO. Typically, the unlocked frequency accuracy during acquisition is significantly better than $<1 \times 10^{-8}$ as the LN-CSAC memorizes its last-known-good tuning voltage and restores this voltage upon power-up and/or subsequent recovery from loss-of-lock.

2.5 WHAT TO EXPECT DURING FIRST POWER-UP

The LN-CSAC output frequency is calibrated prior to shipment. However, the shipment conditions may affect the absolute frequency offset when received by the end-user due to temperature excursions, vibration, duration of transit, and so on. As such, some frequency offset should be expected when the LN-CSAC is first powered on by the user. Off- sets may be corrected, as explained in **Section 2.6 "Frequency Adjustment"**.

2.6 FREQUENCY ADJUSTMENT

> **Note:** Clockstudio™ software is a graphical interface provided for communication and evaluation of LN-CSAC. To display the functionality of the LN-CSAC, screen shots of Clockstudio are included in the sections that follow. For more information on Clockstudio, refer to the Clockstudio User's Guide. See **Section 4.4 "Clockstudio Software Information"** for installation.

For external steering and/or calibration, the LN-CSAC internal microwave synthesizer may be adjusted by the user through the `!F` command (see **Section 3.3.2 "Frequency Adjustment (F)"**). Steering values are entered in (integer) units of 1×10^{-15}, though the resolution realized by the LN-CSAC hardware is approximately 1×10^{-12}. Steering commands may be entered as either absolute steers (`!FA`) or as relative steers (`!FD`). In the case of an absolute steer, the contents of the steer register are replaced with the new value. In the case of a relative steer, the new value is summed with the existing value in the steer register. In either case, the maximum steer that can be applied to the LN-CSAC is $\pm 2 \times 10^{-8}$ ($\pm 2000000000 \times 10^{-15}$). If a larger value is sent to the LN-CSAC, the maximum allowed steer is applied.

To overcome the software steering limit of ±2 × 10^{-8}, the frequency latch command (`!FL`) may be employed (for more information, see **Section 2.6.1 "Frequency Calibration"**). Ultimately, the LN-CSAC steering capability is physically limited by the EMXO tuning voltage. An alarm will trigger when this voltage is breached.

Note:	Steering commands can only be entered when the unit is locked (Status=0). Steering commands entered when Status ≠ 0 are ignored.

Frequency steering is volatile. Upon reboot, the LN-CSAC returns to its nominal (calibrated) frequency setting. To update the non-volatile calibration, use the Frequency Latch command (**Section 3.3.2 "Frequency Adjustment (F)"**).

Note:	Steer reports the actual hardware steering, in units of ×10^{-12}, even though the software registers maintain resolution of ×10^{-15}, so that many small relative corrections may be applied. As a result, the reported value may appear to disagree with the applied correction in the lowest digit due to roundoff error. An example is provided in **Section 3.3.2 "Frequency Adjustment (F)"**.

The current steering value appears in the telemetry string as Steer.

To apply a frequency correction from Clockstudio, click on the Frequency Adjustment tab, then select relative or absolute from the pull-down menu and enter the desired steering into the Digital Tune field in ×10^{-15}.

Figure 2-3 shows an example where an absolute correction of -100000 ×10^{-15} is entered. The correction is applied to the LN-CSAC when **Apply** is selected.

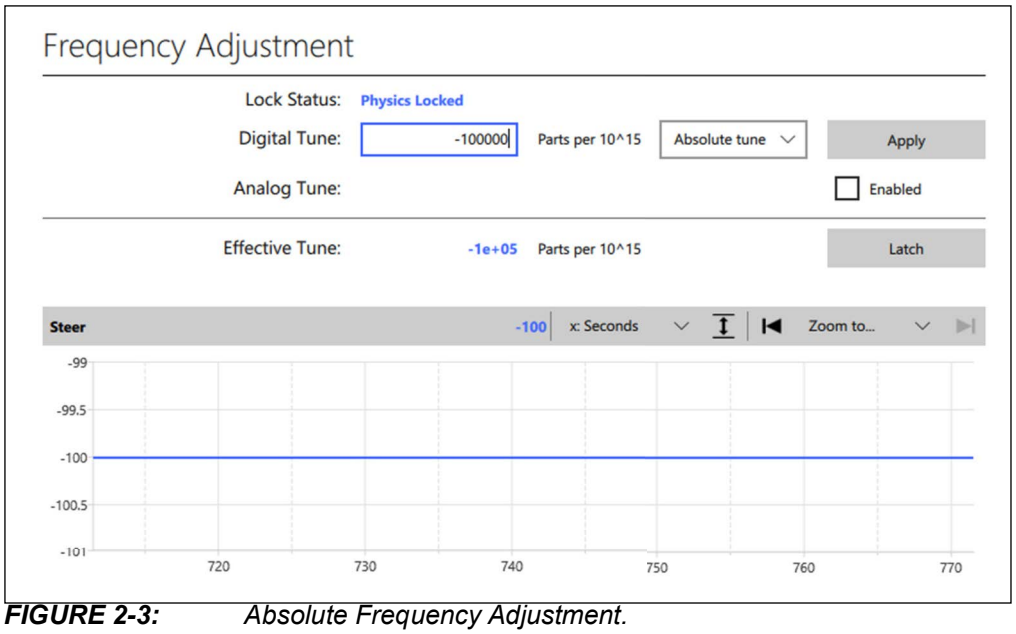


FIGURE 2-3: *Absolute Frequency Adjustment.*

As shown in Figure 2-3, after Apply is clicked, the correction is applied to the LN-CSAC and the value of Steer changes (on the next polling update) to indicate the internal correction of –100 × 10^{-12}.

Figure 2-4 shows an example of relative frequency tuning after absolute steer is reset to 0. In this example, each time Apply is clicked, an additional correction of –100000 × 10^{-15} is applied to the LN-CSAC. In this screen shot, Apply has been clicked a total of four times. The resultant value of Steer is –400 × 10^{-12}.

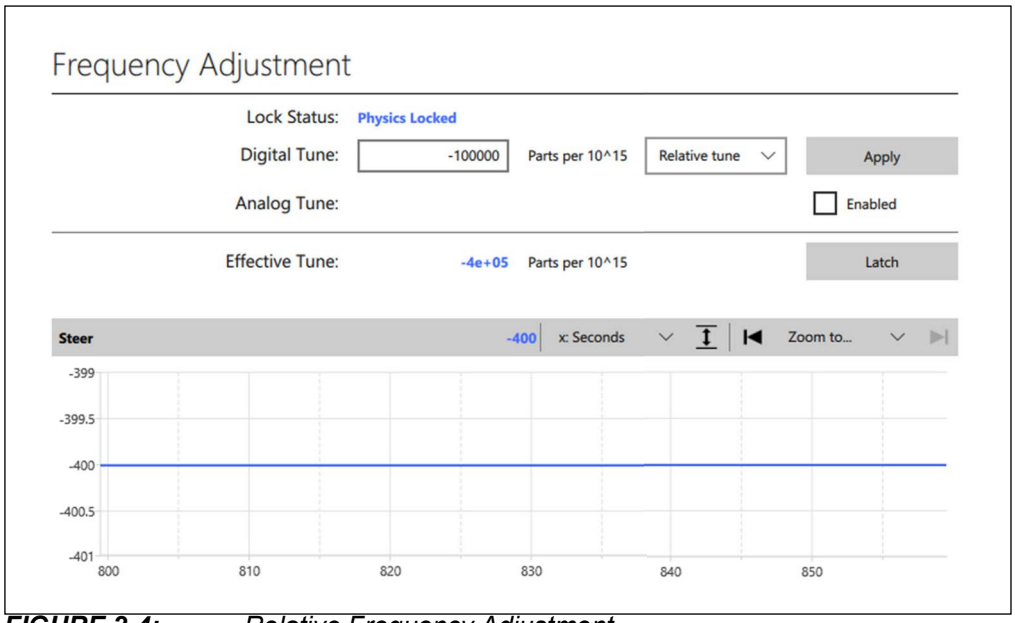


FIGURE 2-4: *Relative Frequency Adjustment.*

2.6.1 Frequency Calibration

The internal frequency calibration of the LN-CSAC is set prior to shipment. The calibration may need to be updated from time to time to remove cumulative frequency aging off- sets.

Calibration of the LN-CSAC is a two-step process. First, the LN-CSAC is steered onto frequency, either through an external `!F` command (see **Section 2.6 "Frequency Adjustment"**) or through 1 PPS disciplining (see **Section 2.10 "1 PPS Disciplining"**). Second, the present value of Steer is summed into the non-volatile calibration register through the Frequency Latch command (see **Section 3.3.2 "Frequency Adjustment (F)"**). Following a Latch command, the value of Steer resets to zero.

Note:	The Latch command is only valid when the LN-CSAC is locked (Status = 0).

To latch the current steer value to non-volatile storage from Clockstudio, click **Latch**.

Note:	It may be tempting, particularly in disciplining applications, to frequently latch the steering value into calibration in the event of unforeseen power outage. This is highly discouraged for the following reason. The lifetime of the LN-CSAC's non-volatile memory is finite; updating it >20,000 times will damage it and render the LN-CSAC inoperable.

2.7 1 PPS OUTPUT

A CMOS level 1 pulse-per-second (1 PPS) output is available on pin 10 upon power-up (PPSOUT). The output series impedance is 200Ω. Nominal levels are 0VDC to 3.3VDC. For synchronization purposes, the on-time point is the rising edge of pin 10.

The PPSOUT signal is derived by digital division of the RF reference frequency. The frequency stability and accuracy of PPSOUT reflects that of the RF output. When unlocked (BITE = 1, status ≠ 0), PPSOUT stability reflects that of the free-running EMXO.

Control of PPSOUT signal, synchronization, and disciplining is provided on the 1 PPS Disciplining tab in Clockstudio. The 1 PPS Disciplining tab is shown in Figure 2-5.

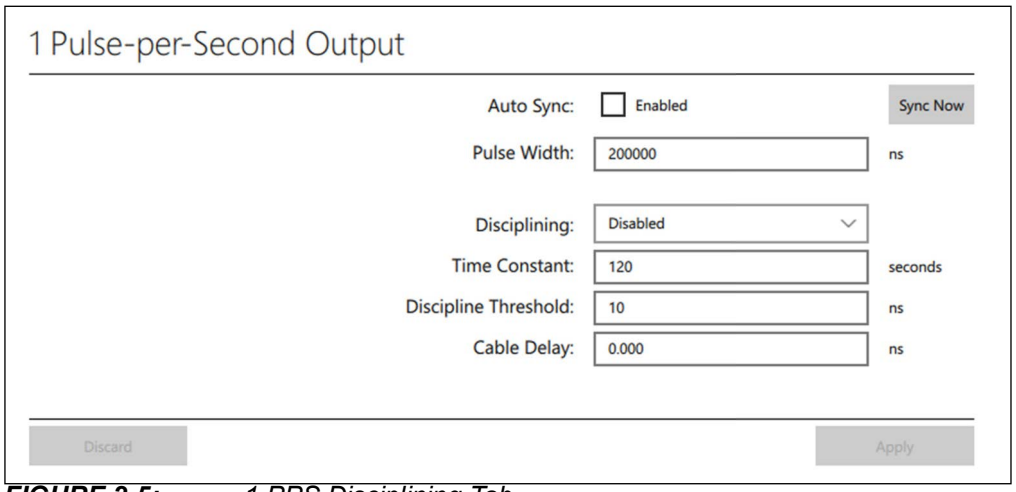


FIGURE 2-5: *1 PPS Disciplining Tab.*

The output pulse width (PPSWidth) of PPSOUT can be set to a value between 10 µs and 500,000 µs in increments of 10 µs by adjusting PPSWidth (See **Section 3.3.10 "Set PPSWidth (>)"**). To adjust PPSWidth from Clockstudio, enter the new value (in nanoseconds) into the Pulse Width field and click **Apply**.

Note:	The increments of PPSWidth are under the assumption of a 10 MHz LN-CSAC. For an LN-CSAC with a different output frequency, consult the datasheet for the available increments of PPSWidth.

2.8 TIME-INTERVAL COUNTER

The LN-CSAC accepts a user-supplied 1 PPS input reference signal as an input on pin 9 (PPSEXT). The LN-CSAC time-interval counter (TIC) measures the time interval (TI) between the rising edges of PPSOUT and PPSEXT. The TIC measurement is reported in the telemetry field "**Phase**" (see **Section 3.3.1 "Telemetry (6 and ^)"**), where the sign convention is (Phase = PPSEXT – PPSOUT), i.e. a negative value of **Phase** indicates that PPSOUT occurs after PPSEXT by **Phase** ns.

For values of **Phase** outside the range of ±800 ns the TIC reports **Phase** with resolution of 100 ns (10 MHz LN-CSAC). For values of **Phase** within ±800 ns, the TIC reports **Phase** with resolution of 1 ns.

The TIC operates whenever a rising edge appears on PPSEXT. If no PPSEXT is detected for more than 2 seconds, the TIC reports "---" in the telemetry **Phase** field.

Upon initial startup, prior to any synchronization between PPSOUT and PPSEXT, the TIC will report the (unsynchronized) **Phase** on the range of ±0.5 seconds (±500000000 ns).

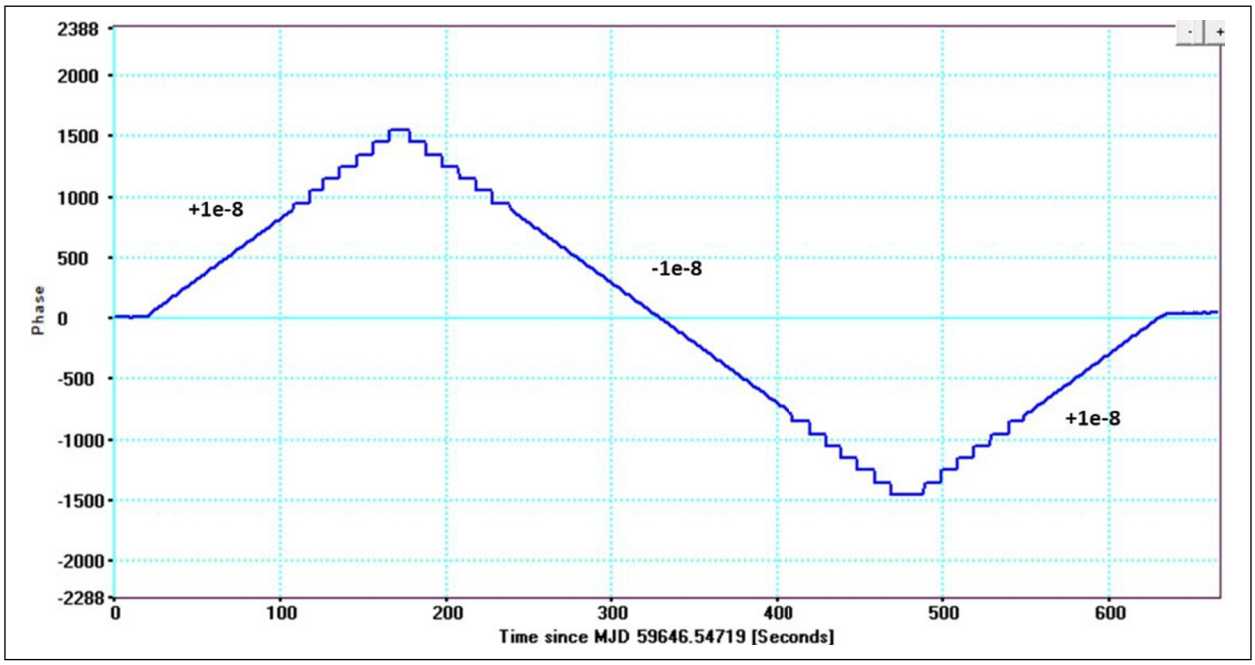


FIGURE 2-6: *Time-interval Counter Performance.*

Figure 2-6 illustrates the transition of the TIC output (Phase telemetry parameter) from fine to coarse measurement as PPSOUT is swept through Phase = 0. For this data, PPSOUT was synchronized to PPSEXT prior to time = 0. Absolute Frequency Steers of ±1E-8 were applied to the LN-CSAC at times 25 sec., 175 sec., and 475 sec.

2.9 1 PPS SYNCHRONIZATION

> **Note:** Synchronization has the effect of a one-time alignment between incoming and outgoing PPS signals. For sustained alignment, the Discipling mode is recommended instead.

The rising edge of the 1 PPS output is synchronous with one rising edge of the RF output (pin 3). The 1 PPS output may be synchronized with a particular cycle of the RF by applying a synchronization pulse to PPSEXT (pin 9). When synchronized, the counters are reset such that the 1 PPS output occurs on the RF rising edge, which is immediately subsequent to the externally applied rising edge. In this way, the LN-CSAC 1 PPS can be synchronized to within one clock cycle (–100 ns to +100 ns) of the external reference.

During the synchronization process, the length of the second immediately following the next rising edge of PPSEXT is adjusted to accomplish synchronization. In the case where PPSEXT appears ahead of PPSOUT by <0.5 seconds, the subsequent epoch may be extended by up to 0.5 seconds. In the case where PPSEXT appears following PPSOUT by <0.5 seconds, the subsequent epoch is shortened by up to 0.5 seconds.

The LN-CSAC provides two modes for 1 PPS synchronization, Manual and Automatic, which are selected through a bit in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**).

> **Note:** The configuration of the mode register is non-volatile (preserved across power cycles).

2.9.1 Manual Synchronization

In Manual Synchronization mode (default), the LN-CSAC ignores any signal present on the PPSEXT (pin 9) until commanded. When a synchronization command is received (see **Section 3.3.4 "1 PPS Synchronization (S)"**), the PPSOUT is synchronized to the next rising edge of PPSEXT to appear on pin 9.

This mode is applicable to configurations where the LN-CSAC is embedded in a system where a 1 PPS reference signal is always present, but not always reliably accurate or stable (such as a GPS receiver). The host microprocessor may command the LN-CSAC to synchronize after it has verified the state-of-health of the 1 PPS reference source (for example, after querying lock state of a GPS receiver).

To manually synchronize the LN-CSAC from Clockstudio, make sure that a valid 1 PPS reference is connected to the 1 PPS reference input and click Sync Now on the 1 PPS Tab (Figure 2-5). The LN-CSAC synchronizes to the next rising edge of PPSEXT detected on pin 9.

2.9.2 Automatic Synchronization

In Automatic Synchronization mode, the LN-CSAC synchronizes PPSOUT to every PPSEXT rising edge that appears on pin 9. In this mode, synchronization may be performed by connecting a reference 1 PPS signal to pin 9 without needing to issue the synchronization command. Automatic synchronization can be enabled/disabled through bit 3 (`0x0008`) in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**).

This mode can be useful, for example, in cases where the host system does not communicate with the LN-CSAC and uses gating of the PPS to indicate validity.

> **Note:** Automatic Synchronization mode and Disciplining mode (see **Section 2.10 "1 PPS Disciplining"**) are mutually exclusive. Enabling either in the mode register disables the other.

To enable Automatic Synchronization from Clockstudio, select the Enable Auto Sync checkbox on the 1 PPS panel and click **Apply** (see Figure 2-5).

2.10 1 PPS DISCIPLINING

In order to achieve higher-resolution synchronization of PPSOUT as well as frequency calibration of the LN-CSAC, the LN-CSAC incorporates a simple proportional-integral (PI) disciplining algorithm.

Based on the measurements of the TIC, the disciplining algorithm adjusts the LN-CSAC's microwave synthesizer through the digital tuning value (steer, observed from the telemetry string). The algorithm steers the frequency so as to simultaneously discipline both the time- and frequency-error of the LN-CSAC to that of the external reference, ultimately achieving accuracies of <5 ns and 1×10^{-12}, respectively. Note that, unlike the `!FA` and `!FD` commands, there is no software limitation upon the disciplined value of steer.

Disciplining can be enabled/disabled through bit 4 (`0x0010`) in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**). The time constant of the steering algorithm is user selectable through the `!D` or `!d` the command (see **Section 3.3.5 "Set 1 PPS Disciplining Time Constant (D)"**).

> **Note:** Both mode settings and time constants set via the `!D` command are non-volatile, that is, preserved across power cycles.

Prior to the onset of steering, the disciplining algorithms first perform an initialization sequence in which the variables of the steering algorithm are reset to defaults and a 1 PPS synchronization operation (see **Section 3.3.4 "1 PPS Synchronization (S)"**) is executed to bring the 1 PPS output within 100 ns of the reference.

Initialization is performed when Disciplining is first enabled in the mode register and, in the case where Disciplining is already enabled after the LN-CSAC achieves frequency lock (BITE = 0, status = 0).

Automatic synchronization, at ±100 ns, is enabled along with Disciplining, in order to maintain PPSOUT – PPSEXT < ±100 ns. This may happen, for example, during the early stages of disciplining, particularly if the initial frequency or phase of PPSOUT is far from that of PPSEXT.

In the event that the 1 PPS reference is removed from pin 9 while Disciplining, the LN-CSAC remains in holdover and preserves the most recent steering value. If the 1 PPS reference subsequently reappears, Disciplining continues where it left off, without reinitializing.

If it is necessary to force re-initialization of the disciplining variables, perhaps because the reference source is deemed untrustworthy and subsequently recovers, this can be accomplished by disabling and re-enabling Disciplining in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**).

In Clockstudio, enabling/disabling Disciplining and setting the discipline time constant are both accomplished on the 1 PPS panel, accessible from the View menu (See Figure 2-5 modify the discipline time constant, enter the new value in the field (60 to 10000 in seconds) and click **Apply Changes**.

> **Note:** Due to the time it takes for the internal loop filter (see Figure 2-1) to adjust the crystal frequency, it is recommended to use longer time constants if the application allows. Shortening the time constant may cause unwanted overshoot or frequency oscillation while disciplining.

The status of Disciplining is indicated by the DiscOK parameter in the telemetry. DiscOK = 0 upon startup. DiscOK = 1 when magnitude of TIC measurement is less than a user-specified threshold (see **Section 3.3.9 "Set Threshold for DiscOK Indicator (m)"**) for two time constants of duration. DiscOK = 2 when in holdover (disciplining enabled but no 1 PPS present).

> **Note:** Automatic Synchronization mode (see **Section 2.9.2 "Automatic Synchronization"**) and Disciplining mode are mutually exclusive. Enabling either in the mode register disables the other.

The DiscOK indicator and DiscOKthreshold have no impact on the behavior or performance of the LN-CSAC, DiscOK is a simple status indicator. In practice, DiscOK is frequently employed for detection of initial acquisition to an external reference. It is less useful for long-term monitoring, where intermediate excursions may exceed the long-term stability objective.

In Clockstudio, the current status of DiscOK and the DiscOKthreshold setting both appear on the 1 PPS tab (See Figure 2-5). To modify DiscOKthreshold, enter the new value (10 to 10000 in nanoseconds) in the field and click **Apply Changes**.

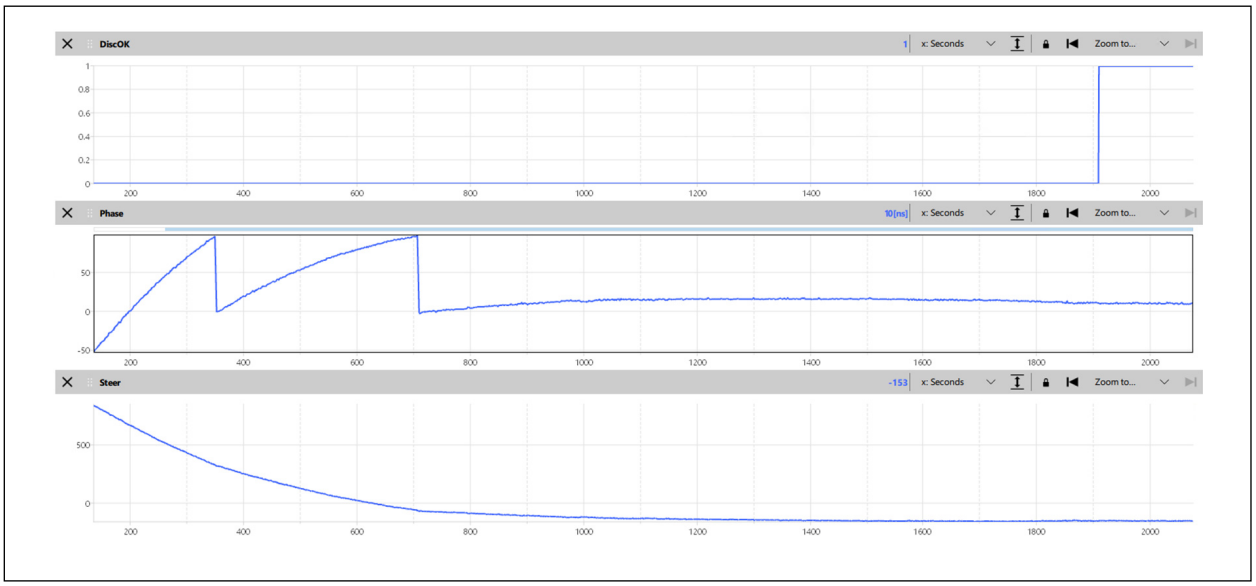


FIGURE 2-7: *PPS Discipling.*

Figure 2-7 shows an example of Disciplining with DisciplineTau = 600 and DiscOKthreshold = 20. As Discipline steered both phase and frequency to 0 with a 600 sec. time constant, Discipline periodically re-synced PPSOUT to PPSEXT in order to maintain **Phase** within ±100 ns. DiscOK transitioned from 0 to 1 when **Phase** < 20 ns for two 600-second time constants.

2.10.1 Cable Length Compensation

The zero point of disciplining can be adjusted to accommodate cable and other instrumentation delays (or advances) which impact the arrival time of the PPSEXT at the LN-CSAC 1 PPS input pin. The compensation value can optionally be stored in the LN-CSAC non-volatile RAM for persistent calibration.

The maximum compensation adjustment is ±25 ns, with resolution of 100 ps. The compensation value is entered into the LN-CSAC as a signed integer in units of 100 ps, where positive sign indicates phase advancement of the input 1 PPS. For example, if there is 10 ns of delay (approximately 2 meters of RG-58 coaxial cable) between the on-time point and the LN-CSAC 1 PPS input then the compensation value would be +100.

> **Note:** Compensation is implemented in the disciplining algorithm, not in the TIC itself. The phase measurement, as reported through telemetry, reports the actual phase measurement, that is, if the LN-CSAC is disciplined with +10 ns of compensation, the phase meter reports –10 ns of phase error.

Compensation is set with the `!DC` command (see **Section 3.3.6 "Set Volatile 1 PPS Disciplining Time Constant (d)"**).

2.11 POWER CONTROL

LN-CSAC time-to-lock (TTL) from cold start is limited by the need to initially warm-up the central core of the physics package which, in turn, is limited by the power supply capacity. TTL may be reduced at the expense of additional power draw during warm-up, based on the user-specified HeaterBoostLimit.

HeaterBoostLimit is a non-volatile parameter that specifies the maximum power provided by the heater control circuit. The units of HeaterBoostLimit are milliwatts, the limits are 50 mW to 250 mW, and the default value is 50 mW. (see **Section 3.3.11 "Set HeaterBoostLimit (.)"**).

With HeaterBoostLimit set to the default value of 50 mW, the LN-CSAC will meet the warm-up power specification on the data sheet. Increasing the value of HeaterBoostLimit will improve lock time at the expense of warm-up power, beyond the data sheet specification.

Note: During startup at low temperatures, continuing to increase HeaterBoostLimit may not significantly decrease TTL. This is due to the physics package being able to achieve nominal temperature much faster than the EMXO which does not have the capability to adjust the warm-up power. If the physics package is at temperature, but the EMXO is not, the clock may need to attempt to lock multiple times before it is achieved.

To configure HeaterBoostLimit using Clockstudio select the Power Management tab shown in Figure 2-8.

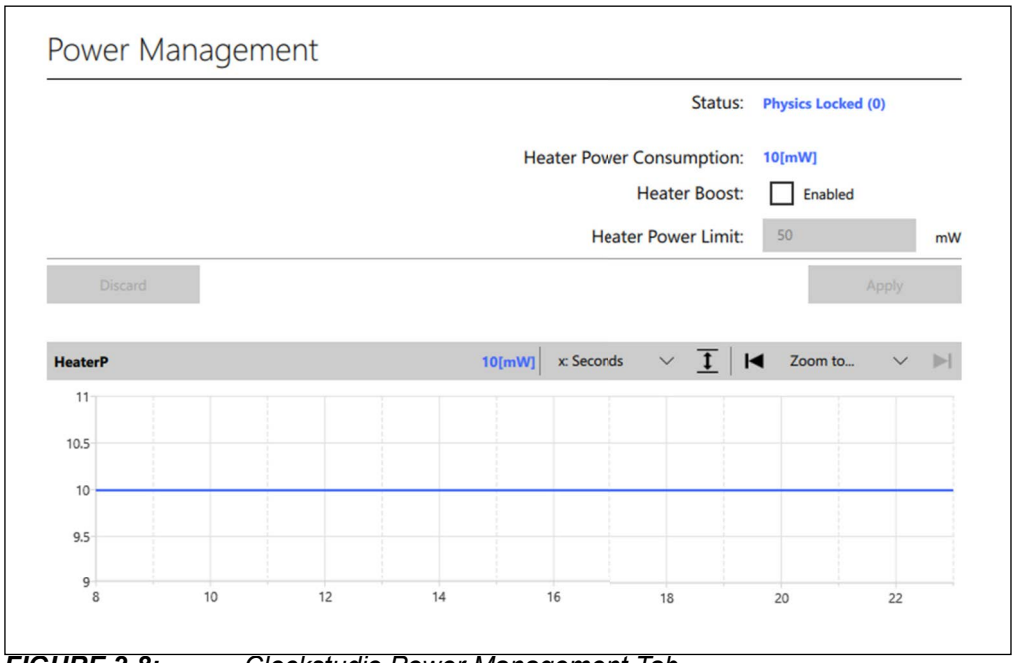


FIGURE 2-8: *Clockstudio Power Management Tab.*

Enter the desired settings and click **Apply Changes** to upload new settings to the LN-CSAC.

2.12 TIME-OF-DAY

The LN-CSAC maintains time-of-day (TOD) as a 32-bit unsigned integer, which is incremented synchronously with the rising edge of the 1 PPS output. Until set otherwise, TOD begins counting from zero when the LN-CSAC is powered on.

TOD is retrieved from the LN-CSAC with the `!T?` command (see **Section 3.3.8 "Time-of-Day (TOD)"**). When the `!T?` command is received, the LN-CSAC waits for the next rising edge of 1 PPS before replying with the TOD of the current epoch, that is, if the command is received during epoch N, then the reply N+1 appears immediately following the next PPSOUT. This strategy provides the host system with minimum ambiguity in interpreting the response.

TOD can be set with the !T command. The !T command includes provision both for setting an absolute number or for a differential (±) adjustment of the present TOD. An example is provided in **Section 3.3.8 "Time-of-Day (TOD)"**. To avoid ambiguity in setting the TOD, it is recommended that the host system wait for PPSOUT prior to transmitting the setting/adjustment immediately thereafter.

The Clockstudio program shows TOD on the Time of Day tab as shown in Figure 2-9.

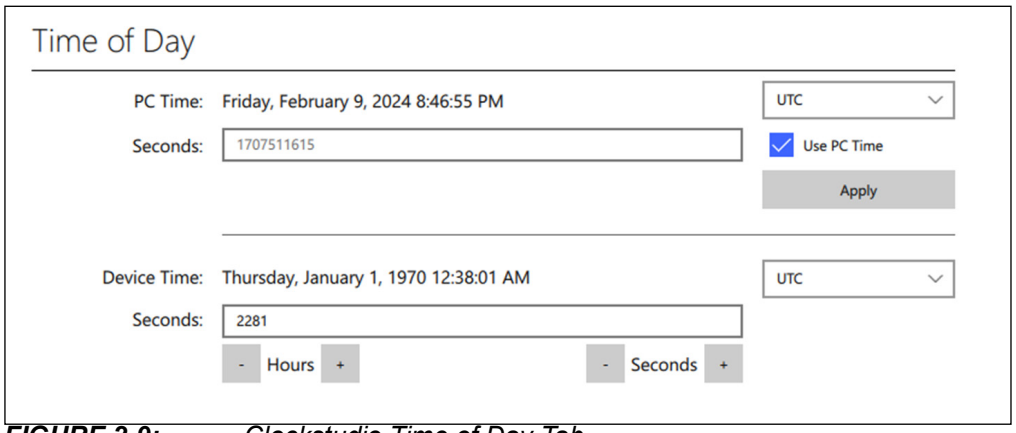


FIGURE 2-9: *Clockstudio Time of Day Tab.*

The raw LN-CSAC TOD values is shown in the lower field of the panel (here 2281). The upper display of the TOD tab realizes the timekeeping convention of the C programming language (in UNIX and Microsoft Windows), which counts time in seconds from midnight January 1, 1970. Upon clicking **Apply**, it sets the LN-CSAC time according to the host PC's TOD counter (either local time or UTC depending on the setting of the pull-down menu above the **Apply** button. The + and – buttons for hours and seconds adjustment will increment or decrement the LN-CSAC TOD by ±3600 or ±1 second respectively.

Chapter 3. Programmer's Reference

Pins 5 and 6 provide a serial interface for communication with the LN-CSAC The protocol is fundamentally similar to RS-232, with the exception that the voltage levels are CMOS (0V to VCC), rather than ±12V.

The serial communication parameters are as follows: (57600-8-N-1)

- 57,600 Baud
- 8 data bits
- No parity
- 1 stop bit
- No flow control

For interfacing with a standard RS-232 controller interface, which requires ±12V logic levels, an external level shifter must be employed, such as the Maxim MAX202 employed on the evaluation board (see **Section 5.4 "Evaluation Board"**).

3.1 OVERVIEW OF TELEMETRY INTERFACE

The LN-CSAC communicates exclusively with printable (non-binary) ASCII characters.

In general, commands are to be preceded by an exclamation point (`!`) and followed by a carriage-return /linefeed `[CRLF]` pair (ASCII 0x0D 0x0A). For convenience and efficiency, most commands also provide a single-character shortcut, which is executed immediately, that is without bracketing by `!` and `[CRLF]`. For example, the single character shortcut `^` is functionally identical to `!^[CRLF]`.

After transmitting `!` but prior to sending `[CRLF]`, a command may be aborted by sending the escape character (ASCII 0x1B).

All commands produce a response from the LN-CSAC, which are human readable, with individual lines ending in `[CRLF]`. If an unsupported or improperly formatted command is received, the LN-CSAC responds with `?[CRLF]`.

3.1.1 Checksum (Error-Checking Option for Telemetry Interface Communications)

For improved communications reliability, an NMEA-style checksum may be enabled through bit 6 (`0x0040`) of the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**). When enabled, the checksum is required for all input commands and is present on all replies from the LN-CSAC.

The checksum is a two-byte ASCII representation (in hexadecimal) of the XOR of all characters in the command between—but not including—the `!` and the `[CRLF]` characters. The checksum is preceded by a `*` character and appended to the command immediately prior to the `[CRLF]`. Because commands including checksum are inherently multi-character, single-character shortcuts are not available when checksum is enabled.

Example (enable Disciplining through mode register):
Command: `!MD*09[CRLF]`
Unit response: `0x0050*4D[CRLF]`

Example (disable checksum through mode register)
Command: `!Mc*2E[CRLF]`
Unit response: `0x0000[CRLF]`

If the checksum is not present or if the checksum value is invalid, then the command is not executed and the LN-CSAC responds with `*[CRLF]`.

Example (malformed checksum):
Command: `!Mc*2D[CRLF]`
Unit response: `*[CRLF]`

Note: Communicating with the LN-CSAC via Clockstudio does not require a checksum. Any commands sent to the LN-CSAC via the Clockstudio console will have a checksum generated automatically. However, if a checksum is provided, the LN-CSAC will respond appropriately.

3.1.2 How to Calculate the Checksum

The checksum value is a two-digit hexadecimal representation of the logical XOR of each character in the command (excluding "`!`" and "`[CRLF]`"). Table 3-1 illustrates computation of the checksum for sending the `!MD[CRLF]` command. In Table 3-1, `M` and `D` are converted to their binary equivalents and the XOR is computed in the bottom row. The corresponding hexadecimal value of that XOR is 9. Hence, the command should be sent as `!MD*09 [CRLF]`.

TABLE 3-1: CHECKSUM CALCULATION EXAMPLE

Checksum Component	ASCII Character	Binary Value	Hex Value
Input Command Characters	M	0100 1101	–
	D	0100 0100	–
Logical XOR	–	0000 1001	9

3.2 COMMAND SUMMARY

Table 3-2 summarizes the LN-CSAC commands.

TABLE 3-2: COMMAND SUMMARY

Shortcut	Description	Command	Reference Section
6	Return telemetry headers as comma-delimited string	!6[CRLF]	**Section 3.3.1 "Telemetry (6 and ^)"**
^	Return telemetry as comma-delimited	!^[CRLF]	**Section 3.3.1 "Telemetry (6 and ^)"**
F	Set/report frequency adjustment	!F?[CRLF]	**Section 3.3.2 "Frequency Adjustment (F)"**
M	Set/report operating mode register bits	!M?[CRLF]	**Section 3.3.3 "Set/Clear Operating Modes (M)"**
S	Sync LN-CSAC 1 PPS to external 1 PPS	!S[CRLF]	**Section 3.3.4 "1 PPS Synchronization (S)"**
D	Set/report 1 PPS disciplining parameters	!D?[CRLF]	**Section 3.3.5 "Set 1 PPS Disciplining Time Constant (D)", Section 3.3.7 "Set 1 PPS Disciplining Cable Length Compensation (DC)"**
d	Set/report volatile 1 PPS disciplining parameters	!d?[CRLF]	**Section 3.3.6 "Set Volatile 1 PPS Disciplining Time Constant (d)"**

TABLE 3-2: COMMAND SUMMARY (CONTINUED)

Shortcut	Description	Command	Reference Section
T	Set/report time-of-day	!T?[CRLF]	**Section 3.3.8 "Time-of-Day (TOD)"**
m	Set/report DiscOKthreshold	!m?[CRLF]	**Section 3.3.9 "Set Threshold for DiscOK Indicator (m)"**
>	Set/report PPSwidth	!>?[CRLF]	**Section 3.3.10 "Set PPSWidth (>)"**
.	Set/report HeaterBoostLimit	!.?[CRLF]	**Section 3.3.11 "Set HeaterBoostLimit (.)"**
p	Report Part Number	!p?[CRLF]	**Section 3.3.12 "Report Part Number (p)"**
?	Help	!?[CRLF]	**Section 3.3.13 "Help (?)"**

3.3 DETAILED COMMAND DESCRIPTIONS

The following are descriptions of the LN-CSAC's commands.

3.3.1 Telemetry (6 and ^)

LN-CSAC supports two commands, !6 and !^, to retrieve the telemetry headers and values, respectively. Both responses are comma-delimited strings, suitable for importing into spreadsheet programs.

Example:
Telemetry headers command: `!6[CRLF]`
Unit response:

```
Status,Alarm,SN,Mode,Con-
trast,LaserI,TCXO,HeatP,Sig,Temp,Steer,
OCXOCurrent,Phase,DiscOK,TOD,LTime,Ver[CRLF]
```

Example:
Telemetry data command: `!^[CRLF]`
Unit response:

```
0,0x0000,2203CS78105,0x0010,24801,1.15,1.254,10.81,1.992,
27.96,-143,0.041,3,1,2921,2803,2.3
```

Not including the 3-character checksum, if enabled, the maximum length of a telemetry string is 129 characters. See Table 3-3 for details.

> **Note:** The single-characters `6` and `^` are shortcuts for `!6[CRLF]` and `!^[CRLF]`, respectively.

Table 3-3 lists the telemetry parameters and their associated header identifiers.

TABLE 3-3: TELEMETRY PARAMETERS (FIRMWARE VERSION 2.3)

Identifier	Description	Comments	String Length
Status	Unit status	See Table 3-4 and Note 1	Up to 2 decimal digits (2 characters)
Alarm	Pending unit alarms	See Table 3-5 and Note 2	"0x" + 4 hexadecimal digits (6 characters max.)
SN	Unit serial number	See Note 3	11 characters
Mode	Mode of operation	See Table 3-6	"0x" + 4 hexadecimal digits (6 characters max.)
Contrast	Indication of signal level	Typically >1000 when locked, and ≈0 when unlocked	16 bits unsigned (5 characters max.)
LaserI	Laser current (mA)	Typically 0.6 mA to 1.3 mA	16 bits unsigned + "." + 2 digits precision (8 characters max.)
TCXO	Tuning voltage (V)	0 VDC to 2.5 VDC tuning range, ≈±10 × 106	16 bits unsigned + "." + 3 digits precision, maximum value is 400.03 (6 characters max.)
HeatP	Physics package heater power (mW)	Typical 6 mW to 20 mW under normal operating conditions and 25°C ambient	16 bits unsigned + "." + 2 digits precision, maximum value is 250.0 (6 characters max.)
Sig	DC signal level (V)	Typical 0.8V to 1.7V under normal operating conditions	16 bits unsigned + "." + 3 digits precision, maximum value is 2.490 (5 characters max.)
Temp	Unit temperature (°C)	Absolute accuracy is ±2°C	16 bits unsigned + "." + 2 digits precision, range is –54.19 to 159.65 (6 characters max.)
Steer	Frequency adjust	In $pp10^{12}$	32 bits signed (11 characters max.)
OCXOCur-rent	Current used by internal EMXO	Typically around 0.040A at 25°C when locked	16 bits unsigned + "." + 3 digits precision, maximum value is 3.300, accuracy is limited to 1%
Phase	Difference between PPSOUT and PPSIN (ns)	Reports "---" if no PPSIN detected for >2 seconds	32 bits signed, range is ±500000000 nano- seconds (10 characters max.)
DiscOK	Discipline status (0-2)	0 = acquiring, 1 = locked, 2 = holdover when disciplining enabled, otherwise ---	"0", "1", "2" or "---" (3 characters max.)
TOD	Time (seconds)	Starts at 0 upon power-up unless set by command	32 bits unsigned (10 characters max.)
LTime	Time since lock (seconds)	Starts at 0 upon lock	31 bits unsigned (10 characters max.)
FWver	Firmware version	M.m where M is major revision and m is minor revision	"2.0" (4 characters, may be longer in future firmware)

Note 1: Status reflects the steps of the clock initialization process. It starts at 8 on boot and decreases to 0 as acquisition proceeds. When Status ≠ 0, BITE = 1. When Status = 0, BITE = 0.

2: Alarms indicate detection of anomalous operating conditions while locked. Alarm is the logical OR of all pending alarms, as shown in Table 3-4. An alarm will not persist if the condition is fixed or if the unit is reset.

3: LN-CSAC serial numbers are of the form YYMMCSXXXXX where YYMM is the year and month of production and XXXXX is the serialized production unit number.

TABLE 3-4: STATUS CODES OF LN-CSAC

Status	Acquisition Stage
8	Initial warm-up
7	Heater equilibration
6	Microwave power acquisition
5	Laser current acquisition
4	Laser power acquisition
3	Microwave frequency acquisition
2	Microwave frequency stabilization
1	Microwave frequency steering
0	Locked

Note: If LN-CSAC returns a status code other than shown in Table 3-4, then it is re-acquiring its set points. In this case, warm-up time takes longer than stated on the data sheet. To avoid this, it is recommended to always allow LN-CSAC to remain powered on for >102 seconds after it acquires LOCK. The minimum amount of time necessary to save LN-CSAC set points to memory is 102 seconds, thus avoiding set-point re-acquisition upon its next power up.

Alarms indicate detection of out-of-range measurements. Alarms may appear momentarily, due to statistical variation of signals, which do not necessarily indicate performance degradation. If any alarm, other than 0x008, persists for longer than 1 second, a reboot is initiated.

TABLE 3-5: ALARM CODES

Alarm	Definition	Alarm Limit
0x0001	Signal contrast low	Contrast <1000
0x0002	Synthesizer tuning at limit	Synthesizer detuned from calibration by >30 kHz or <–15 kHz
0x0004	Temperature bridge unbalanced	Bridge—set-point >±20 mV
0x0008	Heater Boosted (Note 1)	Heater boost is actively boosting
0x0010	DC light level low	(Set-point - DCL) > ±0.1V
0x0020	DC Light level high	DCL - set-point) > ±0.1V
0x0040	Heater voltage low	<30 mV
0x0080	Heater voltage high	>2.48V
0x0100	µW power control low	<20 mV
0x0200	µW power control high	>2.48V
0x0400	TCXO power control low	<0.1V
0x0800	TCXO power control high	>2.4V
0x1000	Laser current low	<0.5 mA
0x2000	Laser current high	>2.3 mA
0x4000	Stack overflow (firmware error)	—

Note 1: Alarm 0x0008 is a non-fatal alarm, provided for information only, and will not initiate a reboot.

Note: The telemetry interface allows users to send commands at a rate up to the baud rate. However, sending commands, specifically the telemetry commands (`6` and `^`) may cause unwanted frequency behavior if sent at a rate faster than 1 Hz. Limit telemetry requests to 1/sec to avoid any unwanted frequency behavior.

3.3.2 Frequency Adjustment (F)

The output frequency of the LN-CSAC may be adjusted (steered) through the communications port. The internal resolution of the fractional frequency correction is approximately 1×10^{-12}. The correction is entered in integer units of $\times 10^{-15}$. The maximum allowed correction is ±20000000 (2×10^{-8}). Corrections may be applied as either Absolute or Relative, depending on the first character following the `!F`, that is `!FA` or `!FD` for absolute or relative (delta) respectively. In the case of absolute steering, the value of the Steer register is replaced with the new value.

In the case of relative (delta) steering, the new value is summed with the existing value in the Steer register, that is, two relative corrections of –10000 result in a total offset of -2×10^{-11}. The current steering value is reported in the steer field of the telemetry in units of $\times 10^{-12}$.

Note that the reported value of Steer reflects all current steering corrections including the User Steer (entered with `!F`) as well as the current steering inputs from Disciplining (see **Section 2.10 "1 PPS Disciplining"**)

The format for the Adjust frequency command is `!FYXXXXX[CRLF]` where `Y` is either `A` or `D` and `XXXXX` is the new correction in $\times 10^{-15}$.

Example: Apply absolute tuning correction of -1.23×10^{-10}:
Command: `!FA-123000[CRLF]`
Unit response: `Steer = -123[CRLF]`

Example: Apply delta tuning correction of -1.23×10^{-10}:
Command: `!FD-123000[CRLF]`
Unit response: `Steer = -246[CRLF]`

Example: Report current value of steer:
Command: `!F?[CRLF]`
Unit response: `Steer = -246[CRLF]`

Note: The single-character `F` is a shortcut for `!F?[CRLF]`.

The contents of the Steer register are volatile. Steer is reset to `0` when power is cycled to the LN-CSAC. In many cases, it is desirable to preserve the steer upon power-down (for example, calibration of the LN-CSAC). This is accomplished by sending a Frequency Latch command to the LN-CSAC, which updates the internal calibration (stored in non-volatile memory) according to the current value of the Steer register and resets Steer to zero. Note that the Latch command is only valid when the LN-CSAC is locked (`Status = 0`).

Example: Latch the current steer value:
Command: `!FL[CRLF]`
Unit response: `Steer Latched [CRLF] Steer = 0[CRLF]`

Note: Once a Latch command is issued, the previously latched value **cannot** be recovered. There is no command to restore "factory defaults".

Note: The frequency steering command (`!F`) is recommended for real-time disciplining of LN-CSACs, but the value should not be latched (`!FL`) on every steer due to the physical limit on the number of times the non-volatile memory may be written before damage. For example, if a `!FL` command is applied to the LN-CSAC at a rate of 1/sec, the LN-CSAC may experience operational failure within a few days of operation

3.3.3 Set/Clear Operating Modes (M)

Operating modes of the LN-CSAC are enabled/disabled by individual bits in the mode register. The `!M` command provides access to set/clear each of the bits independently. The mode register is non-volatile; Settings persist across power cycles.

The unit responds by reporting the current value of the mode register in hexadecimal. Each bit in the mode register is associated with enabling/disabling a particular operating mode. The bit assignments are shown in the following table.

TABLE 3-6: OPERATING MODES OF LN-CSAC

Enable Bit Assignment	Enable Argument to `!M_`	Definition	Disable Argument to `!M_`
`0x0002`	–	Reserved	–
`0x0008`	`S`	1 PPS auto-sync	`s`
`0x0010`	`D`	Discipline	`d`
`0x0040`	`C`	Require checksum	`c`
`0x0080`	–	Reserved	–
–	`?`	Report current settings	–

Example: Enable and then Disable disciplining:

Command: `!MD[CRLF]`
Unit response: `0x0010[CRLF]`

Command: `!Md[CRLF]`
Unit response: `0x0000[CRLF]`

The current value of the mode register is returned in the standard telemetry query (see **Section 3.3.1 "Telemetry (6 and ^)"**) or may be queried independently with the `!M?` command.

Example: Query mode register:
Command: `!M?[CRLF]`
Response: `0x0010[CRLF]`

Note: The single-character M is a shortcut for `!M?[CRLF]`.

Autosync mode and Discipline mode are mutually exclusive. Setting either Autosync or Discipline disables the other.

3.3.4 1 PPS Synchronization (S)

To synchronize the 1 PPS output (pin 10) to an externally applied synchronization input (PPSEXT, pin 9), connect an external 1 PPS signal to pin 9 and send the `!S` command. The rising edge of PPSOUT will synchronize to within ±100 ns of the next rising edge of the applied PPSEXT. If a valid 1 PPS input does not appear at the PPSEXT within 3 seconds, the operation is aborted, and an error is returned.

Example: Synchronize 1 PPS: Command: `!S[CRLF]`
Unit response: `S[CRLF]`
or: `E[CRLF]`

The unit response (`S` or `E`) occurs after either successful synchronization or 3-second timeout, respectively.

Note: The single-character `S` is a shortcut for `!S[CRLF]`.

3.3.5 Set 1 PPS Disciplining Time Constant (D)

The time constant for disciplining to an externally supplied 1 PPS reference source may be selected to provide optimal performance in each application (see **Section 5.1 "The Art of Disciplining"**).

The time constant can range from 60 to 10000 seconds. The 1 PPS disciplining time constant is set with the `!D` command. The format for setting the time constant is `!DX[CRLF]` where `X` is the new time constant in seconds.

Example: Set disciplining time constant to 100 seconds:
Command: `!D100[CRLF]`
Response: `100[CRLF]`

To query the current time constant setting, without modifying the value, use the command `!D?`

Example: Query current disciplining time constant:
Command: `!D?[CRLF]`
Response: `100[CRLF]`

Note: The single-character `D` is a shortcut for `!D?[CRLF]`.

3.3.6 Set Volatile 1 PPS Disciplining Time Constant (d)

A volatile disciplining time constant may be set using the `!d` command. This time constant will be applied but will not persist across power cycling. This command is useful for quickly disciplining the LN-CSAC during initial calibration while keeping a longer time constant in NVRAM in the event of a power cycle. The format for this command is `!dX[CLRF]` where `X` is the volatile time constant in seconds.

Example: Set a temporary time constant to 100 seconds:
Command: `!d100[CRLF]`
Response: `100[CRLF]`

3.3.7 Set 1 PPS Disciplining Cable Length Compensation (DC)

Cable length compensation can be applied to allow for known delay (or advance) in the arrival time of the reference 1 PPS at the LN-CSAC (see **Section 2.10.1 "Cable Length Compensation"**). Cable length compensation is represented as a signed integer in units of 100 ps, with a maximum value of ±250 (25 ns).

The sign of the compensation is such that a positive value reflects known delay in the arrival time of the 1 PPS. For instance, 2 meters of RG-58 cable requires compensation of approximately +10 ns.

The format for setting the cable length compensation value is !DCX[CRLF] where X is the new compensation value.

Example: Set cable length compensation to +15 nanoseconds:
Command: !DC150[CRLF]
Response: 150[CRLF]

To query the current compensation setting, without modifying the value, use the command !DC?

Example: Query current compensation setting:
Command: !DC?[CRLF]
Response: 150[CRLF]

To store the current compensation setting in non-volatile RAM, use the command !DCL

Example: Latch current value of compensation to power-up default:
Command: !DCL[CRLF]
Response: Phase comp latched[CRLF]

3.3.8 Time-of-Day (TOD)

TOD is maintained internally within the LN-CSAC, represented by a single unsigned long integer value, which begins counting up from 0 when the LN-CSAC is powered on. The TOD is synchronized with the 1 PPS output. TOD is routinely transmitted in the telemetry string (see **Section 3.3.1 "Telemetry (6 and ^)"**).

TOD may be set externally with the !T command in this format: !TYXXXX[CRLF] where Y is either A for absolute setting or D for a delta adjustment of TOD and XXXX is either an unsigned integer TOD or a signed integer adjustment to the TOD.

Example: Absolute setting TOD to 1221578499:
Command: !TA1221578499[CRLF]
Unit response: TimeOfDay = 1221578499[CRLF]

Example: Retard TOD by 3600 seconds = 1 hour:
Command: !TD-3600[CRLF]
Unit response: TimeOfDay = 1221574902[CRLF]

The TOD may be reported synchronous with the 1 PPS output:

Example: Retrieve TOD command:
Command: !T?[CRLF]
Unit Response: XXXX[CRLF] where XXXX is the current TOD.

Note: This response does not occur until the next 1 PPS output pulse.

When queried with the !T? command, the first character of TOD appears on the communications port within 20 ms following the rising edge of the next 1 PPS output pulse. Because this necessarily creates a delay of up to a second between sending the !T? command and receiving a response from the LN-CSAC, the host system must allow for an RS-232 receive timeout of at least 1000 ms when anticipating a response to the !T? command. For less critical timing applications, the TOD can be somewhat ambiguously parsed from the standard telemetry string (see **Section 3.3.1 "Telemetry (6 and ^)"**).

Note: The single-character T is a shortcut for !T?[CRLF].

3.3.9 Set Threshold for DiscOK Indicator (m)

The DiscOK field in the telemetry data indicates whether the measured PPS error has remained within ± a user-defined threshold (DiscOKthreshold) for two intervals of the discipline time constant.

To set the DiscOKthreshold, use the command: `!mX[CRLF]` where `X` is the new DiscOKthreshold in nanoseconds. The range of DiscOKthreshold is 1 nanosecond to 109 nanoseconds, with a default of 20 nanoseconds.

Example: Set DiscOKthreshold to ±20 nanoseconds:
Command: `!m20[CRLF]`
Response: `20[CRLF]`

To query the DiscOKthreshold setting, without modifying the values, use the command `!m?`.

Example: Query current DiscOKthreshold setting:
Command: `!m?[CRLF]`
Response: `20[CRLF]`

Note: The single-character `m` is a shortcut for `!m?[CRLF]`.

3.3.10 Set PPSWidth (>)

The pulse width of the LN-CSAC 1 PPS output (pin 10) can be changed by using the `!>` command with this format: `!>X[CRLF]`, where `X` is a multiple of the base pulse width.

The base pulse width for a 10 MHz SA65-LN is 10 µs.

The allowed range of PPSWidth is from 10 µs to 500,000 µs.

Example: Set PPSoutMultiplier to 2x multiple of base Pulse Width:
Command: `!>2[CRLF]`
Response: `PPS Pulse Width = 2 times ~10 usec [CRLF]`

Note: The default pulse width is dependent on the selected frequency option for RF output (pin 12). Reference the data sheet for frequencies other than 10 MHz

Alternatively, you can set the width of PPSOUT signal in microseconds by using the !>u command with this format `!>uX[CLRF]` where `X` is the number of microseconds of the desired pule width. However, the LN-CSAC is still restricted to multiples of the base width. If a pulse width that is not a multiple of the base width is entered, the LN-CSAC will round to the nearest multiple.

Example: Set PPSWidth to 30 µs
Command: `!>u30`
Response: `PPS Pulse Width = 30 usec`

Example: Set PPSWidth to 46 µs
Command: `!>u46`
Response: `PPS Pulse Width = 50 usec`

To query the 1 PPS Out Pulse Width setting, without modifying the values, use the command `!>?`.

Example: Query current 1 PPS Out Pulse Width as a multiple of the base width:
Command: `!>?[CRLF]`
Response: `PPS Pulse Width 4 =times ~100 usec[CRLF]`

Example: Query current 1 PPS Out Pulse Width in µs
Command: `!>u?[CRLF]`
Response: `PPS Pulse Width = 50 usec[CRLF]`

Note: The single-character `>` is a shortcut for `!>?[CRLF]`.

3.3.11 Set HeaterBoostLimit (.)

The maximum power draw of the LN-CSAC Heater control circuits may be controlled by setting the value of HeaterBoostLimit.

The allowed range of HeaterBoostLimit is from 50 to 250. The default value is 50.

Example: Set HeaterBoostLimit to 50 mW:
Command: `!.50[CRLF]`
Response: `Heater power limit (mW): 50 [CRLF]`

Note: The single-character `.` is a shortcut for `!.?[CRLF]`.

3.3.12 Report Part Number (p)

The LN-CSAC part number may be retrieved with the 'p' command. The stored part number is a free-form ASCII string of maximum length 15 bytes, including a NULL terminator.

Example: Retrieve Part Number:
Command: `!p?[CRLF]`
Response: `Part Number: xxx-xxxx-xxx[CRLF]`

3.3.13 Help (?)

The following table lists all available commands in response to the `?` command.

TABLE 3-7: UNIT RESPONSE TO HELP COMMAND (?)

Command	Description
.-	Adjust HeaterBoostLimit
6-	Telemetry Headers
>-	Set 1 PPS out pulse width
?-	SHow this list
^-	Telemetry
d-	Set a temporary, non-stored, 1 PPS Discipline Tau
D-	Set 1 PPS Discipline Tau
F-	Adjust Frequency
m-	Set 1 PPS Discipline Threshold for Phase in ns
M-	Change Mode register
p-	Show part number
S-	Sync 1 PPS
T-	Change/Report Time of Day

Note: The single-character `?` is a shortcut for `!?[CRLF]`.

NOTES:

Chapter 4. Developer's Kit

The LN-CSAC Developer's Kit includes hardware and cabling to facilitate validation of performance, brass-board demonstrations, and software interface development.

Package Contents

The following table lists the contents of the developer's kit (Part #990-00565-000).

TABLE 4-1: CONTENTS OF LN-CSAC DEVELOPER'S KIT

Item	Part Number	Comments
Evaluation board	089-00794-000	See **Section 5.4 "Evaluation Board"**
Power adapter	140-00041-000	5 VDC 5 mm center positive
RS-232 cable	060-00322-000	—

4.1 EVALUATION BOARD OVERVIEW

Detailed schematics of the evaluation board are provided at the end of this document under **Section 5.4 "Evaluation Board"**. The following illustration shows the connections to the evaluation board.

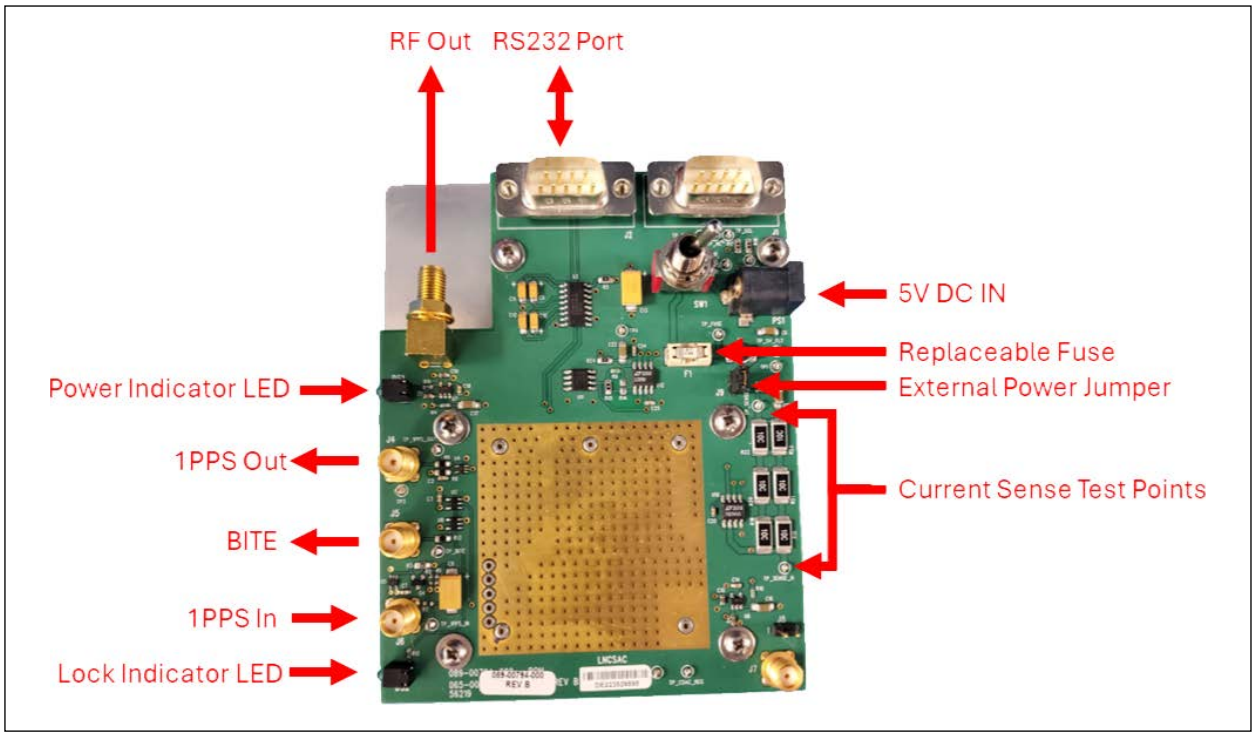


FIGURE 4-1: *Evaluation Board Overview.*

The following items are included in the developer's kit PCB and power supply.

- **RF Output (SMA)**: The LN-CSAC output is an RF, Sine -1.5V to 1.5V waveform. The SMA on the evaluation board is directly connected to RF out (pin 3) on the LN-CSAC.
- **5 VDC Jumper:** The evaluation board provides regulated 3.3VDC to the LN-CSAC. To allow measurement of the LN-CSAC power consumption, a jumper is provided in the VCC connection to the evaluation board. To measure the LN-CSAC current draw, turn off the evaluation board and install a low-impedance current meter in place of the jumper. Observe proper ESD protocols in making this measurement.
- **Replaceable Fuse:** Littelfuse part number 0453 01.5.
- **5 VDC Input:** Input power to the evaluation board is provided on a 5 mm (center positive) coaxial connector (PS1). To avoid damage to the evaluation board, it is highly recommended to use only the power adapter provided by Microchip with the Developer's Kit.
- **RS-232 Connection (DB9M):** The evaluation board provides a level shifter (U3), which converts the LN-CSAC 0VDC to 3.3VDC serial interface to the RS-232 standard ±12V for direct interface with a PC COM port. Connect the evaluation board (J2) to a PC with a standard (non-Null) DB9F-DB9F RS-232 cable. To avoid com- plication, use the proper cable provided by Microchip with the developer's kit.
- **Lock Indicator LED:** Indicates normal operation following initial acquisition of the clock signal. This is the logical complement of the BITE output (LN-CSAC pin 6)
- **BITE (SMA):** This is a buffered output from pin 6 of the LN-CSAC.
- **Power Switch:** Controls power to the evaluation board and to the LN-CSAC.
- **Power LED:** Indicates the state of the power switch.
- **1 PPS Input (SMA):** The 1 PPS input connection to the evaluation board accepts a 1 PPS reference of arbitrary amplitude (logic high: 2V < V_{IN} < 20V) and generates a 0V to 3.3V CMOS pulse to the LN-CSAC. This input is capacitively coupled to the level-shifting circuit on the evaluation board (see Figure 5-3) and therefore the applied pulse width must be <10 ms in duration. By default, the 1 PPS input is high-impedance. When driven with laboratory equipment, it is often essential to install a 50Ω resistor at location R7 on the evaluation board, or to use a 50Ω feed-through terminator at the PPS input, J7. See Figure 4-1 for the location of R7 on the evaluation board.
- **1 PPS Output (SMA):** The 1 PPS output is buffered by a CMOS 0V to 3.3V logic gate on the evaluation board.

CAUTION
To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the LN-CSAC.

4.2 INSTALLING THE LN-CSAC ON THE EVALUATION BOARD

Remove the LN-CSAC and evaluation board from their ESD protective bags only in an ESD-safe environment.

4.3 CABLING

Connect the provided RS-232 cable between the evaluation board and the COM port on the PC. On laptops without an available COM port, a USB-to-RS-232 adapter can be used.

> **Note:** The LN-CSAC pinout is keyed (see Table 1-1) so the LN-CSAC can only be inserted in the proper orientation. Gently insert the LN-CSAC into the socket on the evaluation board.

Make sure the power switch is OFF on the evaluation board, as shown in Figure 4-1. Connect the 5V power adapter between the 5V power input and a wall outlet. (Check labeling on included power supply to ensure compliance with local utility ratings.)

LN-CSAC signal outputs are available from the evaluation board on connectors J3 (RF) and J5 (1 PPS). Connect either (or both) of these to your test equipment (frequency counter, spectrum analyzer, and so on).

4.4 CLOCKSTUDIO SOFTWARE INFORMATION

The Microchip Clockstudio software provides a graphical user interface for monitoring and controlling the LN-CSAC. Clockstudio may also be used for collecting and archiving monitor data from the LN-CSAC. It can be run on any PC that runs Windows 10 or 11 and has at least one available RS-232 (COM) Port.

> **Note:** Multiple LN-CSACs can be monitored from a single PC, provided additional COM ports are available.

The software installation and software user's guide is available for download from the Microchip website: www.micrcohip.com/clockstudio

Upon accepting the default installation options (recommended), Clockstudio is installed in C:\Users\<user>\AppData\Local\Programs\Clockstudio, a startup icon is added to the **Start > Microchip > Clockstudio** menu, and a Clockstudio icon is placed on the desktop.

NOTES:

Chapter 5. Design Guide

The following sections are the design guide for the LN-CSAC.

5.1 THE ART OF DISCIPLINING

Implemented correctly, disciplining can be utilized to calibrate the LN-CSAC frequency in the field, even if a reference source is only occasionally or sporadically available, thereby improving the long-term performance (time and frequency drift) of the LN-CSAC. At the same time, the disciplined LN-CSAC may be used to clean-up the short-term stability of an accurate, but noisy, reference source, such as GPS.

Implemented incorrectly, disciplining may degrade the performance of the LN-CSAC. For example, if the LN-CSAC is disciplined with a short time constant to a source that is noisier than LN-CSAC, such as GPS.

Implementing a successful disciplining strategy involves understanding the noise properties of the LN-CSAC, the reference source, and the time-interval counter (TIC), and selecting the appropriate time constant that makes the best use of the available timing information.

The following graph shows typical instability (Allan Deviation) of the LN-CSAC (in blue), along with the noise floor of its phase meter (in red). Also shown are the instabilities of typical reference sources, GPS (in purple) and a high-performance cesium beam frequency standard (in green).

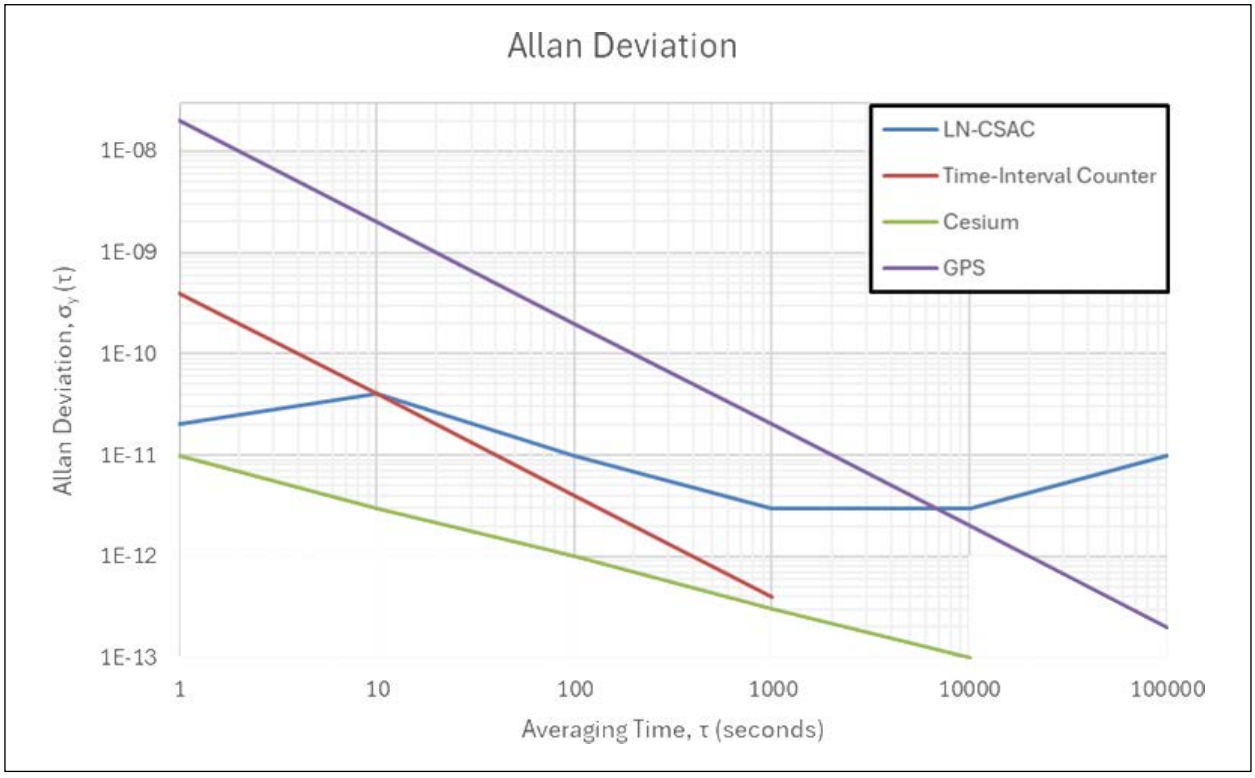


FIGURE 5-1: *Frequency Stability (Allan Deviation) versus Averaging Time.*

When disciplining, the stability of the output of the LN-CSAC (combined clock) at any averaging time reflects the noise properties of the dominant (most noisy) source. For example, if disciplining the LN-CSAC to a GPS source, which is noisier than the LN-CSAC for averaging times $\tau < 5000$ seconds, the disciplining time constant should be set to $\tau > 5000$ seconds so that the (superior) LN-CSAC stability dominates for $\tau < 5000$ seconds and the (superior) GPS stability dominates for $\tau > 5000$ seconds.

On the other hand, consider the case where the LN-CSAC is disciplined to a high-performance cesium clock, which is more stable than the LN-CSAC on all time scales. The noise is dominated by the TIC for $\tau < 10$ seconds and by the LN-CSAC for $\tau > 10$ seconds. In this case, the disciplining time constant may be lowered to 60 seconds (minimum tau for LN-CSAC) for optimal performance.

The following graph shows an example of an LN-CSAC, which is disciplined to a superior reference (in this case a high-performance Rubidium clock) with a time constant of 60 seconds. For this measurement, the LN-CSAC was deliberately mis-tuned in both frequency (y) and phase (φ) prior to the measurement, by $y = 10 \times 10^{-10}$ and φ = ~55 ns.

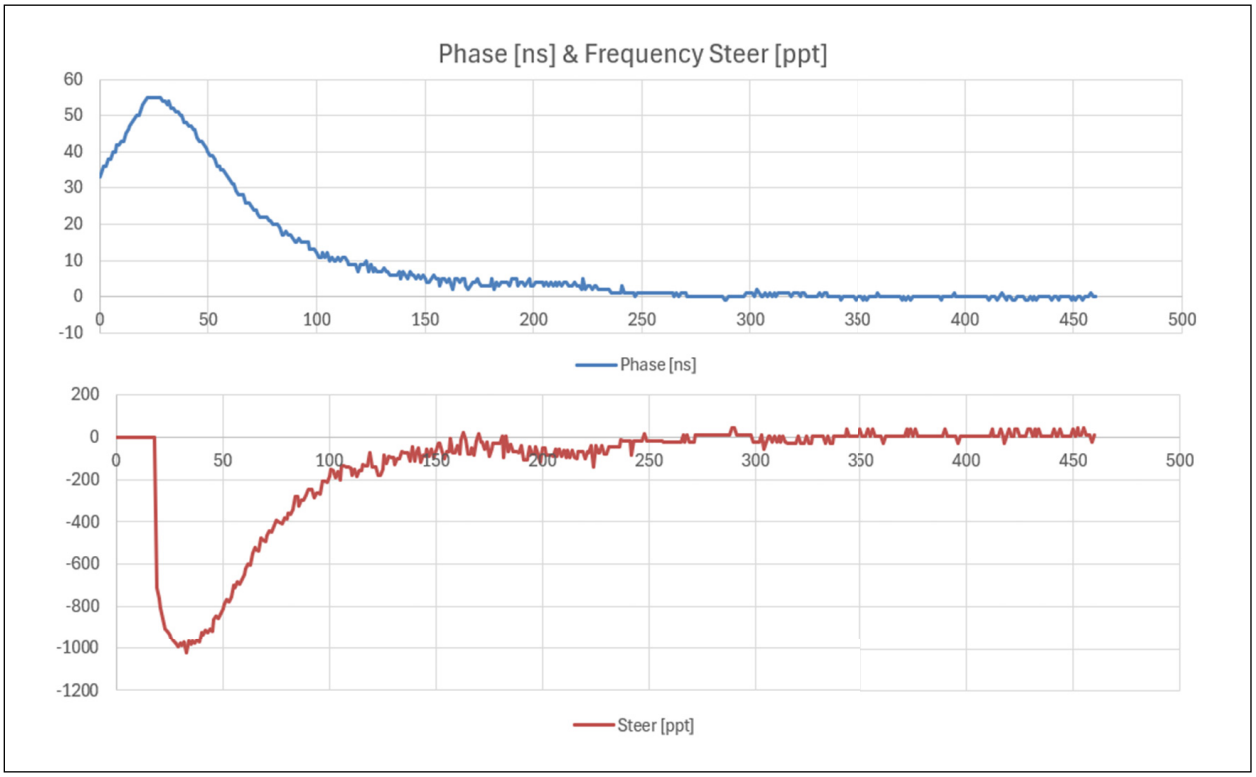


FIGURE 5-2: *CSAC Disciplined to a Superior Reference.*

In the previous graph, when disciplining was enabled, at t = 20 seconds, the steering algorithm immediately inserted a frequency offset of -9×10^{-9}, to steer out the 55 ns time error with 60 second time constant. The steering gradually reduces as the phase approaches zero such that both frequency and time error are corrected to within 1/e of their initial values at one time constant (60 seconds) and $1/e^4$ within two time constants (120 seconds). After five to six time constants (≈ 300 seconds), frequency and time error are corrected to within $\pm 5.5 \times 10^{-13}$ and ±5.5 ns, respectively.

5.2 HEAT SINK

The LN-CSAC does not require a heat sink because it consumes low power and therefore produces little heat. Furthermore, the external parts of LN-CSAC are mu-metal (80% nickel), which is a poor thermal conductor (1/5 that of aluminum). There is no useful thermal path from the inside components to the baseplate or the cover.

5.3 NOTES ON SOLDERING

For initial testing and evaluation, it is recommended that the pins must not be modified or soldered to a PCB. The recommended socket for PCB attachment is Mill Max P/N 0332-0-43-80-18-27-10-0.

After evaluation, the pins can be hand soldered to a PCB using 63/37 tin/lead solder with a maximum soldering tip temperature of 329°C (625°F).

Hand soldering is a necessary requirement for LN-CSAC, and solder re-flow is not recommended because the LN-CSAC cannot go above storage temperature (it is likely to damage it).

The lead material is 52 Alloy with a plating of 50 µin gold minimum (ASTM 8488-01) over 100 µin nickel (QQ-N-290).

5.4 EVALUATION BOARD

The following illustration shows the reference schematic for the evaluation board

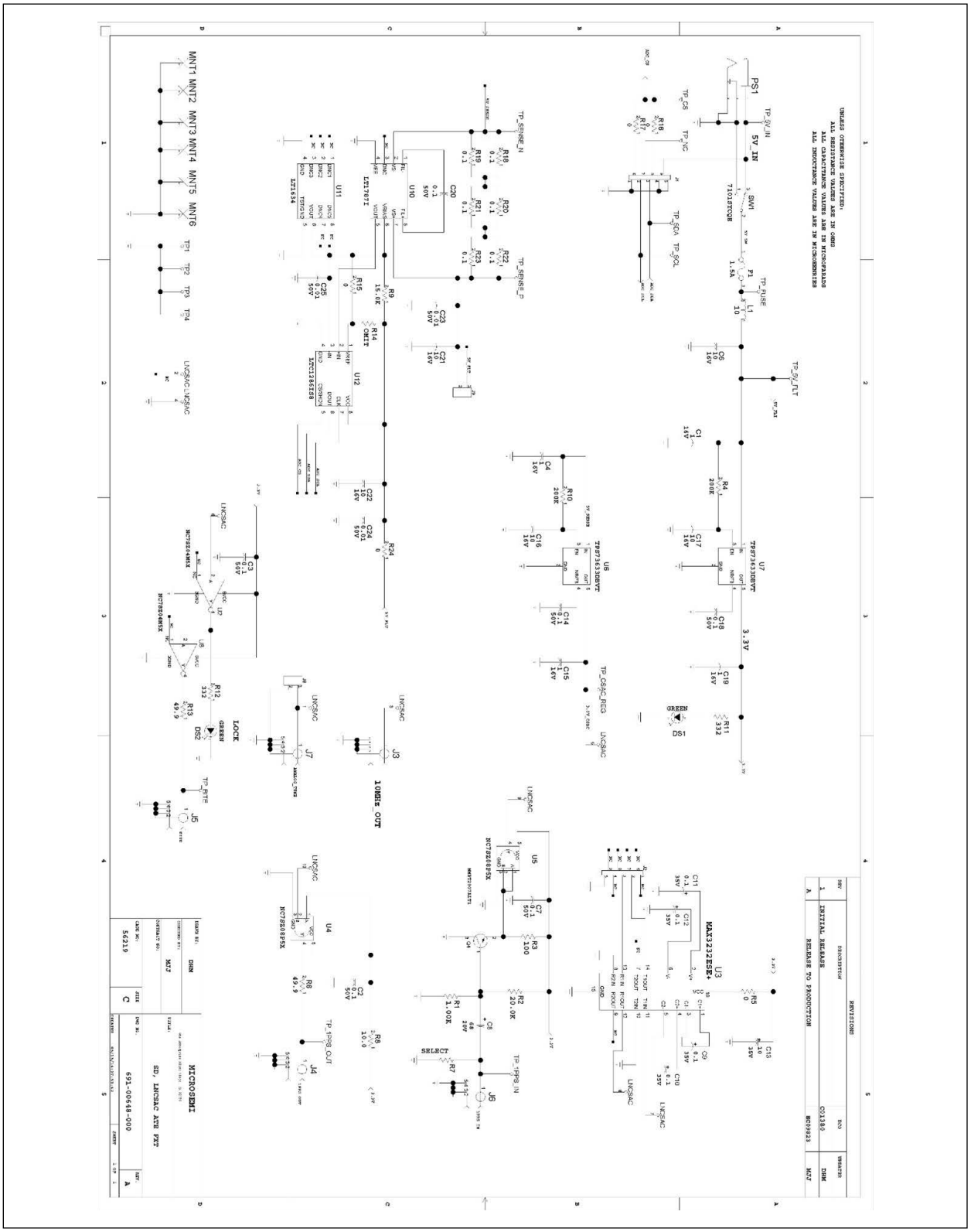


FIGURE 5-3: *Reference Schematic for Evaluation Board.*

5.4.1 Notes on the Evaluation Board

The 1 PPS input on the evaluation board is capacitively coupled to the LN-CSAC through a common collector transistor stage and a UHS inverter. This is to protect the LN-CSAC in the evaluation environment, from 1 PPS signals >5V.

The 10 MHz output from the LN-CSAC is directly connected to J3 on the evaluation board.

5.5 WRITES TO NVRAM

As a best practice, and to maximize the lifetime of the memory devices, it is advisable to restrict the number of NVRAM writes as necessary.

The following are the scenarios of a write to NVRAM:

- Issuing a Frequency Latch command (format `!FL`) causes an NVRAM write.
- Issuing a PPS cable length compensation latch command (format `!DCL`) causes an NVRAM write.
- Issuing a PPS disciplining tau set command that changes discipline tau (format `!Dn` where `n` is a decimal number) causes an NVRAM write.
- Issuing a mode command that changes mode register (format `!Mx` where `x` is an alphabetical character) in list below causes an NVRAM write:
  - Communications Checksum on/off (`!MC` vs `!Mc`)
  - PPS auto-sync on/off (`!MS` vs `!Ms`)
  - PPS disciplining on/off (`!MD` vs `!Md`)
- Issuing a HeaterBoostLimit set command that changes HeaterBoostLimit (format `!.x`, where `x` is a decimal number) causes an NVRAM write.
- Every auto-reset (status 0->8) due to alarm where status reverts from lock state, firmware does an automatic NVRAM write.
- Periodically every 30 days in clock-lock state, firmware does an automatic NVRAM write.
- Issuing a PPS pulse width set command that changes pulse width (format `!>N` where `N` is a decimal number) will cause an NVRAM write.
- Issuing a DiscOKthreshold command that changes DiscOKthreshold (format `!mN` where `N` is a decimal number) will cause an NVRAM write.
- Lock set points are saved after each acquisition of a lock state. This write occurs ~102 seconds after Lock is achieved.

NOTES: