

Parallel Connection of IGBT and MOSFET Power Modules.

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Introduction

Several dice are usually connected in parallel within high current power modules. IGBT and MOSFET modules must then be paralleled to increase current capability sufficient for systems with several hundreds of kW of output power.

Transistors and associated freewheeling diodes are paralleled together, both within and outside power packages, and a lot of precautions must be adopted in order to get equal contribution of each device. Perfect symmetry must be achieved in order to get ideal static and dynamic current sharing starting from the module design to the final assembly.

Current asymmetry can be caused by component parameters or by structural conditions (due to the parasitic elements of the circuit connecting the different components together).

1- Problem of current sharing

1-1 Saturation voltage

The saturation voltage of modules connected together is the same for all of them, and current sharing between each device is strongly dependant on their relative output characteristics. Assuming junction temperature is the same for each device, a higher share of current is carried by the module with lowest on-state voltage at a given current. Taking a simple example of two parallel IGBTs, a difference of output characteristic between the two devices provides a difference of static current ΔI_{DC} , as shown on Fig.1, where I_{C1} and I_{C2} are the currents through each IGBT and their sum is the load current.

Output Characteristics ($V_{GE1}=V_{GE2}=15V$)

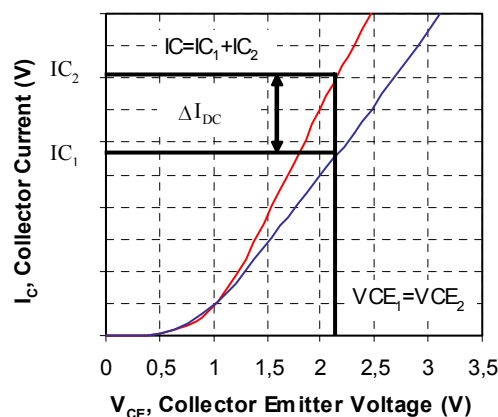


Fig.1 $I_C=f(V_{CE})$ output characteristics

A device with higher current has higher power dissipation, and consequently its junction temperature tends to increase higher than that of other parallel devices. MOSFETs, NPT and Field stop IGBTs have a positive saturation voltage temperature coefficient. As junction temperature increases, on-state voltage at a given current increases. Conversely, at a given on-state voltage, current decreases as temperature increases. This feedback between temperature and current share ensures thermal stability of parallel devices, although it does not force even current sharing.

For PT IGBTs, the $V_{CE(sat)}$ temperature coefficient is negative and transitions to positive only above a crossover point in current. In most cases the crossover point is in the range of the IGBT current rating or a little higher. A negative $V_{CE(sat)}$ temperature coefficient results in thermal instability when paralleling. If devices do not have good heat sharing, then the hottest device

takes a higher share of current, creating more heat and consequently more current hogging, potentially resulting in thermal runaway. Therefore particular care must be taken when PT IGBT devices are connected in parallel and operated below the crossover point where $V_{CE(sat)}$ temperature coefficient is negative. Good heat sharing (a common heat sink and minimized thermal resistance between devices) causes the hottest device to heat its neighbours, thus increasing their current share too, greatly reducing the tendency for thermal runaway. Sorting by $V_{CE(on)}$ at a fixed current may be required for PT IGBT modules.

1-2 Transfer characteristics $I_C=f(V_{GE}, T_j)$; $I_D=f(V_{GS}, T_j)$

Any difference in static current sharing will make difference in switching losses, these being directly proportional to the switched current. Any differences in the threshold voltages, which are amplified with temperature variations, will further increase static and dynamic asymmetries of the switched currents.

Dynamic current asymmetries inevitably lead to higher switching losses in the devices that conduct more current during switching. Taking again the example of two devices in parallel, any difference in threshold voltage leads to a difference in switch current amplitude ΔI_{SW} as shown on Fig.2.

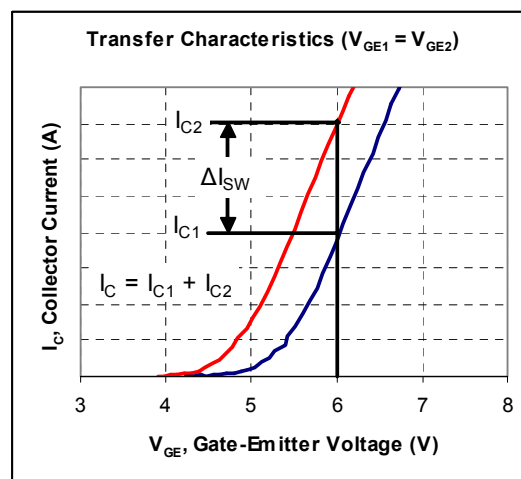


Fig.2 $I_C=f(V_{GE})$ transfer characteristic

Differences in switching delay times, $t_{d(on)}$ and $t_{d(off)}$ and in t_{on} and t_{off} switching times contribute also to switching loss imbalance between paralleled devices.

1-3 Loop inductance in the power circuit

Loop inductance of the circuit is a key factor to ensure good dynamic paralleling of power devices. Perfectly symmetrical layout of the power commutation circuit must be achieved. The loop inductance in each power circuit must be as short as possible to minimize voltage overshoot at device turn-off.

1-4 Driver output impedance

Noise emanating from the drain/collector couples to the gate through the reverse transfer capacitance. Since the gate drive circuit itself is very low impedance, not much noise can couple into it directly unless it has a large loop area or there is capacitive coupling to a noise source. Feedback between the gate and drain/collector can result in oscillation, especially cross-coupled feedback between paralleled devices. Imbalance in gate drive impedance can result in asymmetrical switching. Individual gate resistors provide damping, which eliminates or at least reduces oscillation.

Individual gate resistors also somewhat isolate the gates of each device from each other, reducing cross-coupling. In addition to gate resistors, ferrite beads added to each gate wire can be very effective at preventing oscillation.

2- Gate drive recommendations

2-1 Electrical diagram

The electrical diagram of power modules connected in parallel is shown on fig.3. It is best to use a common gate driver for all paralleled modules because gate signals are synchronized (uniform propagation delay for each gate). Individual gate drivers for each module could cause some variation in turn-on and turn off-delay times, causing asymmetric switching behaviour. This increases even more the switching losses and potential risks of module failures. It is however possible to parallel power modules and their associated drivers if the differences in driver delay times are negligible.

It is imperative that parallel modules have the same part number, and it is also highly recommended to use power modules from the same production lot. This ensures that all devices exhibit the least variation in their characteristics.

It is common practice to implement resistors on the driver to control both turn-on and turn-off behaviour of the power devices. These resistors can be distributed among the modules connected in parallel as gate resistors R_G and return gate resistors R_E as shown in Fig 3. These resistors dampen the parasitic oscillations that might be induced by cross-coupled gate feedback between devices. In addition, each module's individual gate / source or gate / emitter is driven in differential mode that compensates negative effects of possible differences in transfer characteristics between modules. The R_E value should be lower than R_G (In practice $R_E \approx R_G/3$).

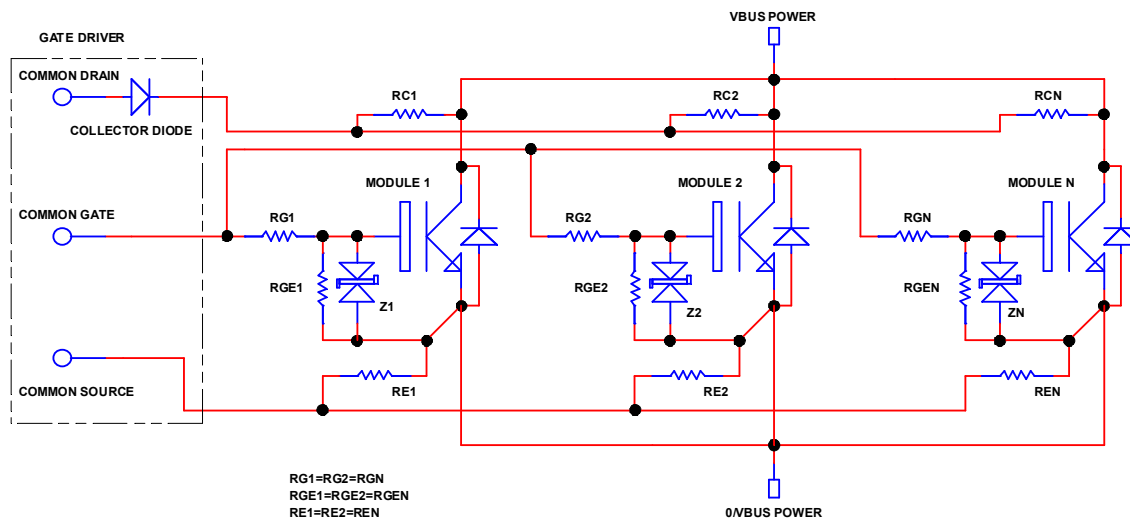


Fig.3 Driver with common output

If the driver offers dual outputs, gate resistors can be doubled into $R_{G(on)}$ and $R_{G(off)}$ resistors to independently control turn-on and turn-off switching speed, as shown in Fig.4. Main common resistors may be placed on the driver if the distributed gate resistors per module are not sufficient to

limit voltage overshoot during switching. It is also recommended to place a resistor (R_{GE} equal to $5k\Omega$ to $10k\Omega$) as well as a bidirectional tranzorb in parallel with gate and emitter of each module.

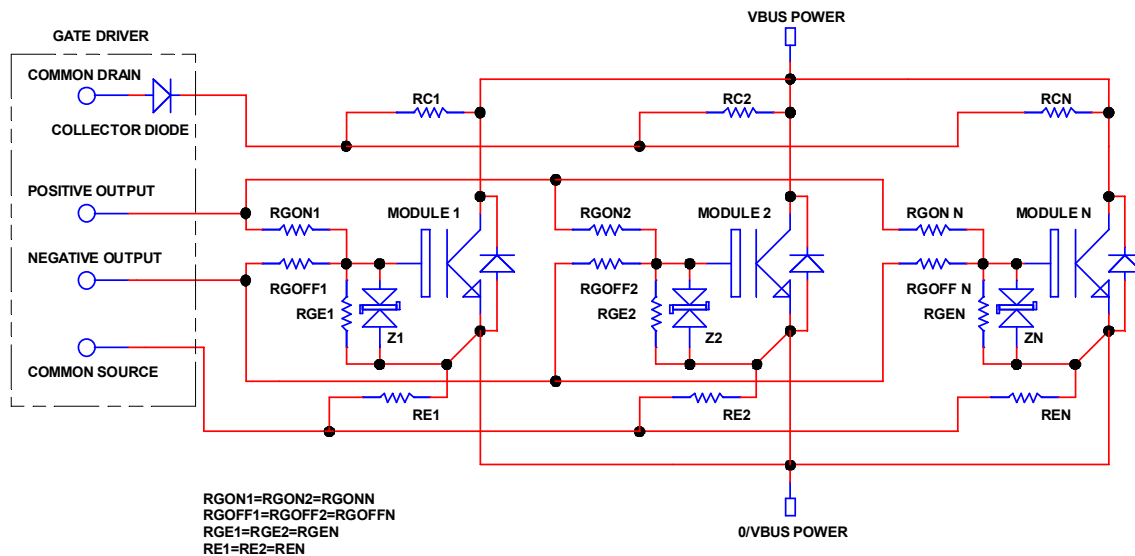


Fig.4 Driver with dual (positive and negative) outputs

2-2 Layout considerations

It is imperative to adopt a perfectly symmetrical layout of the power circuit, and as symmetrical as possible for the gate drive circuit, with minimum loop area and inductance for each.

2-3 Electrical ratings of power modules connected in parallel

All modules connected in parallel must be mounted on the same heat sink to achieve the best possible thermal coupling. It is best to space the modules apart over the whole surface of the heat sink to avoid creating hot spots on the heat sink and to minimize heat density.

Even if all steps described above are followed to optimize the paralleling of power modules, the current rating of the assembly must not exceed 80% to 90% of the total current capability of the modules to compensate for unavoidable parameter variations between modules.

3- Parallel connection of SP3, SP4 and SP6 modules

3-1 SP3 and SP4 modules

SP3 and SP4 modules have very symmetrical designs with very short connections both for power and control terminals. Parasitic inductances of connections are very low, facilitating a parallel module layout with minimum loop inductances.

3-2 SP6 phase leg modules

An industry standard module with 62mm x 108mm package dimensions can easily be connected in parallel, but the pinout location prevents the use of these modules at high frequency. The main reason is that gate and source terminals are located on one side of the module, making the control signal connections to the bottom switch quite long. Control signal loop cannot be symmetrical between top and bottom switches, and the bottom gate-source signal loop would need to be reduced to decrease inductance.

APT Europe has developed full bridge modules featuring perfect symmetry between each switch. In this way the two legs of the bridge can be paralleled to almost double the current capability. This process can be extended to modules in parallel to further increase the current without particularly degrading the performance at high frequency. The SP6 package modules from APT are pin-to-pin compatible with the 62mm x 108mm standard modules available on the market and offer a higher performance alternative.

3-3 Paralleling of SP6 full bridge module.

As the size of a module becomes significant, each switch is made of several cells connected in parallel. Each cell may itself incorporate several dice in parallel.

The SP6 full bridge configuration provides gate and source terminals on each side of the module as shown on Fig.5.

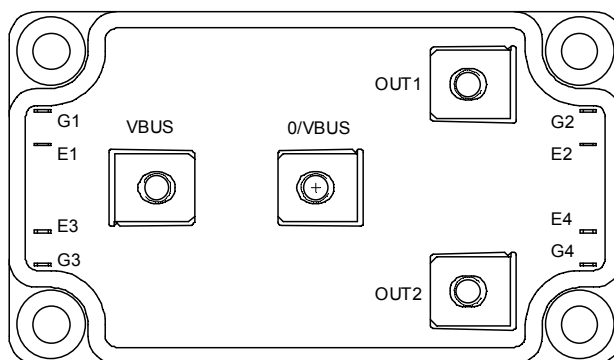


Fig.5 Pin out location of SP6 full bridge module

The connection length is absolutely the same for each cell making a switch, both for top and bottom switches, and remains very short. This fulfils the requirement for very reproducible and minimum control signal loop inductance. Applying distributed gate and source resistors for each cell offers perfect driving for almost an infinite number of modules connected in parallel. This allows reaching very high operating frequencies, in the range of several hundreds

of kHz, using MOSFET devices for hard switching or IGBTs for soft switching.

The low 17mm module height further reduces parasitic inductance in the power circuit loop, facilitating even higher frequency operation with minimum voltage overshoot at switch turn-off.

Fig.6 describes the electrical diagram of the control signal loop for each cell of both top and bottom switches.

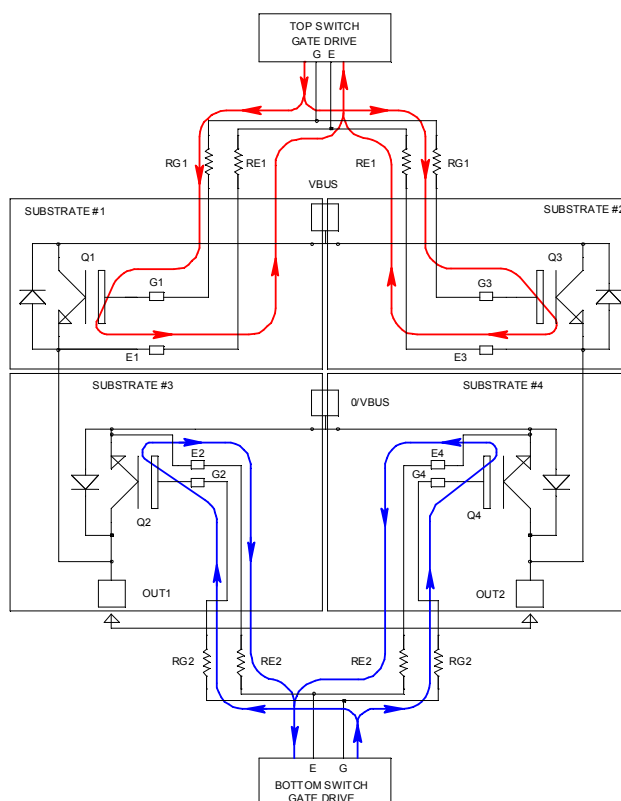
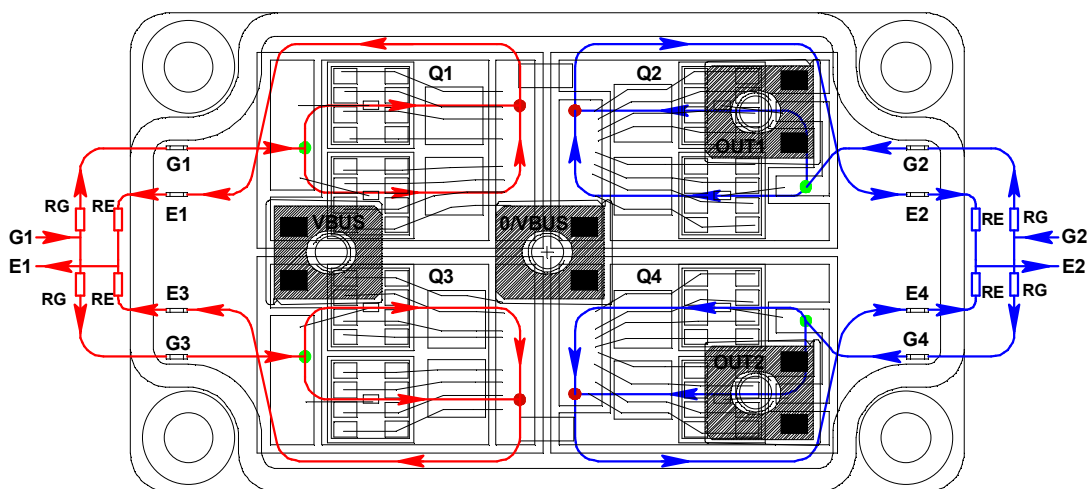


Fig.6 Control signal loop of the SP6 Full bridge module configured as a phase leg.

The control loop and impedance seen by the gate driver is absolutely identical for each group of dice. The same principle can be extended to many modules in parallel.

Fig.7 gives an example of an IGBT module layout and shows again the very symmetrical design, making control signal loops very short and identical.



Green dots: gate connections

Red dots: Source connections

Fig.7 Parallel connection of the two legs of the full bridge

4- Mechanical assembly

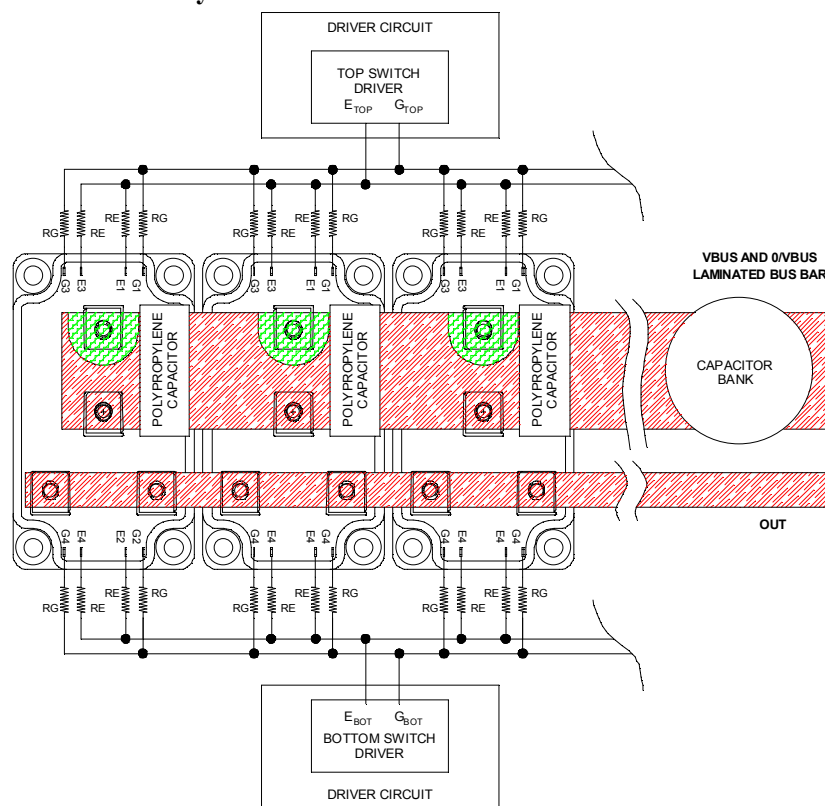


Fig.8 shows the mechanical assembly of modules connected in parallel to achieve a high current phase leg.

Impedance between power source and modules must be as low as possible. It is highly recommended to connect VBUS and 0/VBUS of the modules via laminated bus bars offering very good coupling capacitance and minimum parasitic inductance as shown on Fig. 8.

In any case the parasitic inductance cannot be zero, and fast type capacitors such as polypropylene or even better, ceramic type, must be distributed for each module as close as possible to the power terminals.

It is also important to ensure good current sharing on the power output. If it is not possible to make a very symmetrical layout, it may make sense to insert small inductors with higher impedance than the IGBT between each module output and the load to ensure a good dynamic decoupling of each module output (fig. 9). This should not degrade the performance of the circuit given that in most cases, the load is more or less inductive. The series inductors will tend to decrease the dv/dt applied to the load which may be helpful in some applications.

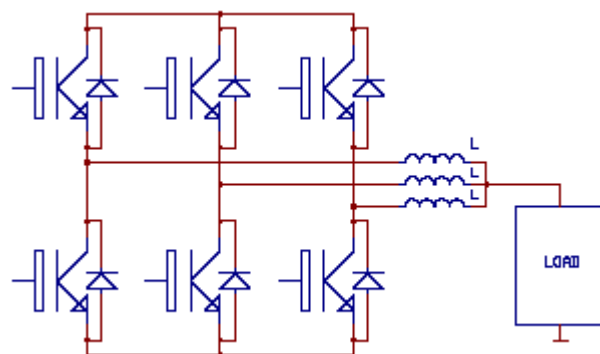


Fig.9 Output current dynamic sharing with series inductors

Conclusion

Paralleling of power modules with good current sharing can be achieved by following some important guidelines. The above recommendations apply both to IGBT and MOSFET modules. However, greater care and maximum precautions are necessary as the number of paralleled modules increases, operating frequencies become very high, and power devices to be paralleled exhibit faster and faster switching times.

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