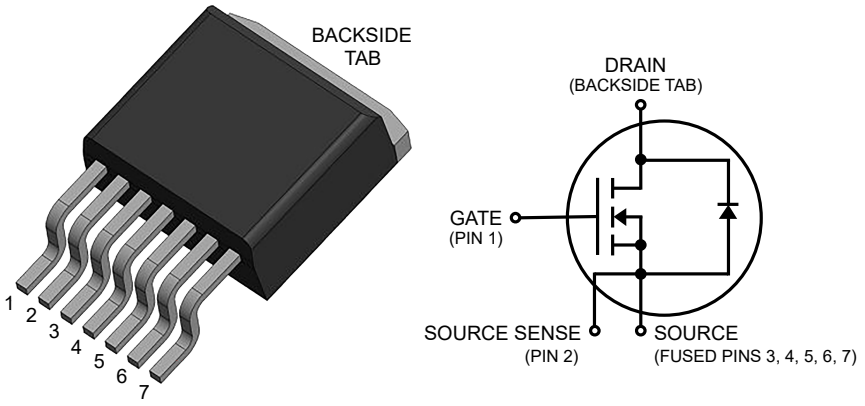
1200V, 80 mΩ N-Channel mSiC™ MOSFET

MSC080SMA120SD

Product Overview

1200V, 80 mΩ typical at V_{GS} = 20V, 90 mΩ typical at V_{GS} = 18V, Silicon Carbide (SiC) N-Channel MOSFET, TO-263 7-lead XL with a source sense.



Features

- AEC-Q101 qualified option available
- Low capacitances and low gate charge
- Fast switching speed due to low internal gate resistance (ESR)
- Stable operation at high junction temperature, $T_{J(max)}$ = 175 °C
- Fast and reliable body diode
- Superior avalanche ruggedness
- RoHS compliant

Benefits

- High efficiency to enable lighter and more compact system
- Simple to drive and easy to parallel
- Improved thermal capabilities and lower switching losses
- Eliminates the need for external freewheeling diode
- Lower system cost of ownership

Applications

- Photovoltaic (PV) inverter, converter, and industrial motor drives
- Smart grid transmission and distribution
- Induction heating and welding
- Hybrid Electric Vehicle (HEV) powertrain and Electric Vehicle (EV) charger
- Power supply and distribution

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1. Device Specifications

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain source voltage	1200	V
I_D	Continuous drain current at T_C = 25 °C	43	A
	Continuous drain current at T_C = 100 °C	30	
I_{DM}	Pulsed drain current[1]	111	
V_{GS}	Gate-source voltage	23 to –10	V
	Transient gate-source voltage	25 to –12	
P_D	Total power dissipation at T_C = 25 °C	268	W
	Linear derating factor	1.7	W/°C

Note:

1. Repetitive rating: pulse width and case temperature are limited by the maximum junction temperature.

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic/Test Conditions	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance	—	0.43	0.56	°C/W
T_J	Operating junction temperature	–55	—	175	°C
T_{STG}	Storage temperature	–55	—	175	
—	Reflow temperature	—	—	260	°C
Wt	Package weight	—	1.6	—	g

ESD practices should comply with JESD-625.

1.2 Electrical Performance

The following table shows the static characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0V, I_D = 100 µA	1200	—	—	V
$R_{DS(on)}$	Drain-source on resistance[1]	V_{GS} = 20V, I_D = 15A	—	80	100	mΩ
		V_{GS} = 18V, I_D = 15A	—	90	—	
$V_{GS(th)}$	Gate-source threshold voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.9	3.0	5.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1200V, V_{GS} = 0V	—	0.2	30	µA
		V_{DS} = 1200V, V_{GS} = 0V, T_J = 175 °C	—	2	—	
I_{GSS}	Gate-source leakage current	V_{GS} = 20V/–10V	—	—	±100	nA

Note:

1. Pulse test: pulse width < 380 µs, duty cycle < 2%.

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The following table shows the dynamic characteristics of this device. T_J = 25 °C unless otherwise specified. The dynamic characteristics are characterized, not 100% tested, at the recommended operating V_{GS} = 20V/–5V.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0V V_{DD} = 1000V V_{AC} = 25 mV ƒ = 200 kHz	—	1031	—	pF
C_{rss}	Reverse transfer capacitance		—	6	—	
C_{oss}	Output capacitance		—	92	—	
Q_G	Total gate charge	V_{GS} = –5V/20V V_{DD} = 800V I_D = 15A	—	64	—	nC
Q_{GS}	Gate-source charge		—	12	—	
Q_{GD}	Gate-drain charge		—	19	—	
$t_{d(on)}$	Turn-on delay time	V_{DD} = 850V V_{GS} = –5V/20V I_D = 20A $R_{G(ext)}$ = 8Ω Freewheeling diode = MSC080SMA120SD (V_{GS} = –5V); reference Figure 1-19	—	13	—	ns
t_r	Voltage rise time		—	10	—	
$t_{d(off)}$	Turn-off delay time		—	22	—	
t_f	Voltage fall time		—	12	—	
E_{on}	Turn-on switching energy		—	469	—	µJ
E_{off}	Turn-off switching energy		—	51	—	
ESR	Gate equivalent series resistance	f = 1 MHz, 25 mV, drain short	—	1.9	—	Ω
SCWT	Short circuit withstand time	V_{DS} = 960V, V_{GS} = 20V	—	3.0	—	µs
E_{AS}	Avalanche energy, single pulse	I_D = 15A	—	1300	—	mJ

The following table shows the body diode characteristics of this device. T_J = 25 °C unless otherwise specified. The body diode reverse recovery is characterized, not 100% tested.

Table 1-5. Body Diode Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	I_{SD} = 15A, V_{GS} = 0V	—	3.7	—	V
		I_{SD} = 15A, V_{GS} = –5V	—	3.9	5.0	
t_{rr}	Reverse recovery time	I_{SD} = 20A, V_{GS} = –5V, Drive R_G = 8Ω, V_{DD} = 850V, dI/dt = –10100 A/µs	—	12	—	ns
Q_{rr}	Reverse recovery charge		—	416	—	nC
I_{RRM}	Reverse recovery current		—	59	—	A

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1.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Drain Current vs. V_{DS} at T_J

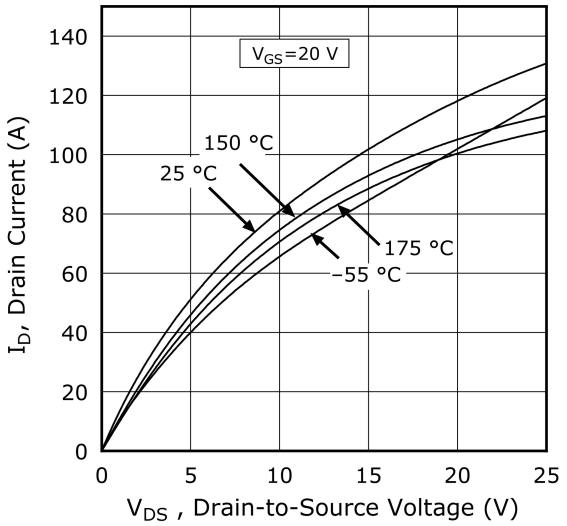

Figure 1-2. Drain Current vs. V_{DS} at V_{GS}

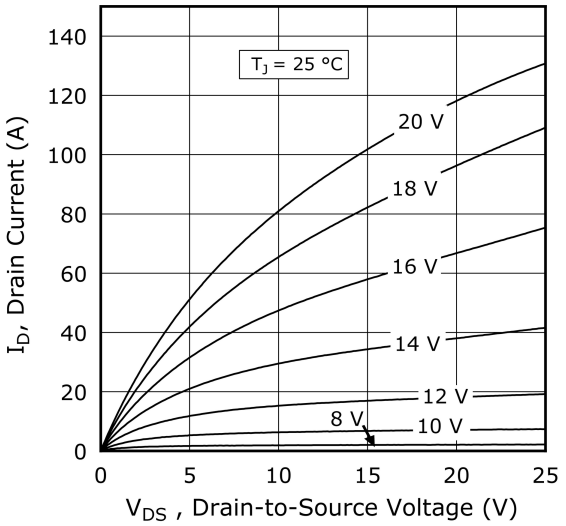

Figure 1-3. Drain Current vs. V_{DS} at V_{GS}

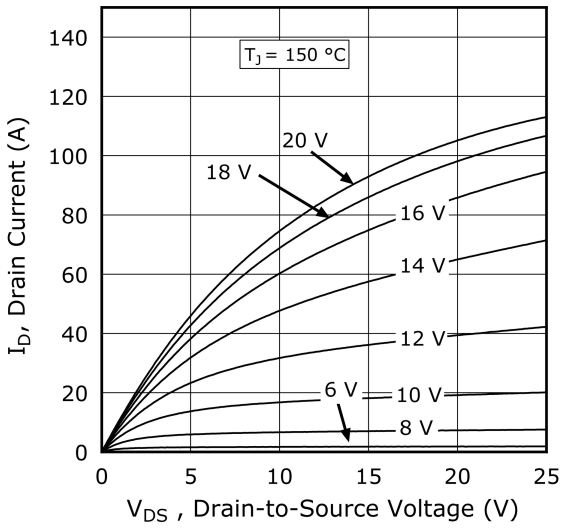

Figure 1-4. Drain Current vs. V_{DS} at V_{GS}

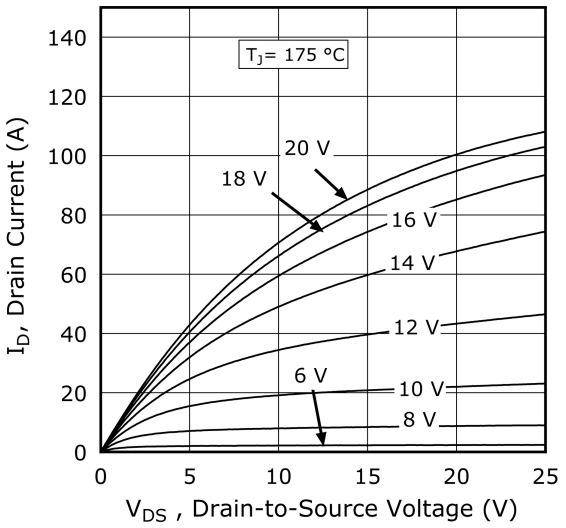

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Figure 1-5. $R_{DS(on)}$ vs. Junction Temperature

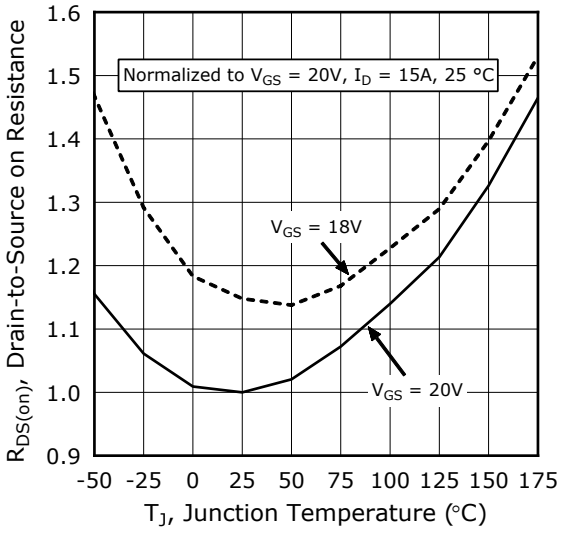

Figure 1-6. Gate Charge Characteristics

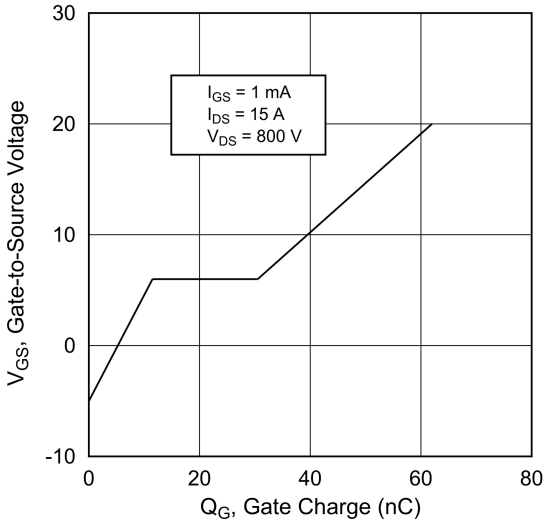

Figure 1-7. Capacitance vs. Drain-to-Source Voltage

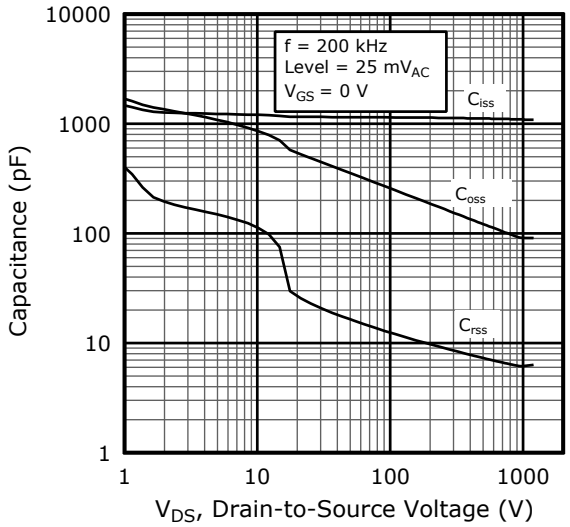

Figure 1-8. Output Charge vs. Drain-to-Source Voltage

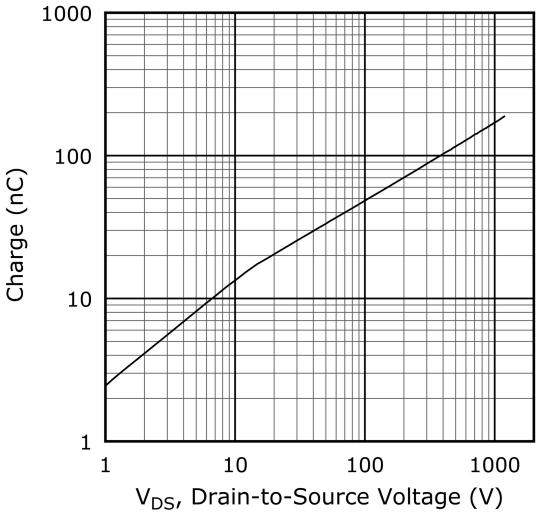

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Figure 1-9. Output Stored Energy vs. V_{DS}

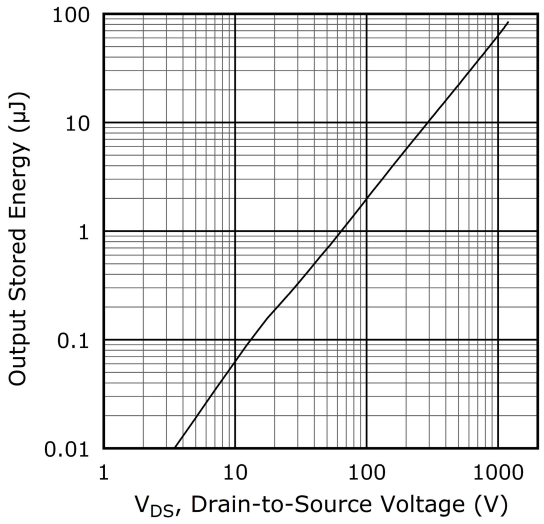

Figure 1-10. I_D vs. V_{DS} 3rd Quadrant Conduction

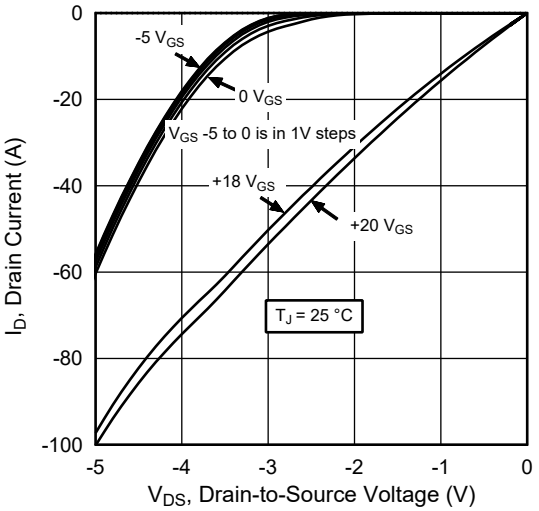

Figure 1-11. I_D vs. V_{DS} 3rd Quadrant Conduction

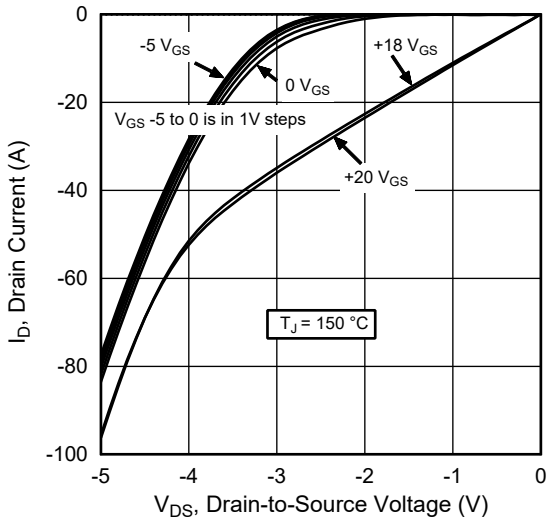

Figure 1-12. Switching Energy E_{on} vs. V_{DS} & I_D

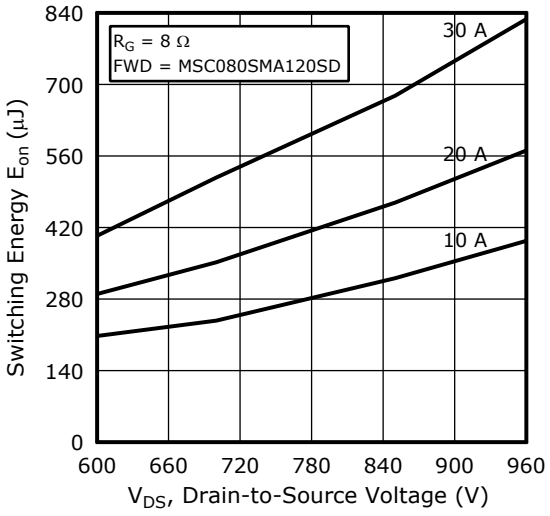

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Figure 1-13. Switching Energy E_{off} vs. V_{DS} & I_D

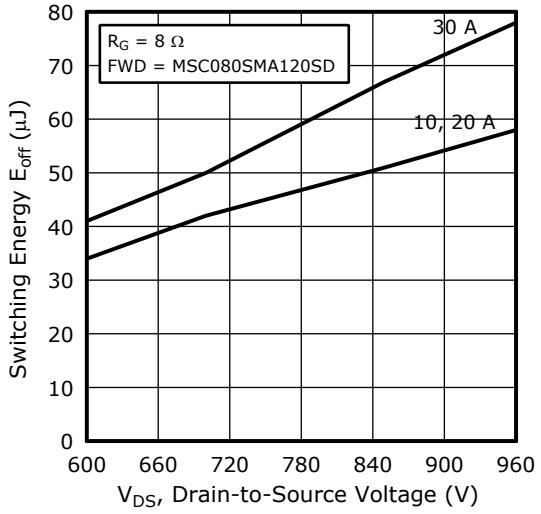

Figure 1-14. Switching Energy vs. R_G

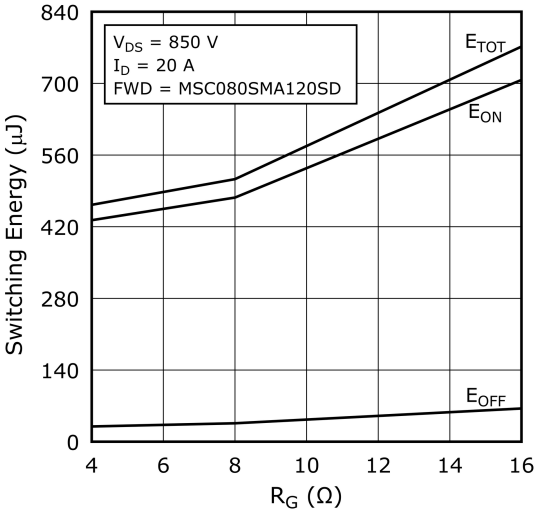

Figure 1-15. Switching Energy vs. Junction Temperature

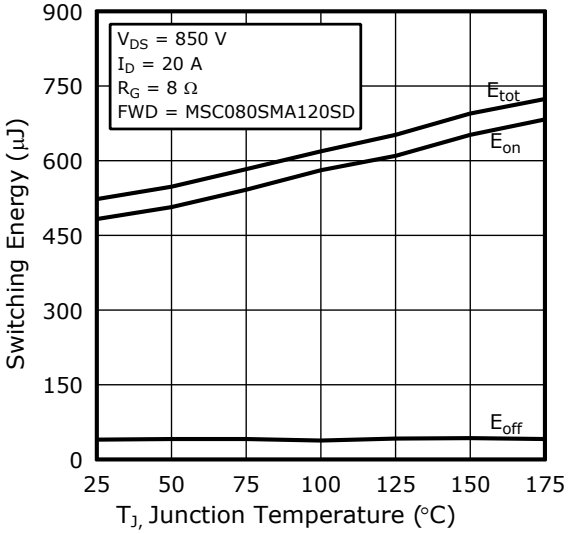

Figure 1-16. Threshold Voltage vs. Junction Temperature

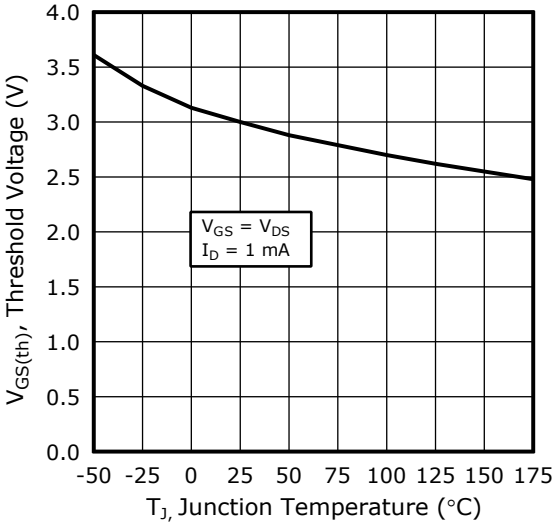

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Figure 1-17. Forward Safe Operating Area

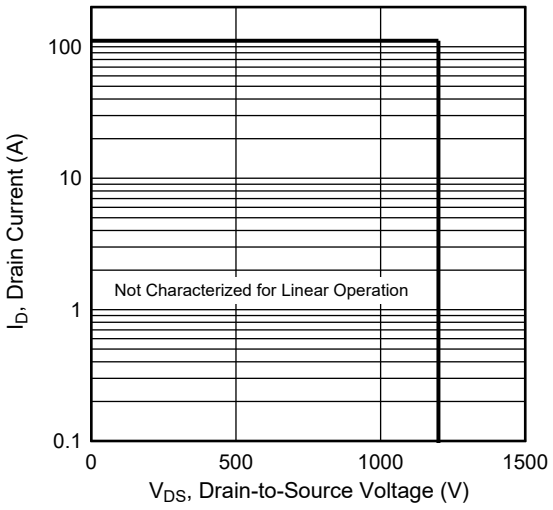
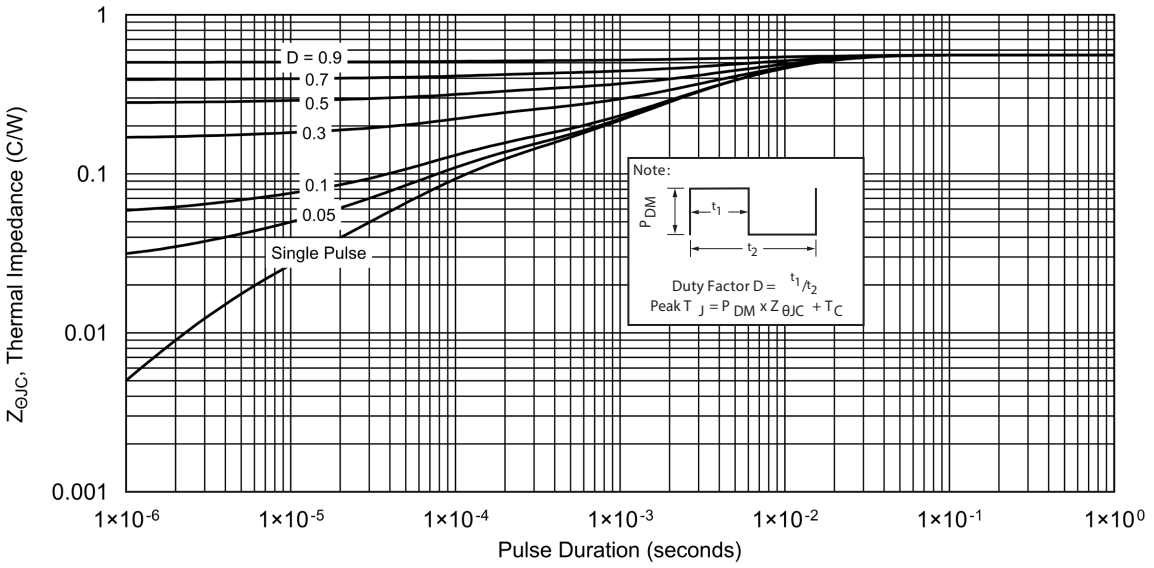
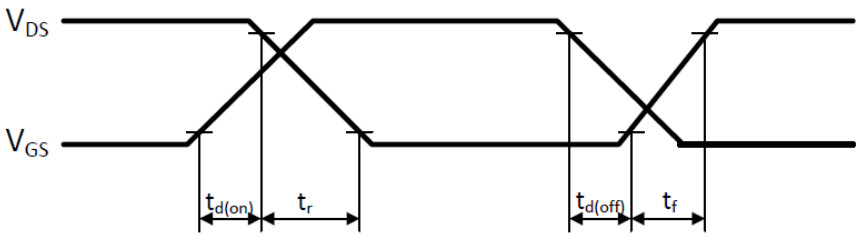


Figure 1-18. Maximum Transient Thermal Impedance



The following figure shows the switching waveform diagram of this device.

Figure 1-19. Switching Waveform



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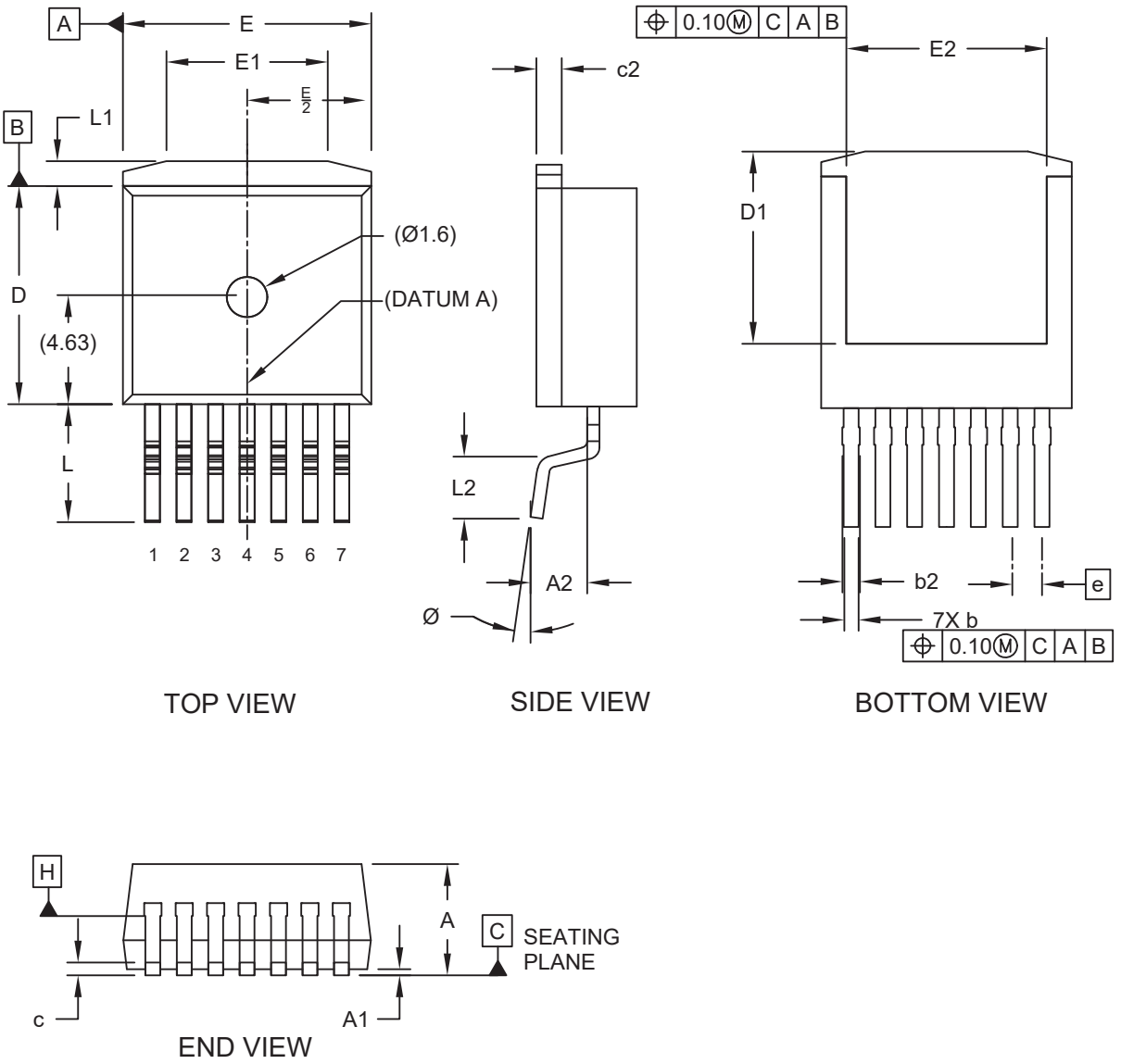
2. Package Specification

This section shows the package specification of this device.

2.1 Package Outline Drawing

The following figure illustrates the TO-263-7L XL package outline of this device.

Figure 2-1. Package Outline Drawing



The following table shows the TO-263-7L XL dimensions and should be used in conjunction with the package outline drawing.

Table 2-1. TO-263-7L XL Dimensions

Symbol	Description	Min. (mm)	Max. (mm)
N	Number of leads	7	
e	Pitch	1.27 BSC	

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.....continued			
Symbol	**Description**	**Min. (mm)**	**Max. (mm)**
A	Overall height	4.30	4.70
A1	Seating plane height	—	0.25
A2	Seating plane to lead	2.20	2.60
b	Lead width	0.52	0.72
b1		0.60	0.80
c	Lead thickness	0.42	0.62
c2	Thermal pad thickness	1.07	1.47
L	Lead length	4.55	4.95
L1	Tab length	0.87	1.27
L2	Foot length	2.48	2.88
D	Molded body length	9.05	9.45
D1	Thermal pad length	7.58	7.98
E	Total width	9.80	10.20
E1	Thermal pad width step back	6.30	6.70
E2	Thermal pad width	7.80	8.20
Ø	Lead foot angle	0°	8°

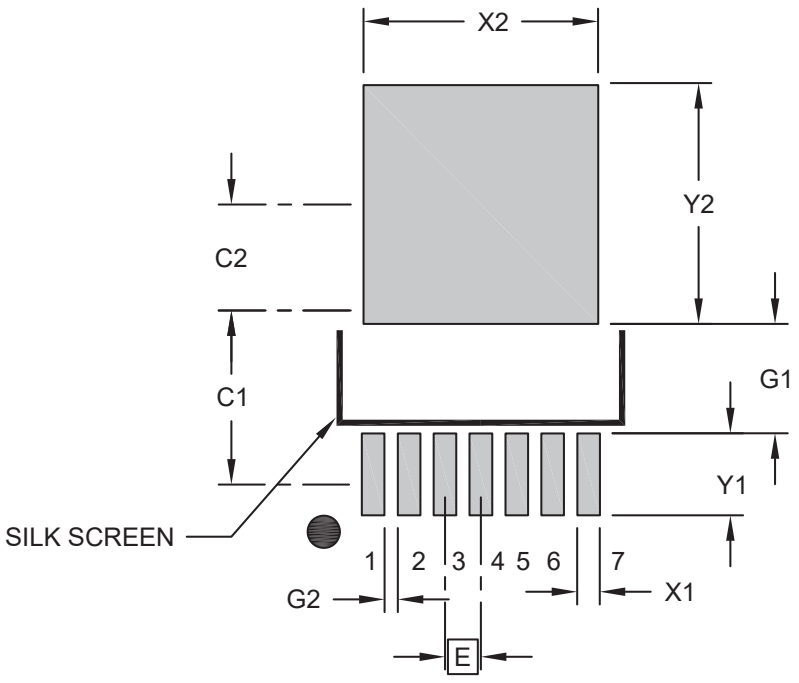
Note: Dimensioning and tolerancing per ASME Y14.5M.

- BSC: Basic dimension. Theoretically exact value shown without tolerances.

2.2 Recommended Land Pattern

The following figure illustrates the recommended land pattern of this device.

Figure 2-2. Recommended Land Pattern



The following table shows the recommended land pattern dimensions.

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Table 2-2. Recommended Land Pattern Dimensions

Symbol	Description	Min. (mm)	Nom. (mm)	Max. (mm)
E	Contact pitch	1.27 BSC		
X2	Center pad width	—	—	8.30
Y2	Center pad length	—	—	8.45
C1	Contact pad spacing	—	6.45	—
C2	Contact pad spacing	—	4.30	—
X1	Contact pad width (X7)	—	—	0.80
Y1	Contact pad length (X7)	—	—	2.90
G1	Contact pad to center pad (X7)	3.88	—	—
G2	Contact pad to contact pad (X6)	0.47	—	—

Notes:

- Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process.

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3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
C	07/2024	The following change is made in this revision • Updated 2.1. Package Outline Drawing • Added 2.2. Recommended Land Pattern
B	05/2024	The following change is made in this revision • Updated Figure 1-5
A	04/2024	Initial revision

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