EVALUATION KIT AVAILABLE

MAX17320

2S-4S ModelGauge m5 EZ Fuel Gauge with Protector, Internal Self-Discharge Detection, and SHA-256 Authentication

General Description

The MAX17320 is a 38µA I_Q stand-alone pack-side fuel gauge IC with protector, battery internal self-discharge detection, and optional SHA-256 authentication for 2 to 4 series lithium-ion/polymer batteries.

The IC monitors the voltage, current, temperature and state of the battery to provide protection against over/undervoltage, overcurrent, short-circuit, over/undertemperature, overcharge, and internal self-discharge conditions using external high-side N-FETs, and provides charging prescription to ensure that the battery operates under safe conditions, thereby prolonging the life of the battery. The IC balances the cells using internal FETs. During prequal charging, the IC uses the CHGFET to linearly control charging.

To prevent battery pack cloning, the IC integrates SHA-256 authentication with a 160-bit secret key. Each IC incorporates a unique 64-bit ID.

The fuel gauge uses Maxim ModelGauge™ m5 algorithm that combines the short-term accuracy and linearity of a coulomb counter with the long-term stability of a voltage-based fuel gauge to provide industry-leading fuel gauge accuracy. The IC automatically compensates for cell aging, temperature, and discharge rate, and provides accurate state-of-charge (SOC) in milliampere-hours (mAh) or percentage (%) over a wide range of operating conditions.

The IC provides a configurable always-on LDO that can power small critical loads on the system side without overloading the cells even under fault conditions. Dynamic power functionality provides the instantaneous maximum battery output power which can be delivered to the system without violating the minimum system input voltage.

A Maxim 1-Wire® or 2-wire I²C/SMBus interface provides access to data and control registers. The IC is available in a lead-free, 2.4mm x 2.6mm 30-bump 0.4mm pitch WLP and 4mm x 4mm 24-pin TQFN packages.

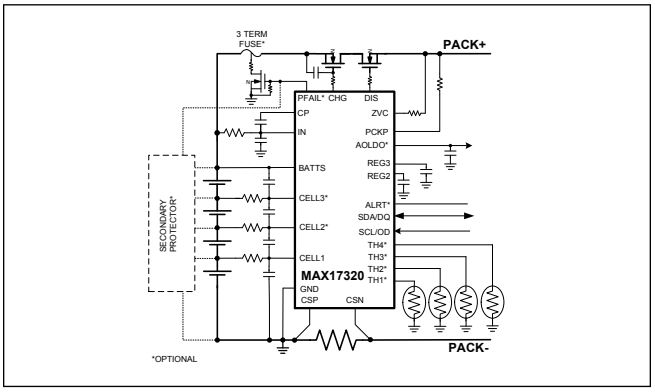
Applications

- Smartphones, Tablets, and 2-in-1 Laptops
- Medical Devices, Health and Fitness Monitors
- Digital Still, Video, and Action Cameras
- Handheld Computers, Radios, and Terminals
- Power Tools, Wireless Speakers, and Drones
- Smart Batteries and Battery Backup

Benefits and Features

- Battery Health + Programmable Safety/Protection
  - Overvoltage (Temperature Dependent)
  - Overcharge/Overdischarge/Short-Circuit Current
  - Over/Undertemperature
  - Undervoltage + SmartEmpty
  - Battery Internal Self-Discharge Detection
  - Ideal Diode Discharge During Charge Fault
  - Charging Prescriptions (JEITA)
  - Prequal Charge Control with CHG FET
- ModelGauge m5 EZ Algorithm
  - Percent, Capacity, Time-to-Empty/Full, Age
  - Cycle+™ Age Forecast
- Precision Measurement Without Calibration
  - Current, Voltage, Power, Time, Cycles
  - Die Temperature, 4 Thermistors ±1°C
- Cell Balancing with Internal FETs
- SHA-256 Authentication
- Nonvolatile Memory for Stand-Alone Operation
  - History Logging, User Data (84 Bytes)
- Low Quiescent Current
  - FETs Enabled: 38µA Active
- Pushbutton Wakeup—Eliminates System Consumption Until Button Press
- Always-On LDO
- Dynamic Power—Estimates Power Capability
- SBS 1.1 Compatible Register Set

Simplified Block Diagram



ModelGauge is a trademark of Maxim Integrated Products, Inc.
1-Wire is a registered trademark of Maxim Integrated Products, Inc.
Cycle+ is a trademark of Maxim Integrated Products, Inc.

Ordering Information appears at end of data sheet.

19-100749; Rev 11; 1/25

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Absolute Maximum Ratings

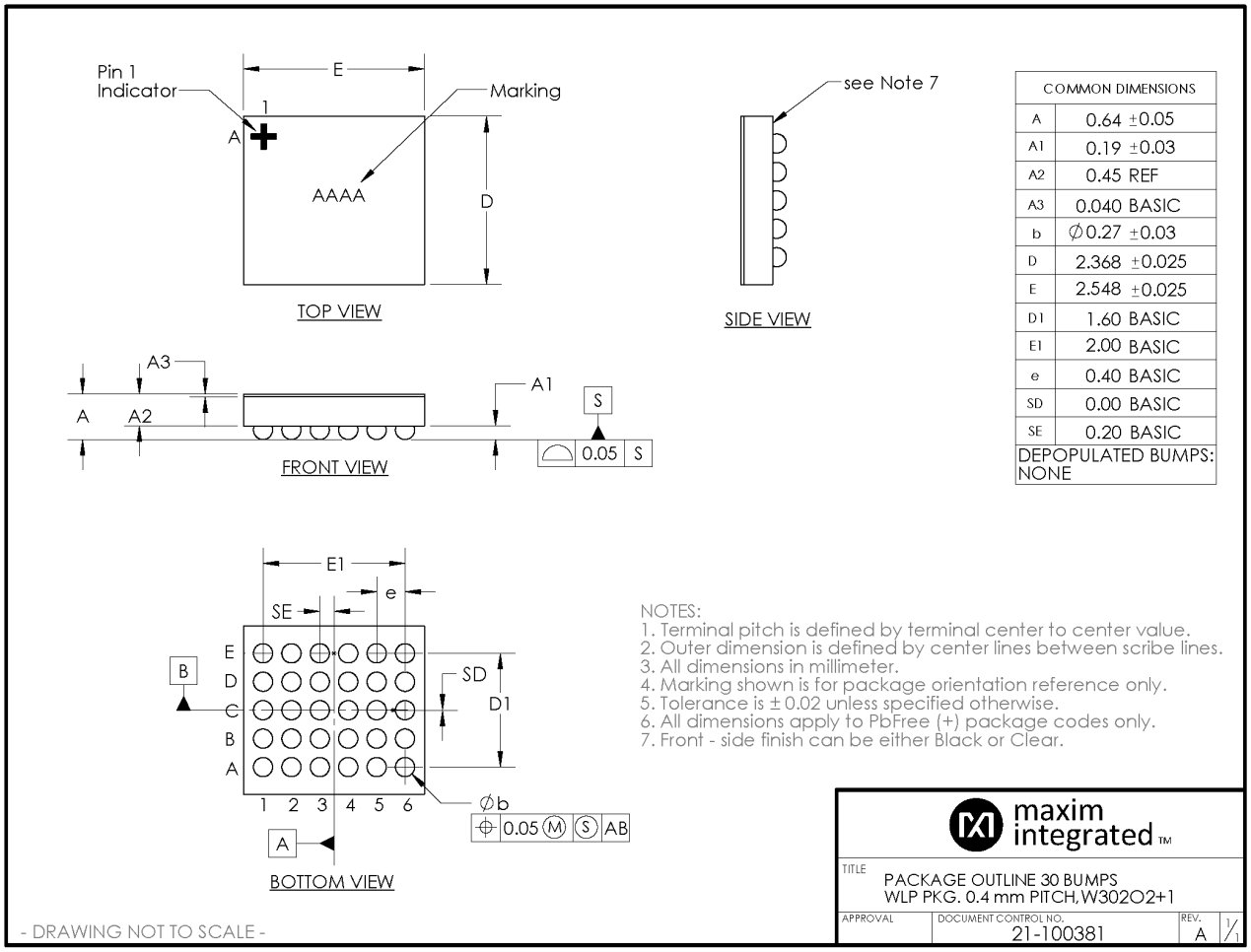
IN to GND ..... -0.3V to +20V
BATTS to GND ..... -0.3V to min of (IN + 0.3 and +20)V
CELL3, CELL2, CELL1 to GND ..... -0.3V to min of (IN + 0.3 and BATTS + 0.3)V
BATTS to CELL3 (Balancing switches) ..... -0.3V to +20V
CELL3 to CELL2 (Balancing switches) ..... -0.3V to +20V
CELL2 to CELL1 (Balancing switches) ..... -0.3V to +20V
CELL1 to GND (Balancing switches) ..... -0.3V to +20V
CP to GND ..... -0.3V to +36V
CP to IN ..... -0.3V to +36V
CHG to GND ..... IN - 0.3 to CP + 0.3
DIS to GND ..... PCKP - 0.3V to CP + 0.3V
PCKP, ZVC to GND ..... -0.3V to +28V
SCL, SDA, ALRT to GND ..... -0.3V to +20V
REG3, AOLDO to GND ..... -0.3V to +6V
PFAIL, TH1, TH2, TH3, TH4 to GND ..... -0.3V to REG3 +0.3V
REG2 to GND ..... -0.3V to +2.2V
CSN to GND ..... -2V to +2V
CSP to GND ..... -0.3V to +0.3V
Continuous Current of Balancing Switches 100mA
Continuous Current between ZVC and IN 50mA
Continuous Power Dissipation (Single-Layer Board) (T_A = +70°C, derate 65mW/°C above +70°C) 1000mW
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 55mW/°C above +70°C) 1950mW
Operating Temperature Range ..... -40°C to +85°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

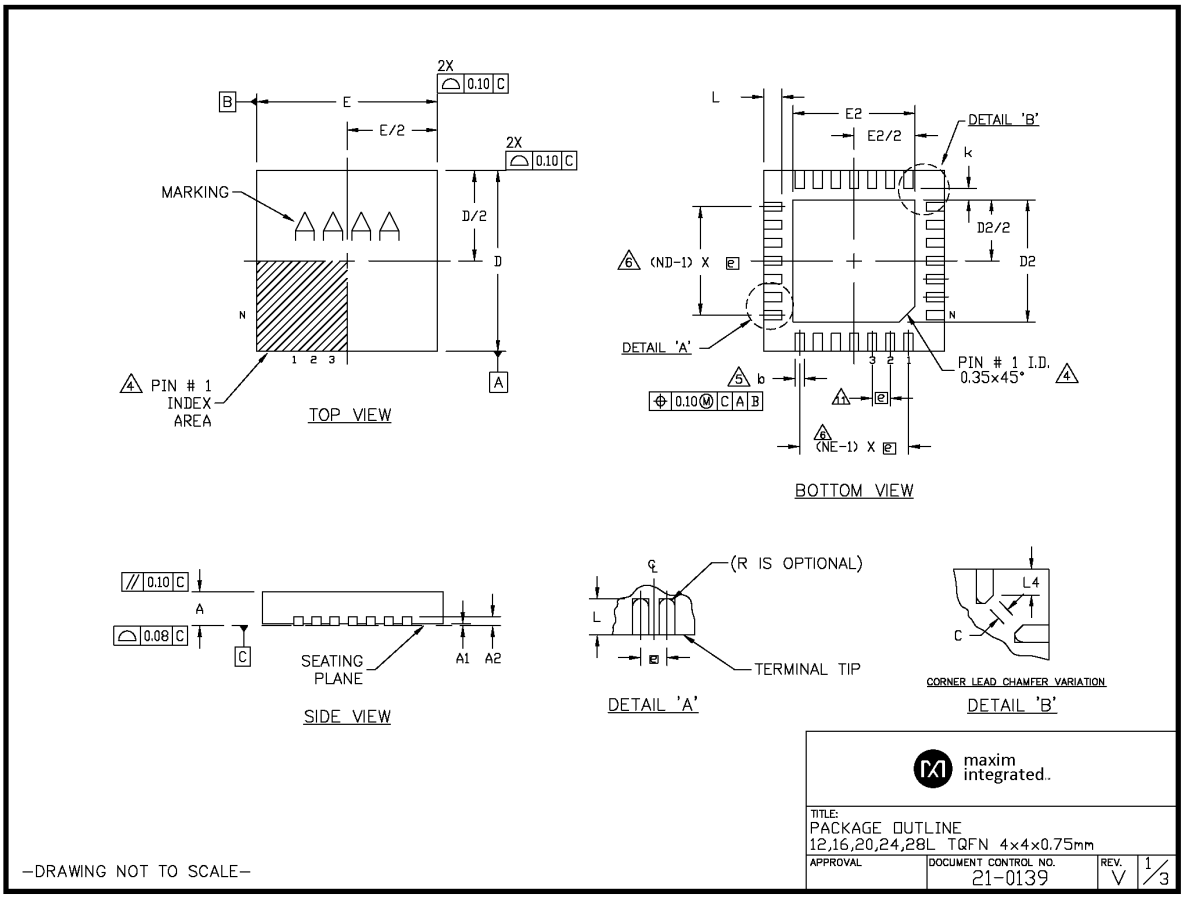
30 WLP

Package Code	W302O2+1
Outline Number	21-100381
Land Pattern Number	Refer to ***Application Note 1891***
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49°C/W
Junction to Case (θ_{JC})	N/A



24 TQFN

Package Code	T2444+4C
Outline Number	21-0139
Land Pattern Number	90-0022
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	68°C/W
Junction to Case (θ_{JC})	11°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	60°C/W
Junction to Case (θ_{JC})	11°C/W



For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(IN = 4.2V to 18V, T_A = -40°C to +85°C, typical values are T_A = +25°C, see the schematic in the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{IN}		4.2		18	V
Shutdown Supply Current	I_{DD0}	Shutdown, V_{BATT} = 18V, +25°C		2.2	3.5	µA
Ship Mode Supply Current	I_{DD1}	T_A ≤ +50°C		16	25	µA
Active Supply Current	I_{DD2}	T_A ≤ +50°C, average current, not including thermistor measurement current, AOLDO off		38	57	µA
REG3 Voltage	V_{REG3}			3.4		V
REG2 Voltage	V_{REG2}			1.8		V
Always-On LDO Voltage	V_{AOLDO}	1.8V output, I_{LOAD} = 2mA	1.62	1.8	1.98	V
		3.4V output, I_{LOAD} = 2mA	3	3.4	3.8	
CHARGE PUMP						
Charge Pump Output	V_{CP}	1.5 x IN < CP_{REG}, V_{CP} - IN	1.5 x IN - 1	1.5 x IN	1.5 x IN + 1	V
		6V selection	5	6	7	
		8V setting, V_{IN} > 6V	7	8	9	
		10V setting, V_{IN} > 7.5V	9	10	11	
CHG DRIVER						
CHG Driver Output	$V_{CHGHIGH}$	CHG is high, IN = 10V, 10MΩ resistor between CHG and IN	CP - 0.1	CP	CP + 0.1	V
CHG Resistance	R_{CHGON}	CHG is high			4000	Ω
	R_{CHGOFF}	CHG is low			1000	
DIS DRIVER						
DIS Driver Output	$V_{DISHIGH}$	DIS is high, IN = 10V, 10MΩ resistor between DIS and PCKP	CP - 0.1	CP	CP + 0.1	V
DIS Resistance	R_{DISON}	DIS is high			4000	Ω
	R_{DISOFF}	DIS is low			1000	
ZERO-VOLT RECOVERY						
ZVC Minimum Voltage	V_{ZVCMIN}	IN = 0, 10mA Recovery current	1.4	2.4	3.3	V
		IN = 0, 30mA Recovery current	2.1	2.9	3.8	
		IN = 0, 50mA Recovery current	2.5	3.4	4.5	
ANALOG-TO-DIGITAL CONVERSION						
Cell Voltage Measurement Error	V_{GERR}	T_A = +25°C (Note 10)	-12.5		+12.5	mV
		(Note 10)	-25		+25	
Cell Voltage Mismatch Error	V_{CMM}	Cell voltage mismatch between channels (CELL1, 2, 3, 4) +25°C	-5		+5	mV

Electrical Characteristics (continued)

(IN = 4.2V to 18V, T_A = -40°C to +85°C, typical values are T_A = +25°C, see the schematic in the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BATT Voltage Measurement Error	VB_{GERR}	T_A = +25°C, IN = BATTS, from 4.2V to 20V	-30		+30	mV
		IN = BATTS, from 4.2V to 20V	-100		+100	
PCKP Voltage Measurement Error	VP_{GERR}	T_A = +25°C	-30		+30	mV
			-100		+100	
Cell Voltage Measurement Resolution	V_{LSB}	Individual cell		78.125		µV
BATT Voltage Measurement Resolution	VB_{LSB}	BATTS		312.5		µV
PCKP Voltage Measurement Resolution	VP_{LSB}	PCKP pin		312.5		µV
Cell Voltage Measurement Range	V_{FS}	(Note 10)	2.1		4.9	V
BATT Voltage Measurement Range	VB_{FS}	BATTS pin	4.2		19.6	V
PCKP Voltage Measurement Range	VP_{FS}	PCKP pin	4.2		19.6	V
Current Measurement Offset Error	I_{OERR}	CSP = 0V, long-term average (Note 2)		±2		µV
Current Measurement Gain Error	I_{GERR}	CSP between -50mV and +50mV	-1		+1	% of Reading
Current Measurement Resolution	I_{LSB}			1.5625		µV
Current Measurement Range	I_{FS}			±51.2		mV
Die Temperature Measurement Error	TI_{GERR}			±1		ºC
Die Temperature Measurement Resolution	TI_{LSB}	(Note 11)		0.00391		ºC
Thermistor Measurement Error	TE_{GERR}	See the *Thermistor Configuration* section		±1		% of Reading
RESISTANCE AND LEAKAGE						
Leakage Current, CELL1, CELL2, CELL3, BATTS, CSN, ALRT, PFAIL, ZVC, CHG, DIS	I_{LEAK}	ALRT < 15V, IN < CP < 30V	-1		+1	µA
Cell-Balancing Resistance	R_{BAL}	V_{BATT} = 18V, I_{BAL} = 50mA, between BATTS - CELL3, CELL3 - CELL2, CELL2 - CELL1, and CELL1 - CSP	3	9	20	Ω
Communication Removal Test Current	I_{PD}	SDA, SCL pin = 0.4V	0.05	0.2	0.4	µA

Electrical Characteristics (continued)

(IN = 4.2V to 18V, T_A = -40°C to +85°C, typical values are T_A = +25°C, see the schematic in the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT / OUTPUT						
Output Drive Low, ALRT, SDA/DQ, PFAIL	V_{OL}	I_{OL} = 4mA, REG3 = 3.4V			0.4	V
Output Drive High, PFAIL	V_{OH}	I_{OH} = -1mA	REG3-0.1			V
Input Logic High, SCL/OD, SDA/DQ, ALRT	V_{IH}		1.5			V
Input Logic Low, SCL/OD, SDA/DQ, ALRT	V_{IL}				0.44	V
ALRT Wake Debounce		Sleep mode		100		ms
COMPARATORS						
Overcurrent Threshold Offset Error	OC_{OE}	OC, OD, or SC comparator	-1.2		+1.2	mV
Overcurrent Threshold Gain Error	OC_{GE}	OC, OD, or SC comparator	-5.0		+5.0	% of Threshold
NONVOLATILE MEMORY						
Programming Supply Current	I_{PROG}	Current from V_{BATT} for block programming		4	10	mA
Block Programming Time	t_{BLOCK}			368	7360	ms
Page Programming Time	t_{UPDATE}	SHA secret update or learned parameters update		64	1280	ms
Nonvolatile Memory Recall Time	t_{RECALL}				5	ms
Write Capacity, Configuration Memory	n_{CONFIG}	(Notes 2, 3, 4)		7		writes
Write Capacity, SHA Secret	n_{SECRET}	(Notes 2, 3, 4)		5		writes
Write Capacity, Learned Parameters	$n_{LEARNED}$	(Notes 2, 3, 4)		99		writes
Data Retention	t_{NV}	(Note 2)	10			years
1-WIRE INTERFACE, REGULAR SPEED						
Time Slot	t_{SLOT}		60		120	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		60		120	µs
Write-1 Low Time	t_{LOW1}		1		15	µs
Read-Data Valid	t_{RDV}				15	µs
Reset-Time High	t_{RSTH}		480			µs
Reset-Time Low	t_{RSTL}		480		960	µs
Presence-Detect High	t_{PDH}		15		60	µs
Presence-Detect Low	t_{PDL}		60		240	µs

Electrical Characteristics (continued)

(IN = 4.2V to 18V, T_A = -40°C to +85°C, typical values are T_A = +25°C, see the schematic in the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1-WIRE INTERFACE, OVERDRIVE SPEED						
Time Slot	t_{SLOT}		6		16	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		6		16	µs
Write-1 Low Time	t_{LOW1}		1		2	µs
Read-Data Valid	t_{RDV}				2	µs
Reset-Time High	t_{RSTH}		48			µs
Reset-Time Low	t_{RSTL}		48		80	µs
Presence-Detect High	t_{PDH}		2		6	µs
Presence-Detect Low	t_{PDL}		8		24	µs
2-WIRE INTERFACE (I^2C and SMBus)						
SCL Clock Frequency	f_{SCL}	(Note 5)			400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 6)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 7, 8)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 7)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		5		300	ns
Fall Time of Both SDA and SCL Signals	t_F		5		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Width Suppressed by Input Filter	t_{SP}	(Note 9)			50	ns
Capacitive Load for Each Bus Line	C_B				400	pF
SCL, SDA Input Capacitance	C_{BIN}			6		pF
SCL Low Timeout				30		ms
TIMING						
Time-Base Accuracy	t_{ERR}	T_A = +25°C	-1		+1	%

Electrical Characteristics (continued)

(IN = 4.2V to 18V, T_A = -40°C to +85°C, typical values are T_A = +25°C, see the schematic in the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SHA Calculation Time	t_{SHA}			4.5	10	ms
TH Precharge Time	t_{PRE}	Time between turning on the TH bias and analog-to-digital conversions	8.48			ms
Power-on-Reset Time	t_{POR}	(Note 7)			10	ms
Task Period	t_{TP}			351.5		ms

Note 1: All voltages are referenced to CSP.

Note 2: Specification is Guaranteed by Design (GBD); not production tested.

Note 3: Write capacity numbers shown have one write subtracted for the initial write performed during manufacturing test to set nonvolatile memory to a known value.

Note 4: Due to the nature of one-time programmable memory, write endurance cannot be production tested. Follow the nonvolatile memory and SHA secret update procedures detailed in the data sheet.

Note 5: Timing must be fast enough to prevent the IC from entering shutdown mode due to bus being low for a period greater than the shutdown timer setting.

Note 6: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 7: The maximum $t_{HD:DAT}$ can only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 8: This device internally provides a hold time of at least 100ns for the SDA signal (referred to as the minimum V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 9: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

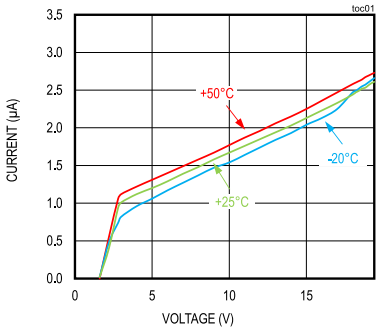
Note 10: BATTS to CELL3, CELL3 to CELL2, CELL2 to CELL1, or CELL1 to CSP, cell voltages between 2.3V and 4.9V; BATTS and CELL1 must be used. Neighbor CELL pins should be shorted if there is no battery connected between them.

Note 11: Specification is for TH1/TH2/TH3/TH4 channels.

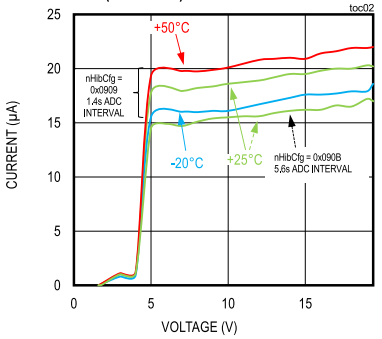
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

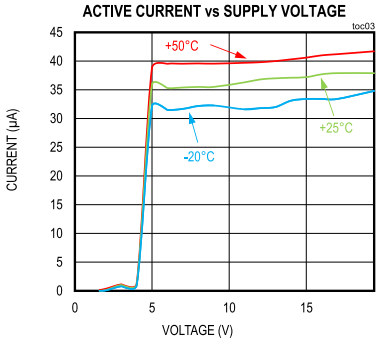
DEEP SHIP MODE CURRENT vs SUPPLY VOLTAGE



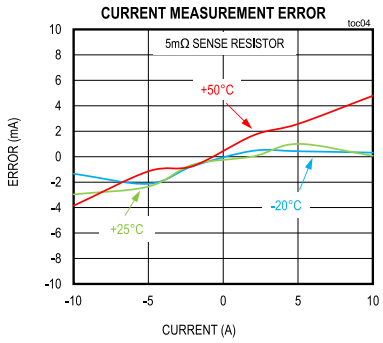
SHIP MODE (FETS OFF) CURRENT vs. SUPPLY VOLTAGE



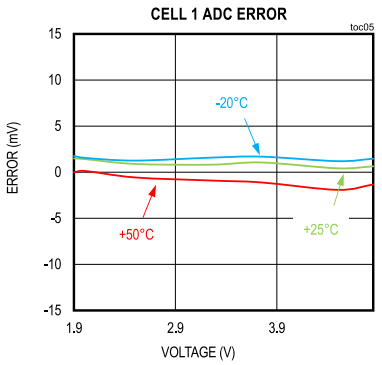
ACTIVE CURRENT vs SUPPLY VOLTAGE



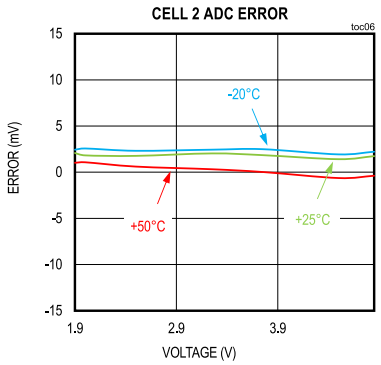
CURRENT MEASUREMENT ERROR



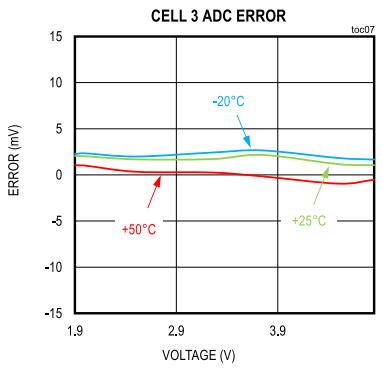
CELL 1 ADC ERROR



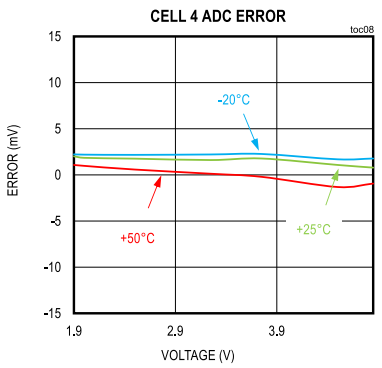
CELL 2 ADC ERROR



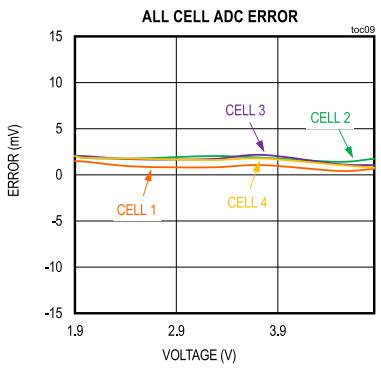
CELL 3 ADC ERROR



CELL 4 ADC ERROR

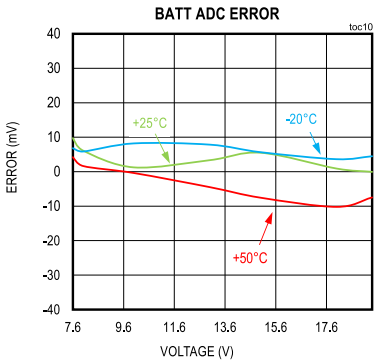


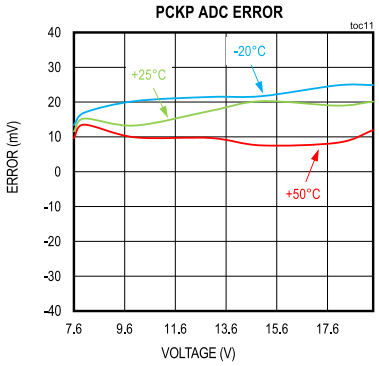
ALL CELL ADC ERROR

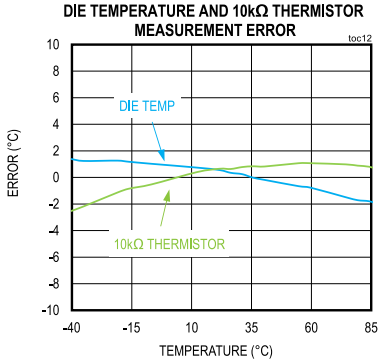


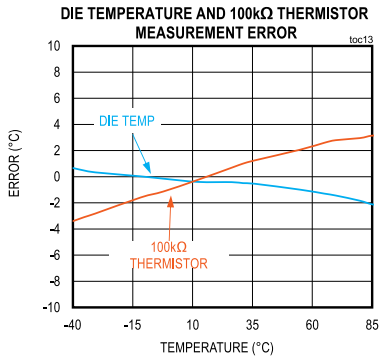
Typical Operating Characteristics (continued)

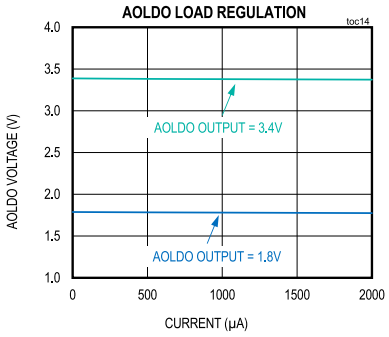
(T_A = +25°C, unless otherwise noted.)

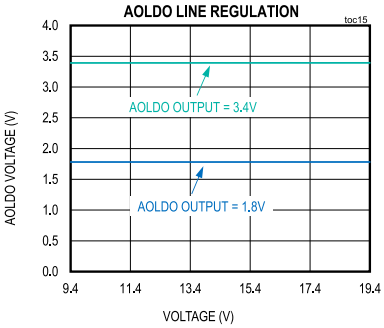


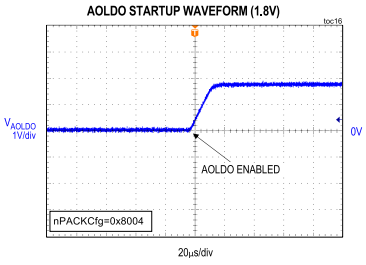


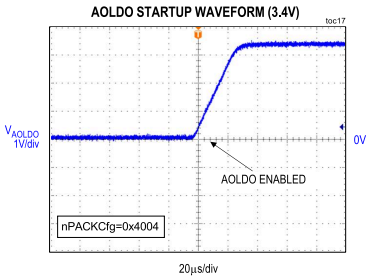








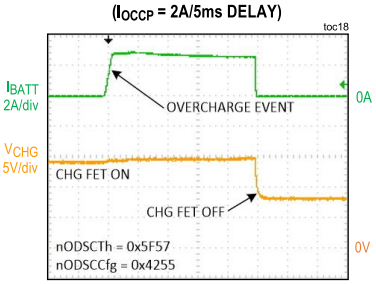




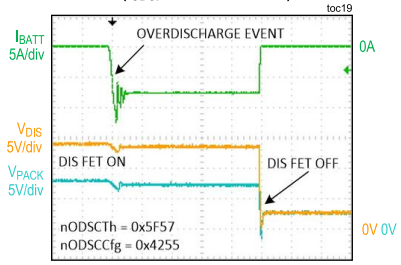
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

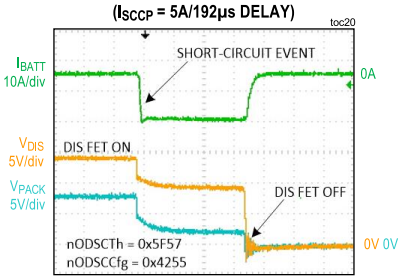
OVERCHARGE CURRENT PROTECTION
(I_{OCCP} = 2A/5ms DELAY)



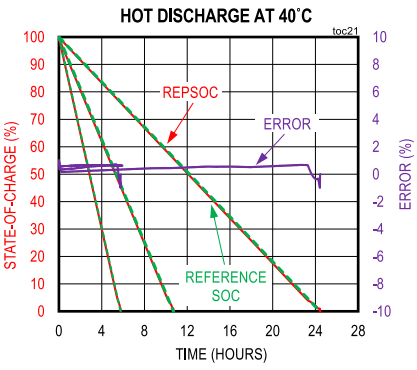
OVERDISCHARGE CURRENT PROTECTION
(I_{ODCP} = 4A/5ms DELAY)



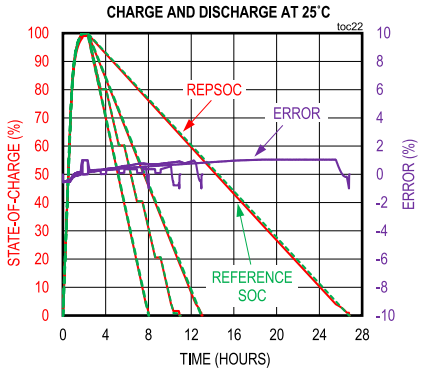
SHORT-CIRCUIT PROTECTION
(I_{SCCP} = 5A/192µs DELAY)



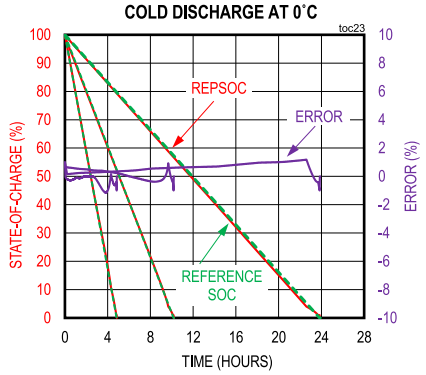
HOT DISCHARGE AT 40˚C



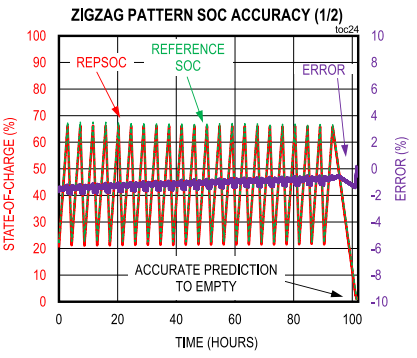
CHARGE AND DISCHARGE AT 25˚C



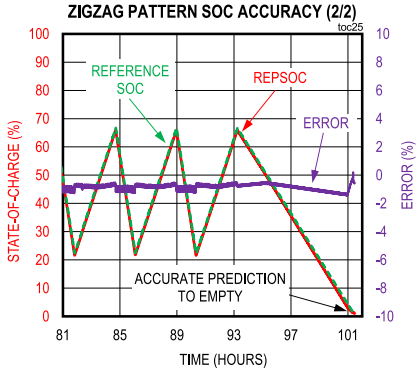
COLD DISCHARGE AT 0˚C



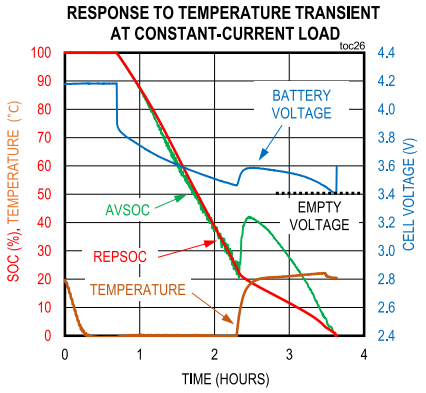
ZIGZAG PATTERN SOC ACCURACY (1/2)



ZIGZAG PATTERN SOC ACCURACY (2/2)

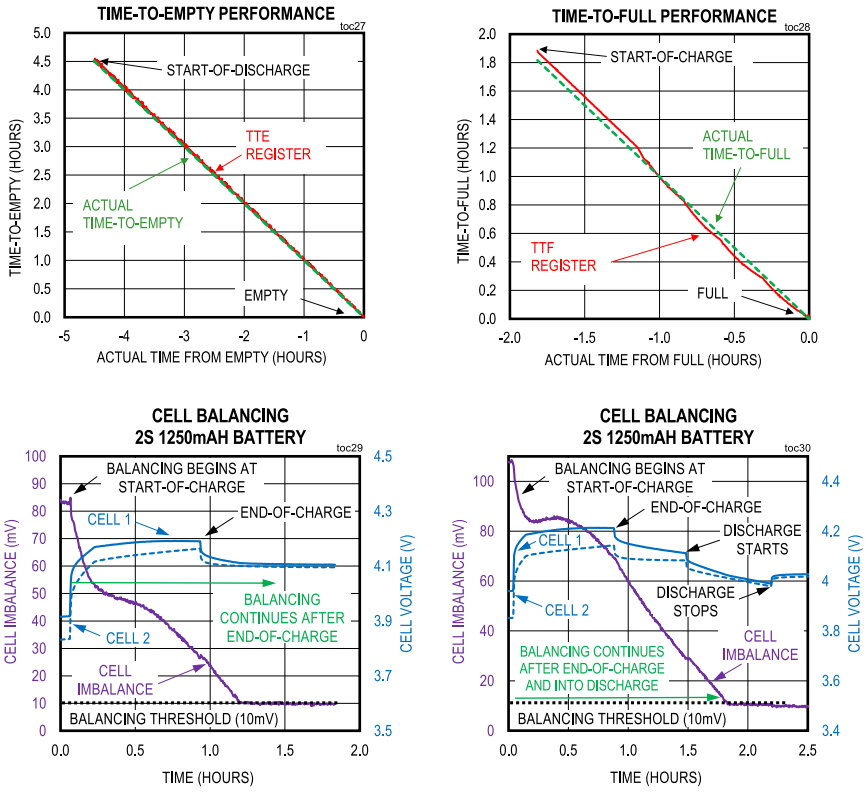


RESPONSE TO TEMPERATURE TRANSIENT AT CONSTANT-CURRENT LOAD



Typical Operating Characteristics (continued)

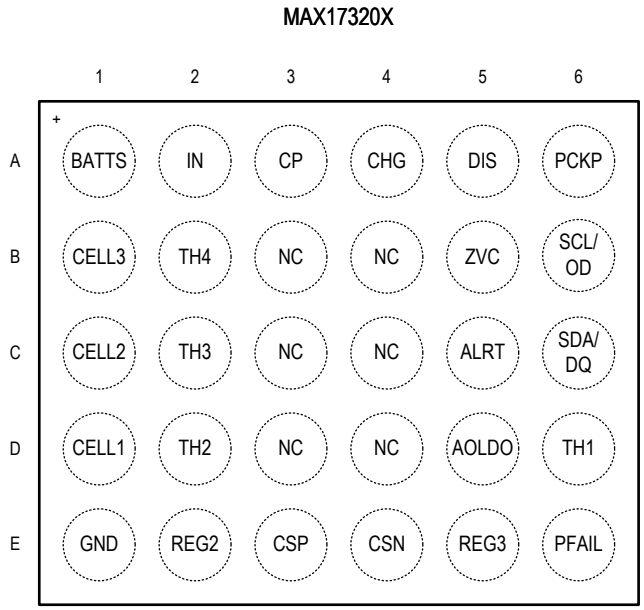
(T_A = +25°C, unless otherwise noted.)



Pin Configurations

WLP

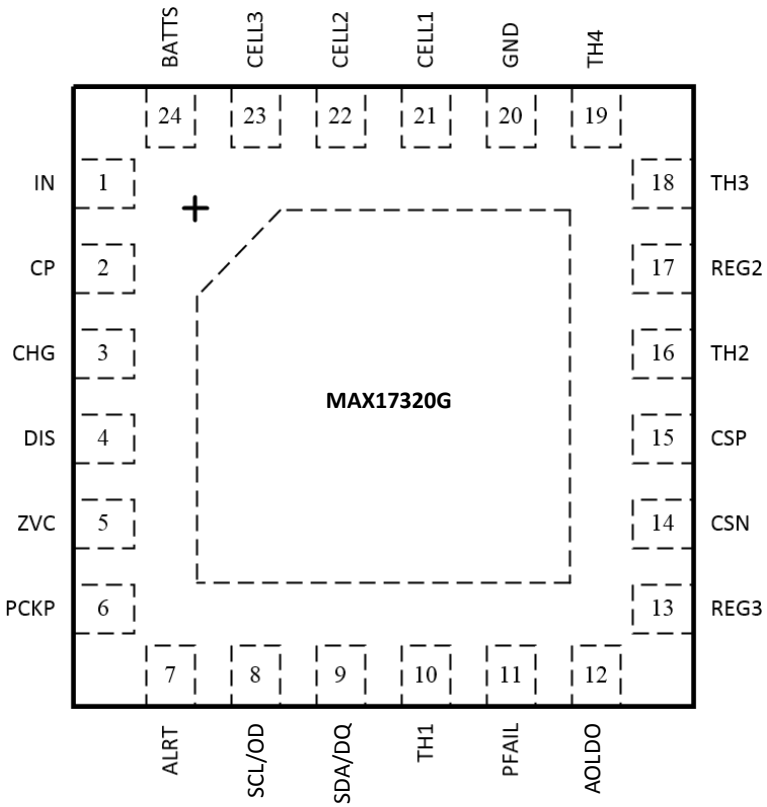
TOP VIEW
(BUMP SIDE DOWN)



(30-BUMP WLP, 0.4mm PITCH)

TQFN

TOP VIEW



(24-PIN TQFN, 4mm x 4mm)

Pin Description

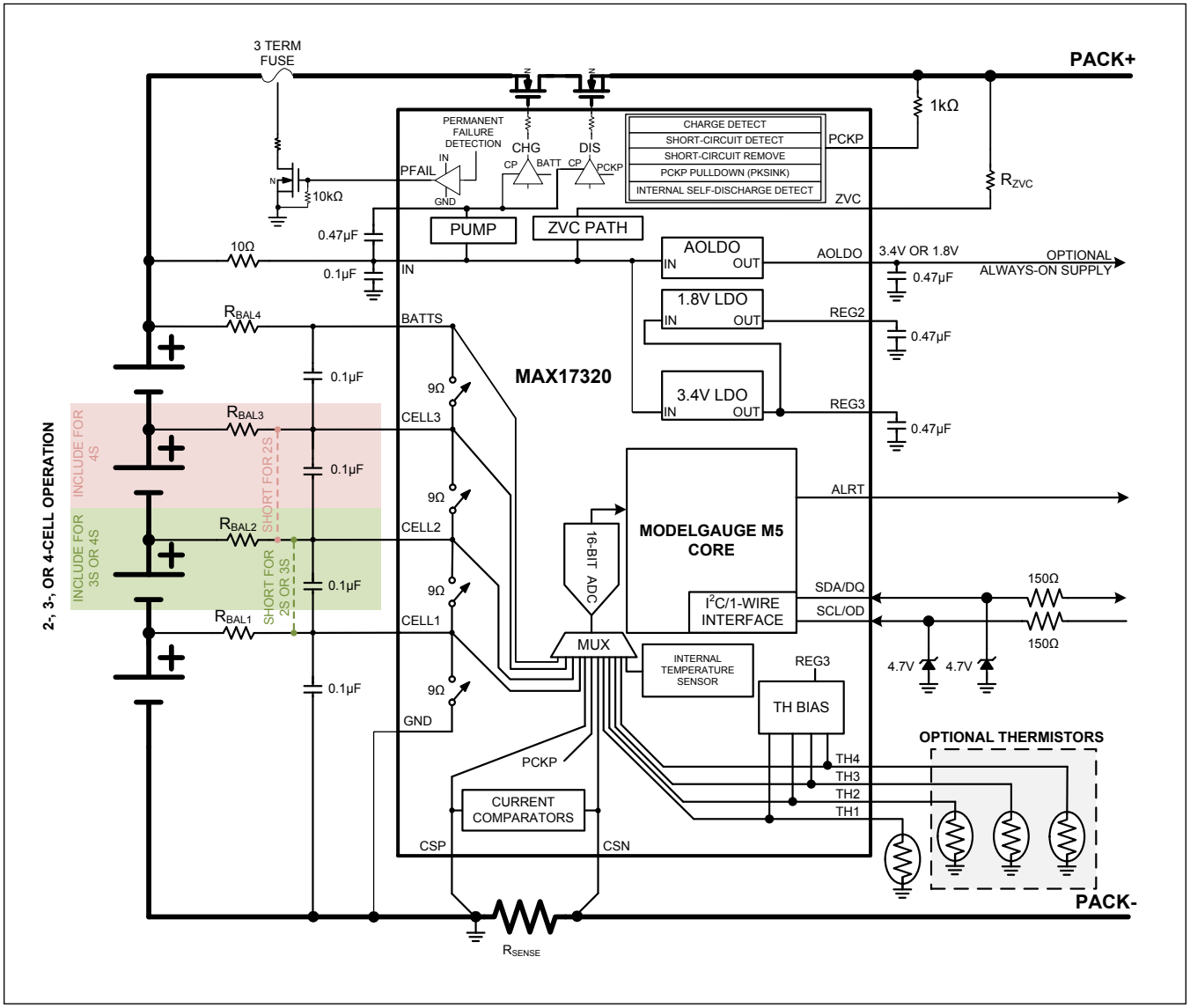
PIN		NAME	FUNCTION
WLP	TQFN		
A2	1	IN	Power Supply Input. Connect to the positive terminal of cell stack with a 10Ω resistor. Bypass with a 0.1µF/25V ceramic capacitor to GND.
A3	2	CP	Charge Pump Output and Bypass. Bypass CP to IN with a 0.47µF/25V ceramic capacitor.
A4	3	CHG	Charge FET Gate Control. Enable/disable the high-side CHG N-FET by driving the gate between CP and IN. Connect a 0.1µF capacitor from Charge FET gate to source.
A5	4	DIS	Discharge FET Gate Control. Enable/disable the high-side DIS N-FET by driving the gate between CP and PCKP.

Pin Description (continued)

PIN		NAME	FUNCTION
WLP	TQFN		
B5	5	ZVC	Zero-Volt Charge Path. Recovery charge current is set by the resistor from the Positive Terminal of the Pack Connector to the ZVC pin. Leave ZVC open if not used.
A6	6	PCKP	Connect to Positive Terminal of Pack Connector Through 1kΩ
C5	7	ALRT	Programmable Alert Output
B6	8	SCL/OD	Serial Clock Input for I^2C Communication or Speed Selection for 1-Wire Communication. Input only. For I^2C communication, connect to the clock terminal of the battery pack. Connect to CSN for standard speed 1-Wire communication. Connect to the REG3 pin for overdrive 1-Wire communication. SCL/OD has an internal pulldown (IPD) for sensing pack disconnection.
C6	9	SDA/DQ	Serial Data Input/Output for Both 1-Wire and I^2C Communication Modes. Open-drain output driver. Connect to the DATA terminal of the battery pack. SDA/DQ has an internal pulldown (IPD) for sensing pack disconnection.
D6	10	TH1	Thermistor Input 1. Connect a 10k/100k thermistor from TH1 to GND. Leave disconnected or connect to GND if not used.
E6	11	PFAIL	Permanent Failure Indicator. Connect to a three terminal fuse to take action in case of primary FET failure detection. If not used, connect to GND with a 1kΩ resistor.
D5	12	AOLDO	Always-On LDO. Configurable as 3.4V or 1.8V. Bypass to GND with a 0.47µF/10V ceramic capacitor. Leave disconnected or connect to GND with a 10kΩ resistor if not used.
E5	13	REG3	Internal 3.4V Regulator Output. Bypass to GND with a 0.47µF/10V ceramic capacitor.
E4	14	CSN	System Ground and Current Measurement Negative Sense Point. Kelvin connect to load side of the sense resistor.
E3	15	CSP	Device Ground and Current Measurement Positive Sense Point. Kelvin connect to cell side of the sense resistor.
D2	16	TH2	Thermistor Input 2. Connect 10k/100k thermistor from TH2 to GND. Leave disconnected or connect to GND if not used.
E2	17	REG2	Internal 1.8V Regulator Output. Bypass to GND with a 0.47µF/10V ceramic capacitor.
C2	18	TH3	Thermistor Input 3. Connect a 10k/100k thermistor from TH3 to GND. Leave disconnected or connect to GND if not used.
B2	19	TH4	Thermistor Input 4. Connect a 10k/100k thermistor from TH4 to GND. Leave disconnected or connect to GND if not used.
E1	20	GND	Ground Pin. Connect to ground. Do not share the ground trace with the CSP Kelvin-sense trace.
D1	21	CELL1	Cell Voltage Sense 1. Used for cell balancing and voltage sensing.
C1	22	CELL2	Cell Voltage Sense 2. Used for cell balancing and voltage sensing.
B1	23	CELL3	Cell Voltage Sense 3. Used for cell balancing and voltage sensing.
A1	24	BATTS	Battery Voltage Sense of Top Cell in Series Stack. Used for cell balancing and voltage sensing.
B3, B4, C3, C4, D3, D4	—	NC	No Connect. The NC pins are not internally connected and can be used for routing vias in certain cases. B3, C3, D3 can take a via from ZVC and ALRT. B4, C4, D4 can take a via from TH2, TH3, TH4 and AOLDO. Other placement of the vias under the NC pins could cause noise to couple to the IC.

Functional Diagrams

Block Diagram



Detailed Description

General Description

The MAX17320 is a 38µA I_Q stand-alone pack-side fuel gauge IC with protector and optional SHA-256 authentication for 2-, 3-, or 4-cell lithium-ion/polymer batteries which implements Maxim's ModelGauge m5 algorithm without requiring host interaction for configuration. This makes the IC an excellent pack-side fuel gauge. The IC monitors the voltage, current, temperature, and state of the battery to ensure that the lithium-ion/polymer battery is operating under safe conditions to prolong the life of the battery. Voltage of each cell of the the battery pack is measured at the CSP or GND/CELL1/CELL2/CELL3/BATTS connections. The total pack voltage is measured at BATTS and PCKP. Current is measured with an external sense resistor placed between the CSP and CSN pins. Power and average power are also reported. Up to four external NTC thermistor connections allow the IC to measure temperature of the cells in the battery pack by monitoring the TH1-4 pins. The TH1-4 pins provide an internal pullup for the thermistor that is disabled internally when temperature is not being measured. Internal die temperature of the IC is also measured and can be a proxy for the protection FET temperature if they are located close by the IC.

The IC provides programmable discharge protection for overdischarge currents (fast, medium, and slow protection), overtemperature, and undervoltage. The IC also provides programmable charge protection for overvoltage, over/undertemperature, overcharge currents (fast and slow), cell imbalance, internal self-discharge, charge done, charger communication timeout, precharge fault, and overcharge capacity fault. The IC provides a fast ideal diode discharge response that allows the battery to provide energy to the system even while the charge fault persists. The IC provides programmable charging current/voltage prescription following 6 JEITA temperature zones as well as step-charging. The IC provides additional protection to permanently disable the battery by overriding a secondary protector or blowing a fuse in severe fault conditions. This is useful when the IC has detected a primary protection FET failure and is unable to block charge/discharge any other way. The IC also modulates the CHG FET to regulate prequalification charge current until the cells cross the prequalification voltage threshold eliminating the need for external precharge circuit. Additional functionality is described in the *Protector* section.

The IC supports a low-power shutdown mode. The IC enters this low-power mode by command or if communication collapsed (if enabled). The IC wakes up from this low-power mode by communication (if battery voltage is above the undervoltage threshold), charger detection, or pushbutton/system presence wakeup (if enabled and installed). Pushbutton/system presence wakeup allows a pack to completely disconnect from a system during shipping, yet wakeup immediately upon the user pressing the button or detecting the system presence, not needing the user to plug in a charger.

The ModelGauge m5 algorithm combines the short-term accuracy and linearity of a coulomb counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. Additionally, the algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time. The IC automatically compensates for aging, temperature, and discharge rate and provides accurate state-of-charge (SOC) in milliampere-hours (mAh) or percentage (%) over a wide range of operating conditions. Fuel gauge error always converges to 0% as the cell approaches empty. Dynamic power functionality provides the instantaneous maximum battery output power which can be delivered to the system without violating the minimum system input voltage. The IC provides accurate estimation of time-to-empty and time-to-full and provides three methods for reporting the age of the battery: reduction in capacity, increase in battery resistance, and cycle odometer. In addition, age forecasting allows the user to estimate the expected lifespan of the cell.

The IC provides a configurable always-on LDO (1.8V or 3.4V) that can power small critical loads (less than 2mA) inside the battery or on the system side without overloading the cells even under fault conditions.

To prevent battery clones, the IC integrates SHA-256 authentication with a 160-bit secret key. Every IC also incorporates a 64-bit unique identification number (ROM ID). Additionally, up to 84 bytes of user memory (NVM) can be made available to store custom information.

Communication to the host occurs over a Maxim 1-Wire or standard I2C/SMBus interface. SCL/OD is an input from the host, and SDA/DQ is an open-drain I/O pin that requires an external pullup. The ALRT pin is an output that can be used as an external interrupt to the host processor if voltage, current, temperature, state-of-charge, or protection conditions (configurable) are detected. The IC offers a pushbutton feature that can be used to wake up the system after cutting power off from the system using the protection FETs, for the purpose of extending the shelf life of the battery.

For additional reference material, refer to the following Application Notes:

Application Note 7177: *MAX17320 Battery Pack Implementation Guide*

Application Note 7161: *MAX17320 Host Software Implementation Guide*

Protector

Lithium-ion/polymer batteries are very common in a wide variety of portable electronic devices because they have very high energy density, minimal memory effect and low self-discharge. However, care must be taken to avoid overheating or overcharging these batteries to prevent damage to the batteries potentially resulting in dangerous outcomes/explosive results. By operating in safe temperature ranges, at safe voltages and current levels, the overall safety of the lithium-ion/polymer batteries can be assured throughout the life of the battery.

Simple protection schemes are available to protect a battery from exceeding the safe levels. These schemes include protection for overdischarge current, short-circuit current, overcharge current, undervoltage, and overvoltage. The next level of protection offers smart protection schemes which include protection for under OCV (*SmartEmpty*), long overdischarge current, overtemperature limits for charge and discharge, undertemperature charge limits. The IC provides all of these simple and smart protection schemes with programmable thresholds and programmable timer delays for each fault.

The IC provides additional protection functionality beyond these schemes as follows:

Discharging Protection Functionality

- **Overcurrent:** (see *nODSCCfg* and *nODSCTh*)
  - **Fast Short-Circuit (70µs to 985µs):** The short-circuit hardware comparator is programmable from 5mV to 155mV with delay programmable from 70µs to 985µs.
  - **Medium (1ms to 15ms):** The overdischarge current hardware comparator is programmable from 2.5mV to 77.5mV with delay programmable from 1ms to 15ms.
  - **Slow (351ms to 35s):** Slow overdischarge protection is programmable from 0mV to 51.2mV in 0.2mV steps with delay programmable from 351ms to 35s (see *nDelayCfg* and *nIPrtTh1*).
- **Overtemperature:**
  - **Hot (OTPD—Overtemperature Discharge):** Discharge overtemperature (OTPD, see *nProtMiscTh*) is separately programmable from charge overtemperature (OTPC). OTPD is typically a higher temperature than OTPC, since charging while hot is more hazardous than discharging. OTPD is programmable in 1°C steps, with a programmable timer (see *nDelayCfg*), and is based on the hottest of the enabled thermistors.
  - **Die-Hot:** The IC measures die temperature as well as up to four thermistor temperatures. Since the IC is generally located close to the external FETs, the die temperature can indicate when the FETs are overheating. This separately programmable threshold (see *nProtMiscTh*) blocks both charging and discharging.
  - **Permanent-Fail-Hot:** When a severe overtemperature is detected, the fault is recorded into NVM and permanently disables the charge and discharge FETs and blows the three terminal fuse if enabled.
- **Undervoltage (UVP):** Undervoltage is protected by two thresholds: UVP (undervoltage protect) and UOCVP (under OCV protect—*SmartEmpty*) (see *nUVPrtTh* register for details).

Charging Protection Functionality:

- **Overvoltage (OVP):** Overvoltage protection is programmable with 10mV resolution (see *nOVPrtTh*). Temperature-region dependent OVP protection is also provided for cold/room/warm and hot temperature regions (see *nJEITAV*). OVP detection is debounced with a programmable timer (see *nDelayCfg*). An additional, higher OVP permanent failure threshold is programmable, which records any excessive OVP into NVM and permanently disables the charge and discharge FETs and blows the three terminal fuse if enabled.
- **Charge Temperature Protection:** Temperature protection thresholds are debounced with a programmable timer (see *nDelayCfg*) and are based on the hottest and coldest of the enabled thermistors.
  - **Hot (OTPC):** Charging temperature protection is programmable with 1°C resolution (see *nTPrtTh1*).
  - **Cold (UTP):** Charging is blocked at cold, programmable with 1°C resolution (see *nTPrtTh1*).

  Each threshold operates with a 1°C hysteresis.
- **Overcharge-Current Protection:**
  - **Fast:** Overcharge current is detected by a programmable hardware comparator and debounce timer between 0mV to 38.75mV and 1ms to 15ms thresholds.
  - **Slow:** A lower and slower overcharge-current protection ensures that more moderate high currents do not persist for a long time. Slow overcharge protection is programmable from 0mV to 51.2mV in 0.2mV steps, with an delay programmable between 0.35s and 35s (see *nDelayCfg* and *nIPrtTh1*). Additionally, with *nNVCfg1*.enJP = 1, this overcurrent-protection threshold is modulated according to temperature region (see *nJEITAC*).
- **Charger-Communication Timeout:** If enabled, during charging the IC turns off the charge FET if the host has stopped communicating beyond a timeout configurable from 11s to 3 minutes (see *nDelayCfg*). In systems which consult the battery for prescribing the charge current or charge voltage, especially to apply JEITA thresholds or step-charging, this feature is useful to protect against uncontrolled charging after an operating system crash or shutdown.
- **Overcharge-Capacity Fault:** If any charge session delivers more charge (coulombs) to the battery than the expected full design capacity, charging is blocked, if the feature is enabled. This threshold is programmable as a percentage (see *nProtMiscTh*.QOvflwTh) beyond the design capacity.
- **Cell Imbalance Fault:** During charging the IC monitors the individual cell voltages and, if enabled, turns off the charge FET if any cell imbalance is greater than programmable threshold (see *nBalTh*.Imbalance).

Other Faults:

- **Nonvolatile CheckSum Failure:** If enabled (*nNVCfg1*.enProtChkSm), the IC blocks charge and discharge when startup checksum of protector NVM does not match the value stored in nProtCfg2.CheckSum.

Other Protection Functionality:

- **Zero-Volt Charging:** The IC allows charging when the battery voltage is at or above 4.2V (ZVC disabled). To enable the charging of battery between 0.0V and 4.2V, ZVC must be enabled. A resistor between ZVC and PCKP is used to enable ZVC and set the maximum recovery current. See the *Zero-Volt Charging* section for more details.
- **Overdischarge-Removal Detection:** Following any overdischarge current fault, after the IC turns off the discharge FET, it tests for load removal by sourcing 30µA into PCKP. Load removal is detected when PCKP exceeds 1V. This low threshold is intentionally below the startup voltage of most ICs in order to allow active loads by external ICs while rejecting passive loads by resistors (short-circuit, failed components, etc.).
- **Charger Removal Detection:** Following any charge fault, after the IC turns off the charge FET, it measures PCKP to detect the removal of the offending charger. Charger removal is detected when PCKP falls below BATT - nOVPrtTh.ChgDetTh or whenever discharge current is detected.
- **Battery Internal Self-Discharge Detection:** The IC measures the internal self-discharge of the battery that might indicate health or safety problems. The IC alerts the system or turns off the charge and discharge FETs when a leakage is detected above the configurable threshold. See the *Battery Internal Self-Discharge* section for more details.
- **Ideal-Diode Control:** During any charge fault, the charge FET turns on when a discharge current is detected, with up to 350ms delay. This ideal diode behavior reduces the heat and voltage drop associated with the body diode during protection faults. All discharge-only faults are released when the charger is connected. See the *Charger Presence and Ideal Diode Behavior* section for more details.

Protection Fault Reporting:

- **Protection Fault Status:** Each charge and discharge fault state is latched in the *ProtStatus* register. When the fault is cleared, the corresponding bit is cleared.
- **Protection Fault Alerts:** The *ProtAlrt* register latches the status of any previous faults detected by the device. Once a fault is detected, the corresponding bit remains set until it is cleared by the host. Additionally, the *Status*.ProtAlrt bit is set when any ProtAlrt bit is set.
- **Protection Fault Logging:** The *nFaultLog* register also indicates which protection events happened during each history log period.

Charging Prescription Registers: The *ChargingVoltage* and *ChargingCurrent* registers can guide the charger according to a recommended charging profile. This can include the following knowledge which generally is associated with a particular battery and may be stored in the battery with the IC:

- **Factory Recommended Charging Current and Voltage:** This is useful when a system involves multiple battery vendors, swappable batteries, aftermarket batteries, or legacy system support.
- **Charging Modifications According to Battery Temperature:** Significantly above and below room temperature, most cell manufacturers recommend charging at reduced current and lower termination voltage to assure safety and improve lifespan. The IC modulates its guidance according to TooCold/Cold/Room/Warm/Hot/TooHot programmable temperature regions (see *nTPrtTh1*/*2*/*3*). Both charging current and voltage are modulated at Cold/Warm/Hot, targeting charge settings lower than Room (see *nJEITAV* and *nJEITAC*).
- **Step-Charging:** A common practice to balance lifespan and charge speed is to apply step-charging profiles (see the *Step-Charging* section). The IC supports three programmable steps with programmable charge currents and voltages.

At a high level, the IC protector has dual state-machines as shown in Figure 1. Each charge and discharge fault state is latched in the *ProtStatus* register, where each fault obeys a separate instance of the state machine shown in Figure 1. Any single charge fault opens the charge FET to block charge current (charge faults are OR'd together). All charge faults must be released to allow charge to resume (charge fault release conditions are AND'd together). The behavior is similar for blocking discharge.

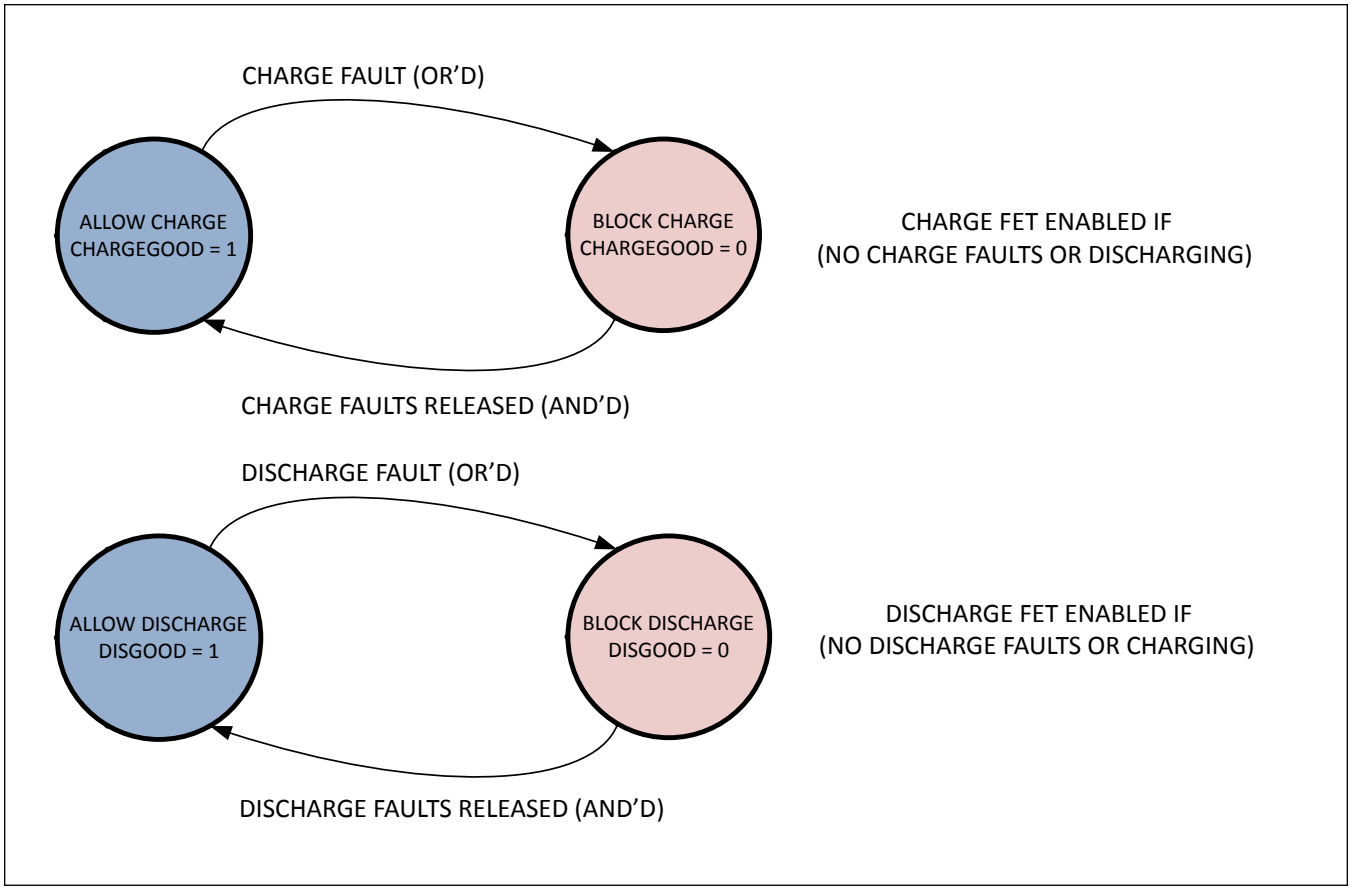


Figure 1. Simplified Protector State Machine

The IC includes a write protection and a permanent locking function. The write protection prevents accidental overwrites of protection parameters. This protection must be cleared before updating any registers and should be set after configuration changes are made. The permanent locks prevent intentional or malicious tampering, and should be enabled after development is completed and the battery pack is ready to ship in production. See the *Memory Locks and Write Protection* section for more details.

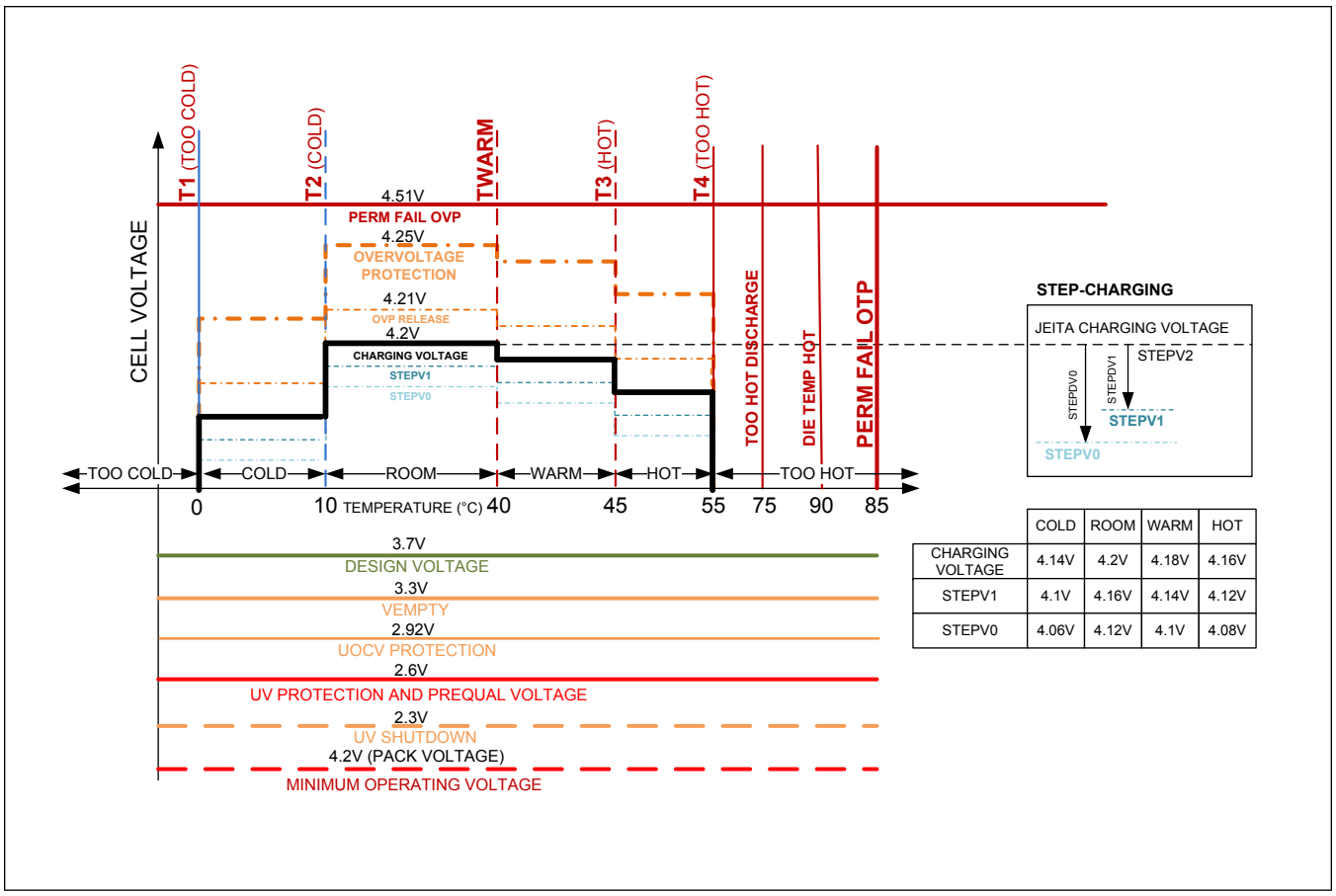
The protector registers are summarized by their protection function in Table 1 and are graphically shown across the various temperature ranges in Figure 2 and Figure 3.

Table 1. Summary of Protector Registers by Function

FUNCTION	REGISTER
Voltage Thresholds	
Permanent Fail Overvoltage Protection	*nOVPrtTh*
Overvoltage Protection	*nJEITAV*, *nOVPrtTh*
Overvoltage Protection Release	*nOVPrtTh*
UnderOCV Protection	*nUVPrtTh*
Undervoltage Protection	*nUVPrtTh*
Undervoltage Shutdown	*nUVPrtTh*
Prequal Voltage	*nChgCfg*

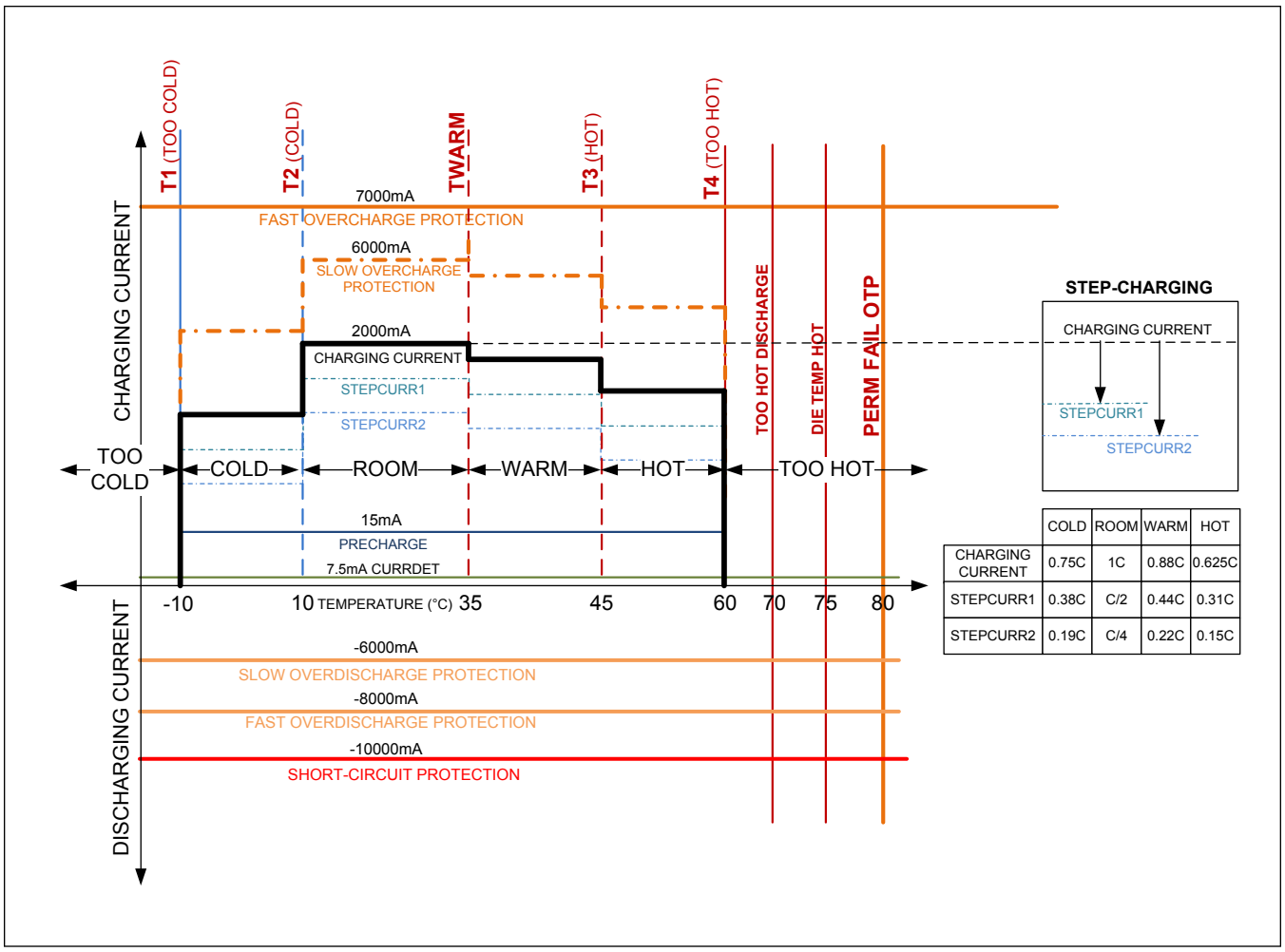
Table 1. Summary of Protector Registers by Function (continued)

Current Thresholds (See Figure 6 for timing details on current thresholds)	
Fast Overcharge Protection	*nODSCTh*, *nODSCCfg*
Slow Overcharge Protection	*nIPrtTh1*
Slow Overdischarge Protection	*nIPrtTh1*
Fast Overdischarge Protection	*nODSCTh*, *nODSCCfg*
Short-Circuit Protection	*nODSCTh*, *nODSCCfg*
Charging Detected	*nProtMiscTh*
Discharging Detected	*nProtMiscTh*
Charge Termination Current	*nIChgTerm*
Temperature Thresholds	*nTPrtTh1*, *nTPrtTh2*, *nTPrtTh3*, *nProtMiscTh*
Fault Timers	*nDelayCfg*, *nODSCCfg*
Cell Balancing Thresholds	*nBalTh*
Charging Prescription (ChargingCurrent, ChargingVoltage registers)	
Charging Voltage	*nJEITAV*
Charging Current	*nJEITAC*
Prequal Current	*nChgCfg*
Step Charging	*nStepChg*
Protection Status/Configuration	*nProtCfg*, *ProtStatus*, *nBattStatus*, *ProtAlrt*, *nFaultLog*



	COLD	ROOM	WARM	HOT
CHARGING VOLTAGE	4.14V	4.2V	4.18V	4.16V
STEPV1	4.1V	4.16V	4.14V	4.12V
STEPV0	4.06V	4.12V	4.1V	4.08V

Figure 2. Programmable Voltage Thresholds (Default Values Shown) (All Voltages are per Cell)



	COLD	ROOM	WARM	HOT
CHARGING CURRENT	0.75C	1C	0.88C	0.625C
STEPCURR1	0.38C	C/2	0.44C	0.31C
STEPCURR2	0.19C	C/4	0.22C	0.15C

Figure 3. Programmable Current Thresholds (Default Values Shown With 5mΩ Sense Resistor)

Protector Thresholds

The IC provides for a variety of programmable protector thresholds that are stored in nonvolatile memory. These thresholds are for voltage, current, temperature, and timer delays.

Voltage Thresholds

All of the voltage thresholds of the IC are shown graphically in Figure 2 and in table form with details of each threshold and the registers used to set the various thresholds in Table 2. The description of each register provides additional guidance for selection of the register value.

Table 2. Voltage Thresholds (All Voltages are per Cell)

NAME	DESCRIPTION	CONFIGURATION REGISTERS	EXAMPLE (ALL VOLTAGES ARE PER CELL)
Permanent Fail Overvoltage	Both FETs are permanently OFF after this threshold is exceeded beyond PermFailTimer. PFAIL is driven high to blow fuse if enabled.	ChargingVoltage[temp] + *nOVPrtTh*.(dOVP + OVPPermFail)	4.51V
Overvoltage (With 4 JEITA Zones)	Programmable Overvoltage at each JEITA zone. Delta V added to ChargingVoltage (nJeitaV) to set the OVP fault threshold. 10 mV step size. Protection range from 3.9V to 4.88V.	ChargingVoltage[temp] + *nOVPrtTh*.dOVP	{4.14V/4.2V/ 4.18V/4.16V} + 50mV
Overvoltage Release	Programmable release hysteresis. Fault released when VCell drops below this threshold and discharging is detected.	Overvoltage - *nOVPrtTh*.dOVPR	{4.19V/4.25V/ 4.23V/4.21V} - 10mV
ChargeVoltage-Room	ChargingVoltage output, 5mV resolution.	*nJEITAV*.Room	4.20V
ChargeVoltage-Hot	ChargingVoltage output, 10mV resolution.	*nJEITAV*.(Room - Hot)	4.16V
ChargeVoltage-Warm	ChargingVoltage output, 10mV resolution.	*nJEITAV*.(Room - Warm)	4.18V
ChargeVoltage-Cold	ChargingVoltage output, 10mV resolution.	*nJEITAV*.(Room - Cold)	4.14V
DesignVoltage	SBS Design voltage, just for information if SBS is not enabled.	*nDesignVoltage*	3.7V
EmptyVoltage	For fuel gauge only (not related to protection).	*nVEmpty*	3.0V
Under OCV Protection (SmartEmpty)	Programmable under-OCV 40mV steps UVP to UVP+1.28V.	*nUVPrtTh*.(UVP + UOCVP)	3.2V
Undervoltage Protection	Programmable undervoltage 20mV steps 2.2V to 3.46V. Gauging and communications works until undervoltage shutdown.	*nUVPrtTh*.UVP	2.7V
Undervoltage Release	Undervoltage fault persists until charger applied.		
Undervoltage Shutdown	Gauging and communications work until undervoltage shutdown.	*nUVPrtTh*.UVShdn	
Hardware Startup			Pack voltage 4.2V minimum
Zero-Voltage Charging	Enabled by populating ZVC resistor. Charging current set by resistor value.		0.0V

SmartEmpty

Standard undervoltage protection protects the cell voltage from dropping below a certain threshold to protect the battery from reaching an overdischarged state. When a lithium-ion/polymer cell stays in undervoltage state for a long time, it is important to prevent the lithium-ion/polymer cell from eventually discharging to very deep discharged states like 2.0V or even 0V. Staying in a deep-discharge state for a long time can result in a lithium-ion/polymer battery aging faster or going into a hazardous state.

Therefore, the standard objective for lithium-ion/polymer protection when overdischarged is:

> Protect from overdischarge by ensuring some small reserve capacity for long-term-storage survival after protection.

The standard protection is a voltage choice, undervoltage protection (UVP).

The load on the battery greatly influences the state corresponding with the UVP threshold. When the cell voltage reaches the UVP threshold and the protection circuit opens the discharge FET, the cell voltage relaxes to reveal the actual state of the battery as shown in Figure 4. When heavy pulsed loads are placed on the cell, the cell voltage may reach the undervoltage threshold when there is still ~15% of the battery capacity remaining which results in wasted run-time for the application. Additionally, very small loads can allow the battery to be very deeply discharged, potentially damaging the cell, before reaching the undervoltage threshold.

The IC provides SmartEmpty functionality which relies on the fuel gauge's reported state-of-charge to determine empty in the application as opposed to using the predefined UVP threshold. SmartEmpty is not influenced by the load and opens up the discharge FET when the battery reaches the empty state, as shown in Figure 5. The IC continues to protect against higher loads from dropping the cell voltage below the lowered UVP threshold, as shown in Figure 5.

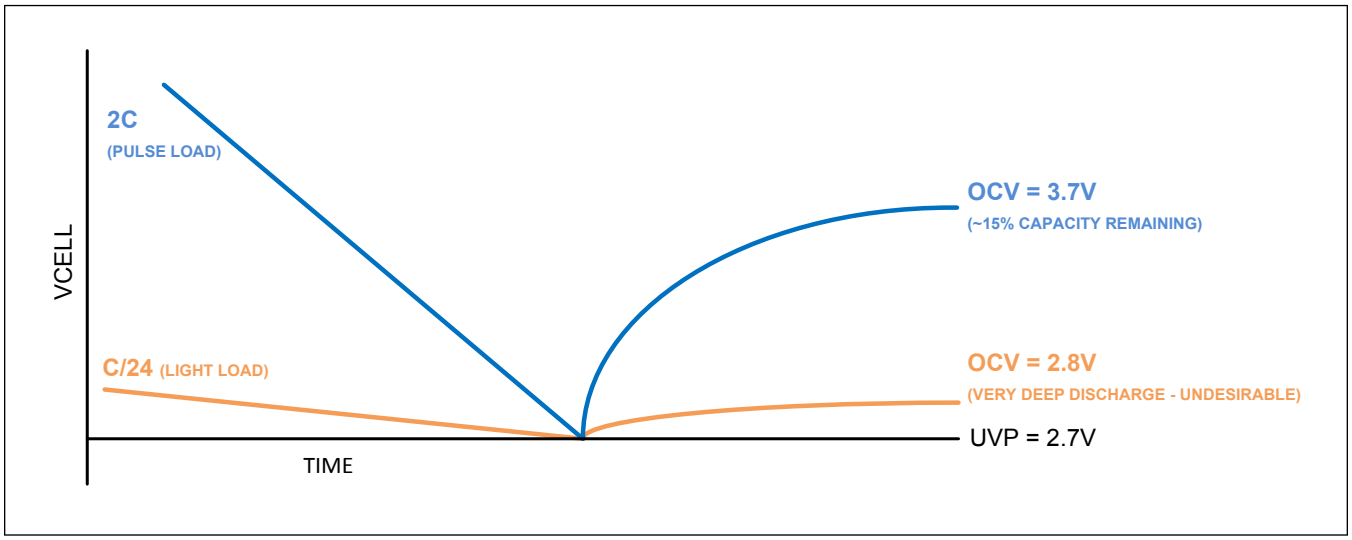


Figure 4. Standard Undervoltage Protection

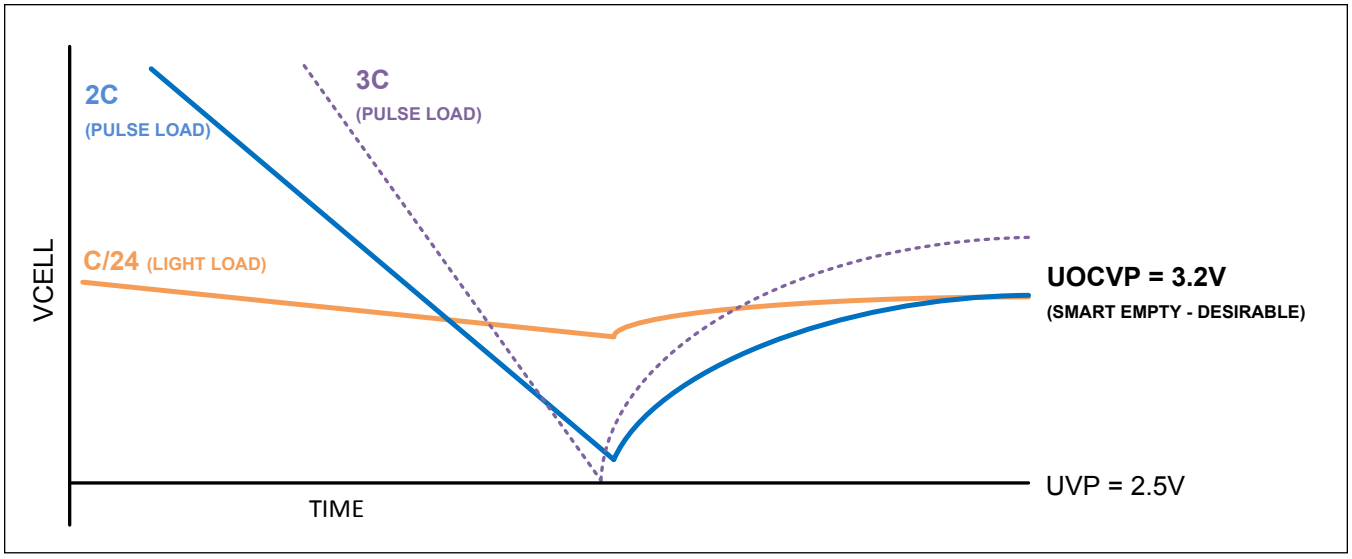


Figure 5. SmartEmpty Protection

Current Thresholds

All of the current thresholds of the IC are shown graphically in Figure 3 and in table form with details of each threshold in Table 3. The description of each register provides additional guidance for selection of the register value. See Figure 6 for timing details on current thresholds.

Table 3. Current Threshold Summary

CURRENT	ACTION	RELEASE	CONFIGURATION REGISTERS	DETAILS
Overcharge Current (fast)	CHG off	Discharging or charger removal detection	*nODSCTh*, *nODSCCfg*	Threshold 5-bit, 1.25mV steps to 38.75mV. Delay programmable 4-bit, 1ms to 15ms in 0.9ms steps.
Overcharge Current (slow with 4 JEITA zones)	CHG off		*nIPrtTh1*, *nDelayCfg*	Programmable 0.4mV steps to 51.2mV. Delay programmable 351ms to 45s. Separate thresholds for 4 out of 6 JEITA zones.
Overdischarge Current (fast)	DIS off	Charging or load removal detection	*nODSCTh*, *nODSCCfg*	5-Bit, 2.5mV steps to 77.5mV. Delay programmable 4-bit, 1ms to 15ms in 0.9ms steps.
Overdischarge Current (slow)	DIS off		*nIPrtTh1*, *nDelayCfg*	Programmable 0.4mV steps to 51.2mV. Delay programmable 351ms to 45s.
Short-Circuit Current	DIS off		*nODSCTh*, *nODSCCfg*	5-Bit, 5mV steps to 155mV. Delay programmable 4-bit, 61µs + 70µs steps to 985µs.
Charging Detected	Normal			See the *Charger Presence and Ideal Diode Behavior* section for details.
Discharging Detected	Normal			See the *Charger Presence and Ideal Diode Behavior* section for more details. When discharging is detected, overcharge current faults release. Other charge faults such as OVP, OTP, UTP remain set, however, the CHG FET turns on to prevent the heat and voltage drop associated with the ~0.6V CHG FET body diode. An OVP fault remains remembered (unreleased) until voltage falls and discharging is also detected.

Overcurrent Protection

The IC provides three levels of protection for overdischarge current events: fast, medium, and slow as shown in Figure 6. The IC also provides fast and slow levels of protection for overcharge-current protection. The fast and medium levels of protection are provided by hardware comparators and the slow levels are based on the ADC readings.

The IC maintains the protection until the source of the fault has been removed. Overcharge-protection fault releases when discharge is detected. Overdischarge current (fast or slow) or short-circuit current protection faults release when PCKP rises above 1V, while the IC applies 30µA source current test to PCKP or when charger is detected. See the *Charger Presence and Ideal Diode Behavior* section for details.

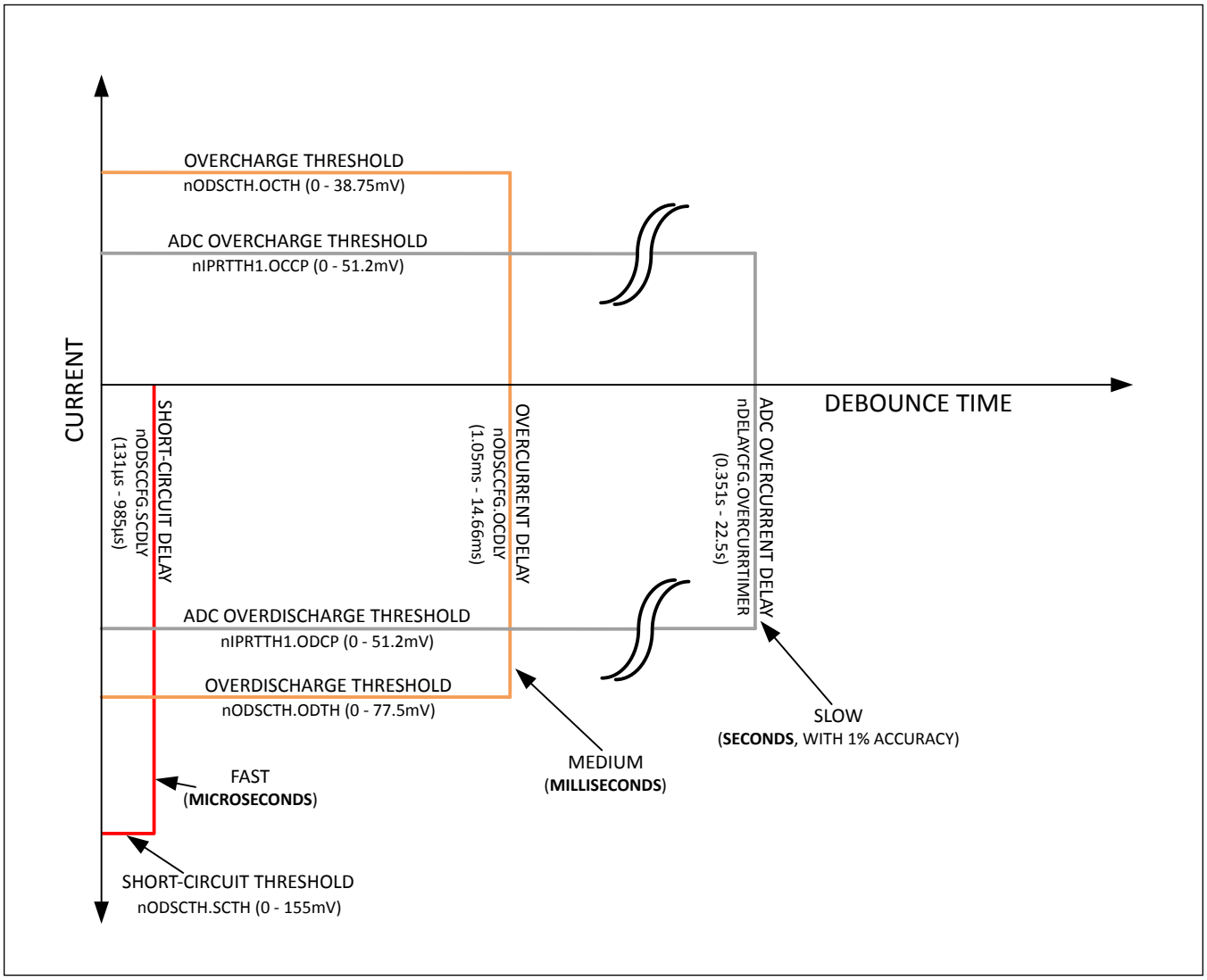


Figure 6. Fast, Medium, and Slow Overcurrent Protection

Fast Overcurrent Comparators

The IC contains three fast overcurrent comparators called Overdischarge (OD), Short-Circuit (SC), and Overcharge (OC) that allow control protection. These comparators have programmable threshold levels and programmable debounced delays. See Figure 7.

The nODSCTh register sets the threshold levels where each comparator trips. The nODSCCfg register enables each comparator and sets their debounce delays. The nODSCCfg register also maintains indicator flags of which comparator has been tripped. These register settings are maintained in nonvolatile memory if the nNVCfg1.enODSC bit is set.

Overcurrent Comparator Diagram

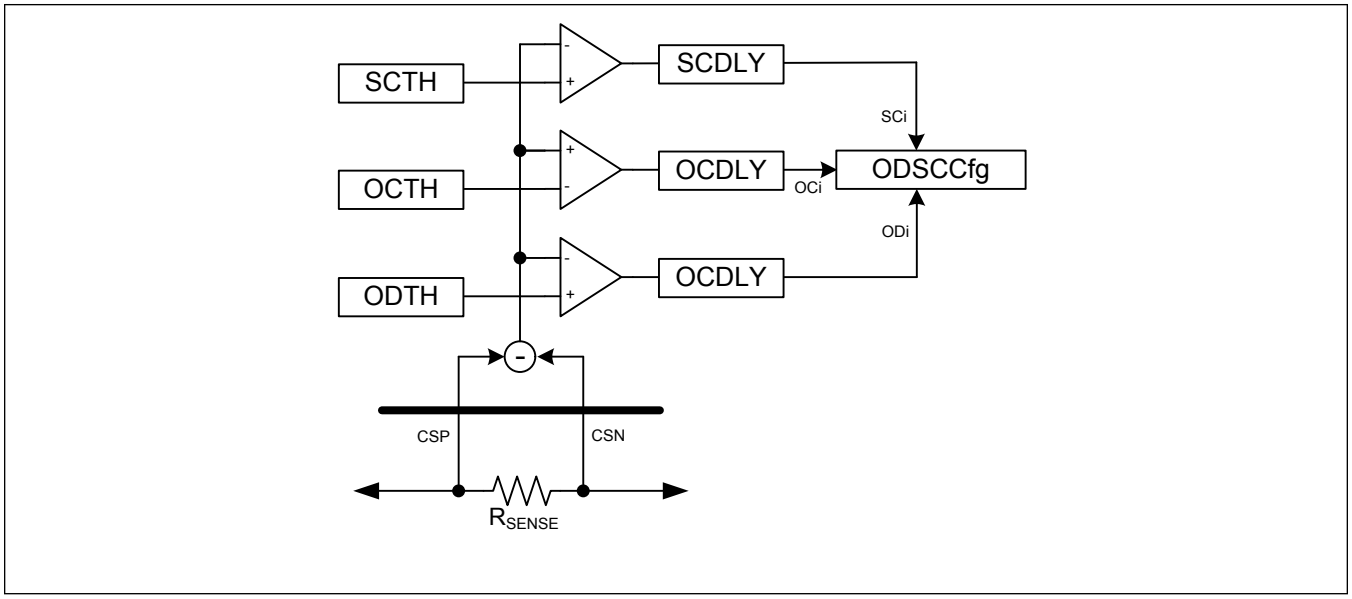


Figure 7. Overcurrent Comparator Diagram

Slow Overcurrent Protection

The IC provides programmable thresholds for the slow overdischarge-current protection (ODCP) and overcharge-current protection (OCCP). ODCP and OCCP can be configured to provide different levels of protection across the six temperature zones as shown in Figure 3. ODCP and OCCP are set in nIPrtTh1 and nJeitaC.

Temperature Thresholds

The six temperature zones shown in Figure 2 and Figure 3 can be configured in the nTPrtTh1 (Too-hot and Too-cold), nTPrtTh2 (Hot and Cold), and nTPrtTh3 (TPermFailHot and Twarm) registers.

Additional Protection Thresholds

The IC provides additional protection for suspending charge when full charge is detected or when communication with a charger has stopped as described in Table 4. The IC can also detect if the CHG FET or DIS FET has failed and alert the secondary protector to activate. Some chargers can request the desired charge voltage and charge current from the battery. The IC provides a six-zone JEITA charge prescription that can be read by the charger from the ChargeVoltage and ChargeCurrent registers.

Table 4. Additional Protection Thresholds

THRESHOLD	ACTION	CONDITIONS
Charge Suspend	CHG off	FullDet Fault—if enabled (nProtCfg.FullEn) and charge termination criteria (see *ICHGTerm* and charge termination). ChgWDT Fault—if enabled (nProtCfg.ChgWDTEn) and communications timeout.
Charge-Suspend Release	Normal	FullDet Release—Discharge or charger removal detected. ChgWDT Release—Communications or discharge or charger removal detected.
Charge FET Failure	Activate secondary protector	CHG off yet charge-current continues—if enabled (nProtCfg.PFEn and nProtCfg.FETPFEn).
Discharge FET Failure	Activate secondary protector	DIS off yet discharge-current continues—if enabled (nProtCfg.PFEn and nProtCfg.FETPFEn).
Charge Voltage/Current Prescription		Six-zone JEITA (four charge currents and voltages).
Step Charging		Two steps per JEITA zone.

Battery Internal Self-Discharge Detection (ISD)

A healthy lithium-ion/polymer battery has a very high coulombic-efficiency, typically greater than 99.9% (defined as discharge mAh vs. charge mAh). Some portion of the charge capacity can be lost by internal self-discharge. This includes natural aging, which is exacerbated if the battery stays at a high temperature and/or high state for long periods of time. However, in a damaged battery, additional capacity can be lost (unavailable for discharge), and some portion of this reflects permanent capacity loss. Unusual self-discharge in a lithium-ion/polymer battery might indicate health or safety problems.

The MAX17320 internal self-discharge (ISD) detection feature measures battery leakage and provides the following functions:

- **Leakage Measurement**. The LeakCurrRep register outputs the milliampere leakage measured across many days and multiple charge termination events.
  - Accurate leakage detection
  - Low ppm false-positive rate at a 3mA threshold
  - Detection during normal use
    - No discharge depth or duration constraints
    - Requires at least four full events, each separated by 20 hours or more
- **Leakage Log.** Leakage measurements are recorded in the battery-life-logging data. This reveals leakage vs. time for any returned battery or for managing deployed packs.
- **Leakage Alert.** If enabled, when LeakCurrRep exceeds the programmable alert threshold, an LDET alert (see ProtAlrt) is asserted.
- **Leakage Fault.** If enabled, when LeakCurrRep exceeds the programmable fault threshold, the protector disconnects the battery.

Example of Internal Self-Discharge Detection

Figure 8 shows the current leakage the MAX17320 detects as a result of placing a 909Ω resistor across a cell to emulate a battery with internal self-discharge over various temperatures.

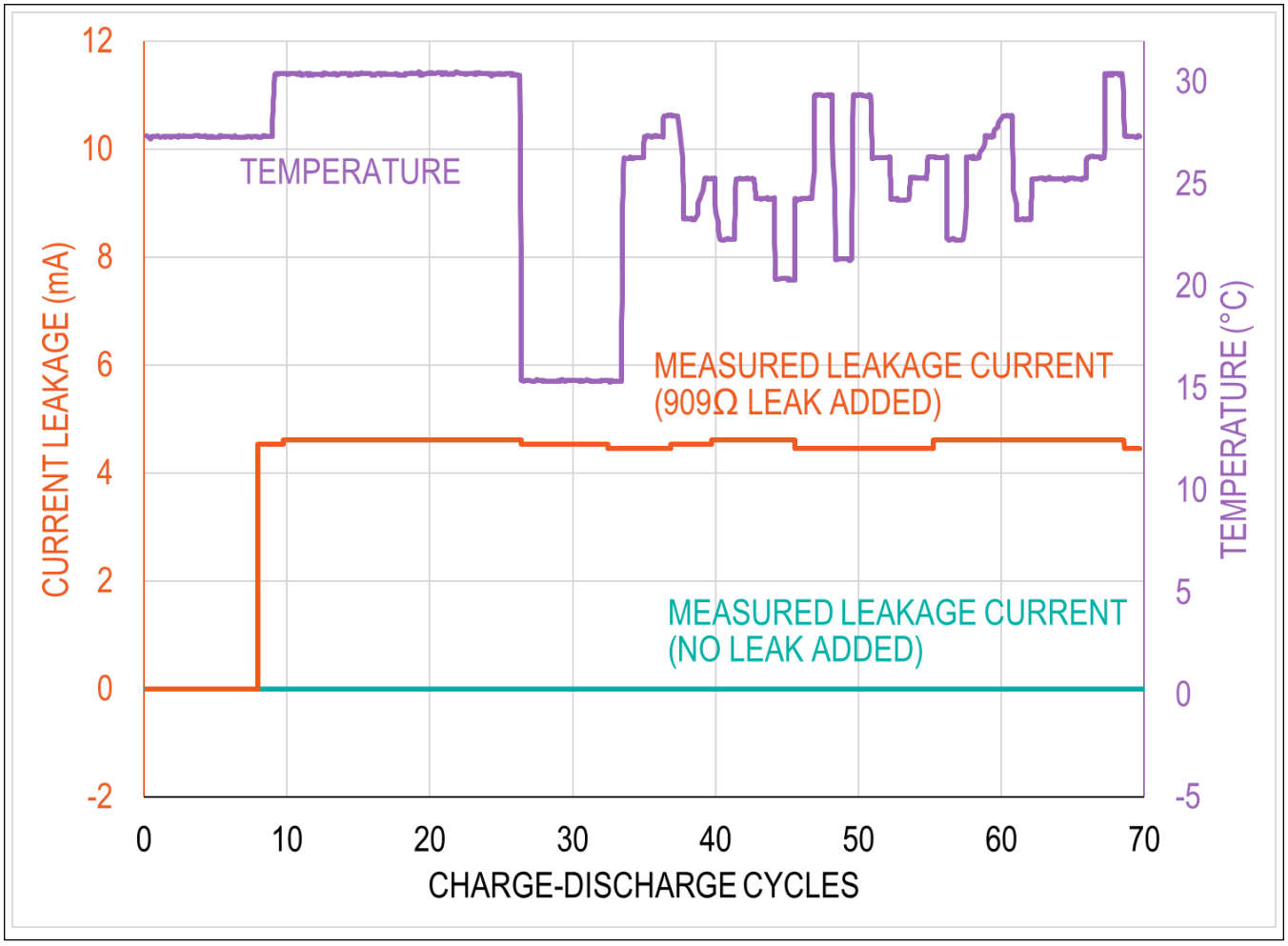


Figure 8. Example of Internal Self-Discharge with Temperature Variation

Configuring ISD

Contact Maxim for configuring the ISD Feature. See the *Battery Internal Self-Discharge Registers* section for configuration details.

Charger Presence and Ideal Diode Behavior

During a charge fault, if there is a discharge current, the current flows through the body diode of the CHG FET and potentially overheats and damages the FET. To prevent this, the IC turns on the CHG FET when discharging is detected. When a charger is detected, the CHG FET turns off again to continue protecting against the charge fault.

The IC uses several methods to detect charge and discharge to provide the following "Ideal Diode" discharge control without forgetting a possible charge fault state such as OVP, OTP, or UTP. Overcharge current is fully released during a discharge condition.

1. **Fast CHG FET On.** When discharge is detected, the CHG FET quickly turns on regardless of any charge fault condition. This limits the heat due to the CHG FET body diode conduction.
   - **Current < -CurrDet.** nProtMiscTh.CurrDet is normally configured to a setting of 2 to provide a clear threshold relative to ADC noise. With a 5mΩ sense resistor, this corresponding to 15mA, provides sufficient sensitivity for most active loads.
   - **PCKP < BATT + nOVPCfg.ChgDetTh (PCKP voltage falling only).** Additionally, a comparator detects charger removal to support better discharging detection even during small standby currents.
2. **Fast CHG FET Off.** When discharge to charge transition is detected while a charge fault (such as OTP/OVP/UTP) remains latched, the CHG FET quickly turns off to prevent charging. Since the charge fault remains remembered (not released by the discharging), the response happens quickly without waiting for the debounce timer.
3. **Slow CHG FET On.** The CHG Fet turns on when **AvgCurrent < -AvgCurrDet**. For default configuration with 5mΩ, AvgCurrDet is sensitive to 2.8mA discharge. The AvgCurrDet threshold follows the filter configuration nFilterCfg.nCurr as well as the hibernate state and configuration according to Table 5 when using default nProtMiscTh.CurrDet = 15mA.

Table 5. AvgCurrDet Threshold When Using 5mΩ and Default nProtMiscTh.CurrDet = 15mA

	AVGCURRENT FILTER CONFIGURATION (NFILTERCFG.NCURR)							
	1 (0.7s)	2 (1.4s)	3 (2.8s)	4 (5.6s)	5 (11.25s)	6 (22.5s)	7 (45s)	8 (90s)
Active (0.351s)	8.44mA	4.68mA	4.68mA	2.82mA	2.82mA	1.88mA	1.88mA	1.4mA
Hibernate (1.4s)	15.0mA	8.4mA	8.4mA	4.6mA	4.6mA	2.8mA	2.8mA	1.88mA
Hibernate (2.8s)	15.0mA	15.0mA	15.0mA	8.4mA	8.4mA	4.6mA	4.6mA	2.8mA

4. **Slow CHG FET Off. AvgCurrent > AvgCurrDet.** If the CHG FET is on for any of the above reasons, the CHG FET turns off while the charge fault persists and the average discharge current is less than AvgCurrDet.

Permanent Failure

The IC supports several types of faults which result in a permanent failure. When any enabled permanent failure is detected, both FETs turn off and remain off regardless of power-cycling. When any permanent failure fault is detected, the nBattStatus.PermFail bit is set in addition to the specific fault bit (also in nBattStatus), and both FET drivers are put in the off state. Furthermore, the PFAIL output drives high to either drive an external fuse or latch a secondary protector. This action is useful when FET failure is detected since charge and discharge can not be blocked in any other way.

The following permanent failure faults are supported whenever permanent failures are enabled (nProtCfg.PFEn = 1) and the condition persists longer than the Permanent Fail debounce timer (nDelayCfg.PermFailTimer).

- **FET Failures:** Enable/disable this feature by configuring nProtCfg.FetPFEn.
  - **DIS FET Shorted:** If discharging is detected during discharge fault, nBattStatus.DFETFs is set and written to NVM.
  - **CHG FET Shorted:** If charging is detected during charge fault, nBattStatus.CFETFs is set and written to NVM.
  - **FET Open Failure:** If either FET is detected open by the detection methods below:
    - **Detected By Discharge Fail:** If DIS = On and V_{PCKP} < 1.5V and discharge current is not detected, nBattStatus.FETFo is set and written to NVM.
    - **Detected By Charge Fail:** If CHG = On and DIS = On and V_{PCKP} > V_{BATT} + ChgDet and charge current is not detected, nBattStatus.FETFo is set and written to NVM.
- **Severe Overvoltage Failure:** If any cell voltage exceeds nOVPrtTh.OVPPermFail, nBattStatus.OVPF is set and written to NVM. Disable by configuring nOVPrtTh.OVPPermFail to the maximum value of 5.12V (FF__h).
- **Severe Overtemperature Failure:** If Temp exceeds nTPrtTh3.TpermFailHot, nBattStatus.OTPF is set and written to NVM. Disable by configuring OTPPermFail to the maximum value of 127°C (7F__h).
- **Severe Battery Internal Self-Discharge Detection:** If enabled to measure internal self-discharge and configured to be treated as a severe fault when the leakage current exceeds the fault threshold (see the *Battery Internal Self Discharge Detection Registers* for configuration details), nBattStatus.LDet is set and written to NVM.
- **Nonvolatile Protector Checksum Failure:** If enabled (nNVCfg1.enProtChkSum), during startup a checksum of the protector configuration is calculated and compared against the nChkSum register. If the value mismatches, nBattStatus.ChkSumF is set.

Charge Control

The IC provides zero-volt charging, prequalification charging and a charging prescription to instruct a charger about how to charge the battery pack.

Zero-Volt Charging

When in undervoltage-protection, the IC turns both FETs off and then enters a low quiescent state. After a long time in the undervoltage state, it is possible for the battery voltage to fall below the minimum 4.2V (pack voltage) operating voltage, making it unable to wakeup by communications or pushbutton-wakeup. In this situation, an external charge voltage must be applied to PCKP in order to wake up the IC. If enabled, the IC allows a small recovery current to gently recover the battery voltage.

The recovery current is set by the R_{ZVC} resistor between the PCKP and ZVC pins as shown in Figure 9. Zero-volt charge recovery can be disabled by depopulating the resistor. The maximum recovery current is calculated as:

$$\text{Maximum Recovery Current} = \text{VOLTAGE}_{PACK+}/(R_{ZVC} + R_{IN}).$$

When the battery is severely depleted and the IC detects that a charger has been connected, the ZVC path is enabled and the recovery current begins to flow as shown in Figure 9. The recovery current continues until the IC determines that the battery voltage has recovered enough to transfer control to the prequalification or normal charge control at which time it disconnects the ZVC path.

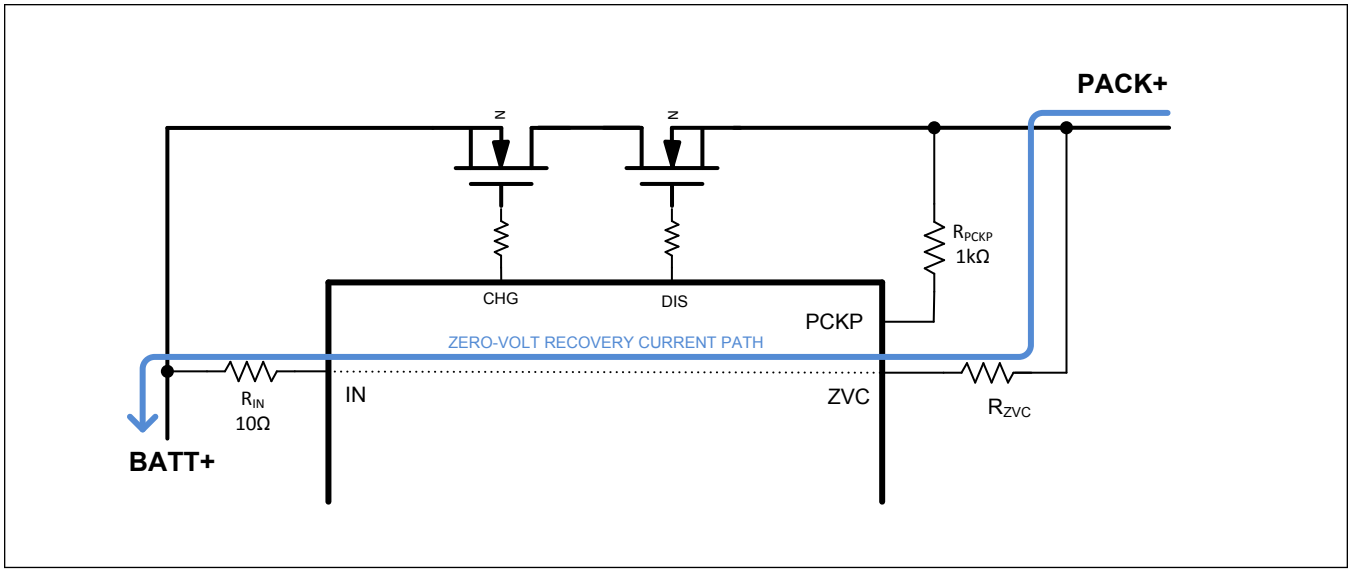


Figure 9. Zero-Volt Charge Recovery

Prequal Charging

The IC provides a prequal charge feature which modulates and reuses the charge NFET to control a limited and configurable prequal current when the battery voltage is low. This eliminates the need for a third power FET. See the *Prequal Configuration* for prequal voltage and current settings.

Charging Prescription

The IC provides appropriate charging voltage and charging current to safely charge the battery depending on the state of the battery and the temperature. The ChargingVoltage and ChargingCurrent registers provide the information according to the recommended charging based on knowledge that is installed in the battery. This information can be stored in the IC to provide the recommended charging current and voltage. This is useful when a system involves multiple battery vendors, swappable batteries, aftermarket batteries, or legacy system support.

As the temperature of the battery changes significantly above and below room temperature, most cell manufacturers recommend charging at reduced current and lower termination voltage to assure safety and improve lifespan. The IC can be configured to change its guidance according to TooCold/Cold/Room/Warm/Hot/TooHot programmable temperature zones (see *nTPrtTh1*/2/3). Both charging current and voltage are updated at Cold/Warm/Hot (see *nJEITAV* and *nJEITAC*). See Figure 2 and Figure 3.

Additionally, the IC provides a step-charging prescription to improve the lifespan of the battery and charge speed by applying a step-charging profile (see the *Step Charging* section) as shown in Figure 10.

Step Charging

A step-charging profile sets three charge voltages, three corresponding charge currents, and manages a state-machine to transition through the stages as shown in Figure 10.

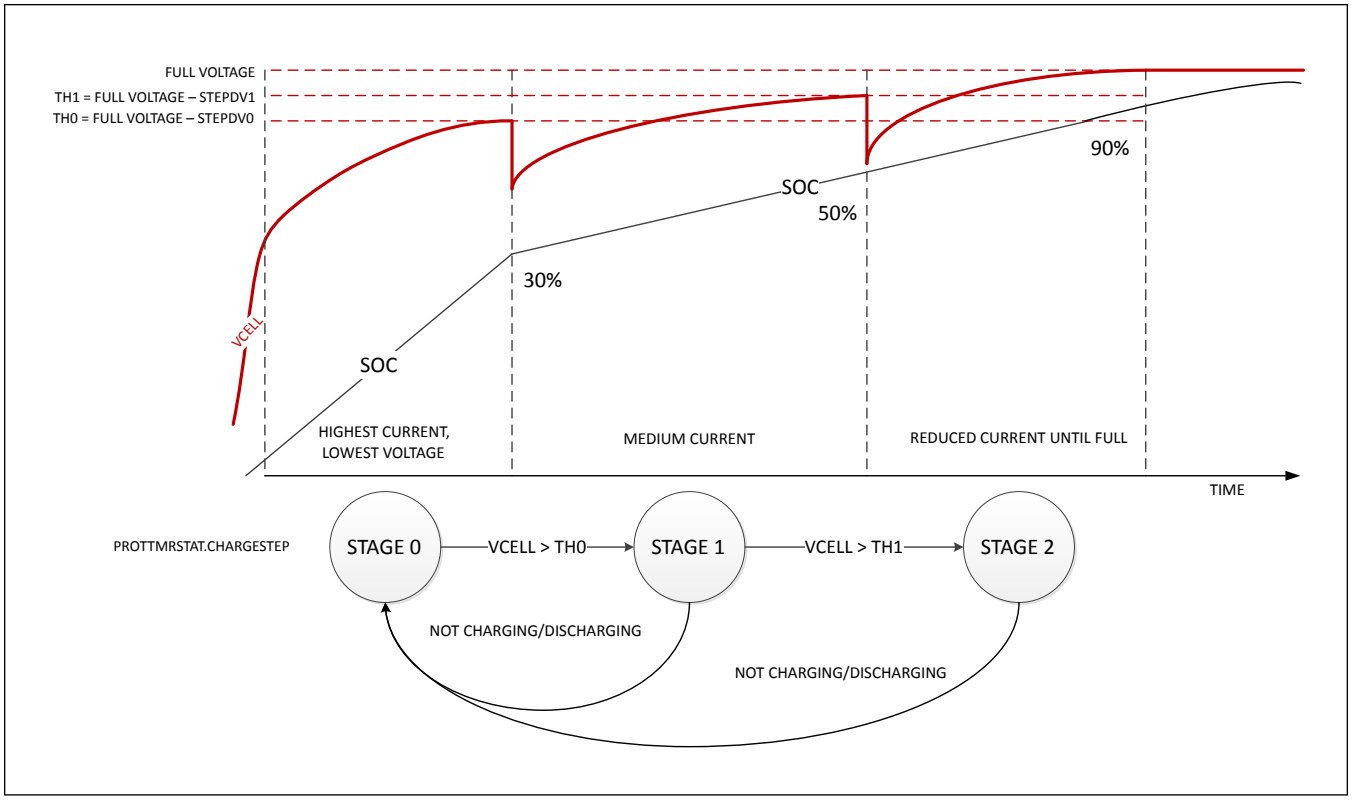


Figure 10. Step-Charging State Machine

This breaks charging into three stages:

Stage 0: Highest current, lowest voltage. ChargingCurrent comes from nJEITAC until VCell > StepVolt0. After VCell > StepVolt0, ChargingCurrent becomes defined by Stage 1.

Stage 1: Medium current. ChargingCurrent comes from nJEITAC x (StepCurr1 + 1)/16, which is a ratio from 1/16 to 16/16 until VCell > StepVolt1. When VCell > StepVolt1, ChargingCurrent becomes defined by Stage 2.

Stage 2: Reduced current until full. ChargingCurrent comes from nJEITAC x (StepCurr2 + 1)/16, which is a ratio from 1/16 to 16/16 until full.

For example, a charge may start with a ChargingCurrent of 2000mA until the cell voltage reaches 4.12V. At that point, the ChargingCurrent is reduced to 1000mA until the cell voltage reaches 4.16V. Then, the ChargingCurrent is further reduced to 500mA where it remains until the current begins to taper off naturally to the termination current.

Disabling FETs by Pin-Control or I²C Command

The IC provides FET override control by either I²C command or pin-command to the ALRT pin. This functionality can be useful for various types of applications:

- **Factory Testing.** Disconnecting the battery is useful for testing with a controlled external power supply.
- **Battery Selection.** In a multiple battery system, one battery can be disconnected and another connected by operating the FETs.
- **Ship Mode.** The last step in the battery or system factory could be to disable the FETs to disconnect power to the system to prevent the battery from draining during shipment, or when the system is in the warehouse or store shelf.

When allowed by Nonvolatile configuration, both FETs can be turned off by pin control or either FET can be individually turned off by I²C command. The control operates as follows:

- **ALRT Pin Override.** Set nProtCfg.OvrdEn = 1 and drive ALRT low to force both FETs into the off state. Releasing the ALRT line recovers the FETs according to the protector's fault state machine. Alert pin output is not functional in this mode.
- **I²C Command Override.** Set nProtCfg.CmOvrdEn = 1 and write CommStat.CHGOff or CommStat.DISOff to independently disable either the charge or discharge FET. Clearing CHGOff and DISOff recovers the FETs according to the protector's fault state machine.

These features can be disabled and locked by nonvolatile memory to prevent system code from disabling the FETs. Although disabling FETs does not produce any safety issue, it can be a nuisance if system-side software denies power to the system.

Fuel Gauge

ModelGauge m5 Algorithm

Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated, causes the reported capacity error to increase over time, and requires periodic corrections. Corrections are usually performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the true state-of-charge (SOC) based on the battery voltage after a long time of no current flow. Both have the same limitation; if the correction condition is not observed over time in the actual application, the error in the system is boundless. The performance of classic coulomb counters is dominated by the accuracy of such corrections. Voltage measurement based SOC estimation has accuracy limitations due to imperfect cell modeling, but does not accumulate offset error over time.

The IC includes an advanced voltage fuel gauge (VFG), which estimates OCV, even during current flow, and simulates the nonlinear internal dynamics of a Li+ battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC. This SOC estimation does not accumulate offset error over time. The IC performs a smart-empty-compensation algorithm that automatically compensates for the effects of temperature and load conditions to provide accurate state-of-charge information. The converge-to-empty function eliminates error toward empty state. The IC learns battery capacity over time automatically to improve long-term performance. The age information of the battery is available in the output registers.

The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a VFG. See Figure 11. The complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG while providing the strengths of both. A mixing algorithm weighs and combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state, canceling the coulomb-counter drift.

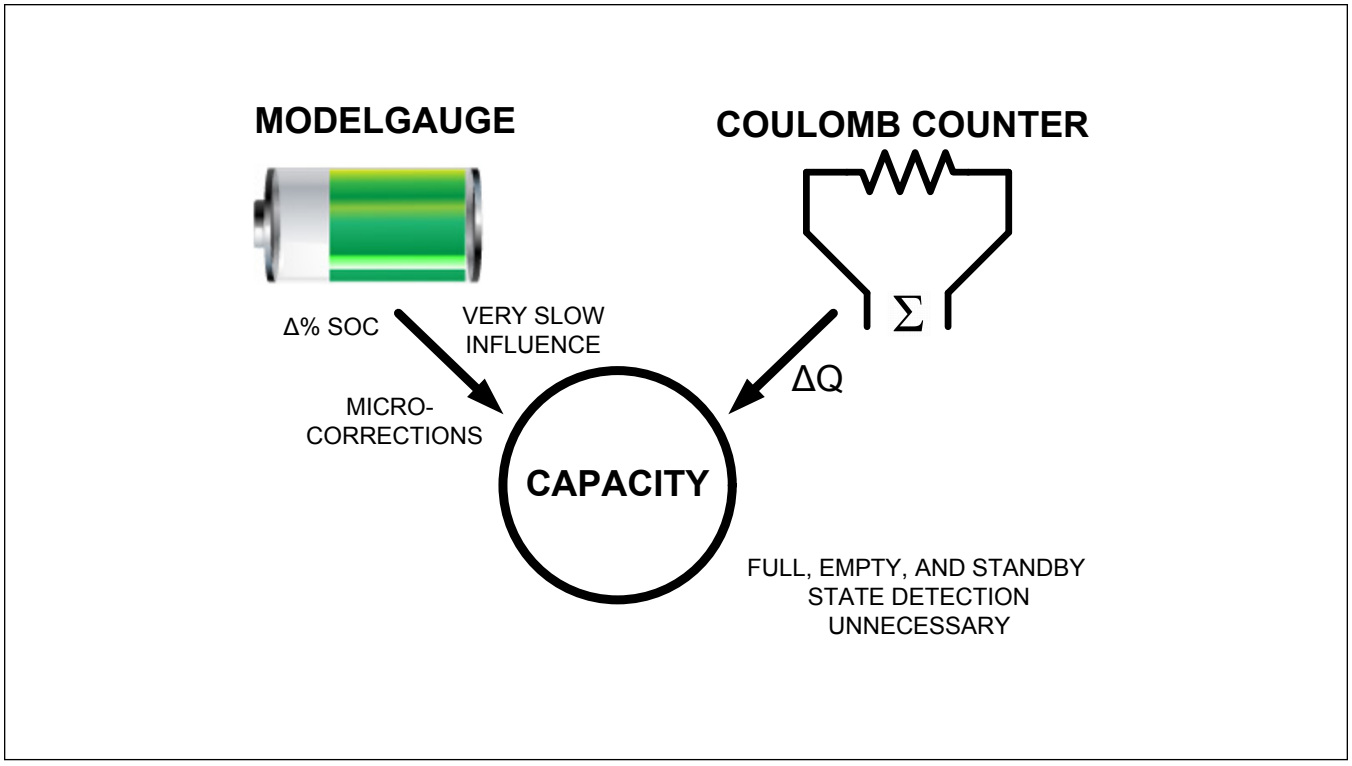


Figure 11. Merger of Coulomb Counter and Voltage-Based Fuel Gauge

The ModelGauge m5 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. As the battery approaches the critical region near empty, the ModelGauge m5 algorithm invokes a special error correction mechanism that eliminates any error.

The ModelGauge m5 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the voltage-fuel-gauge dynamics adapt based on cell-voltage behavior in the application.

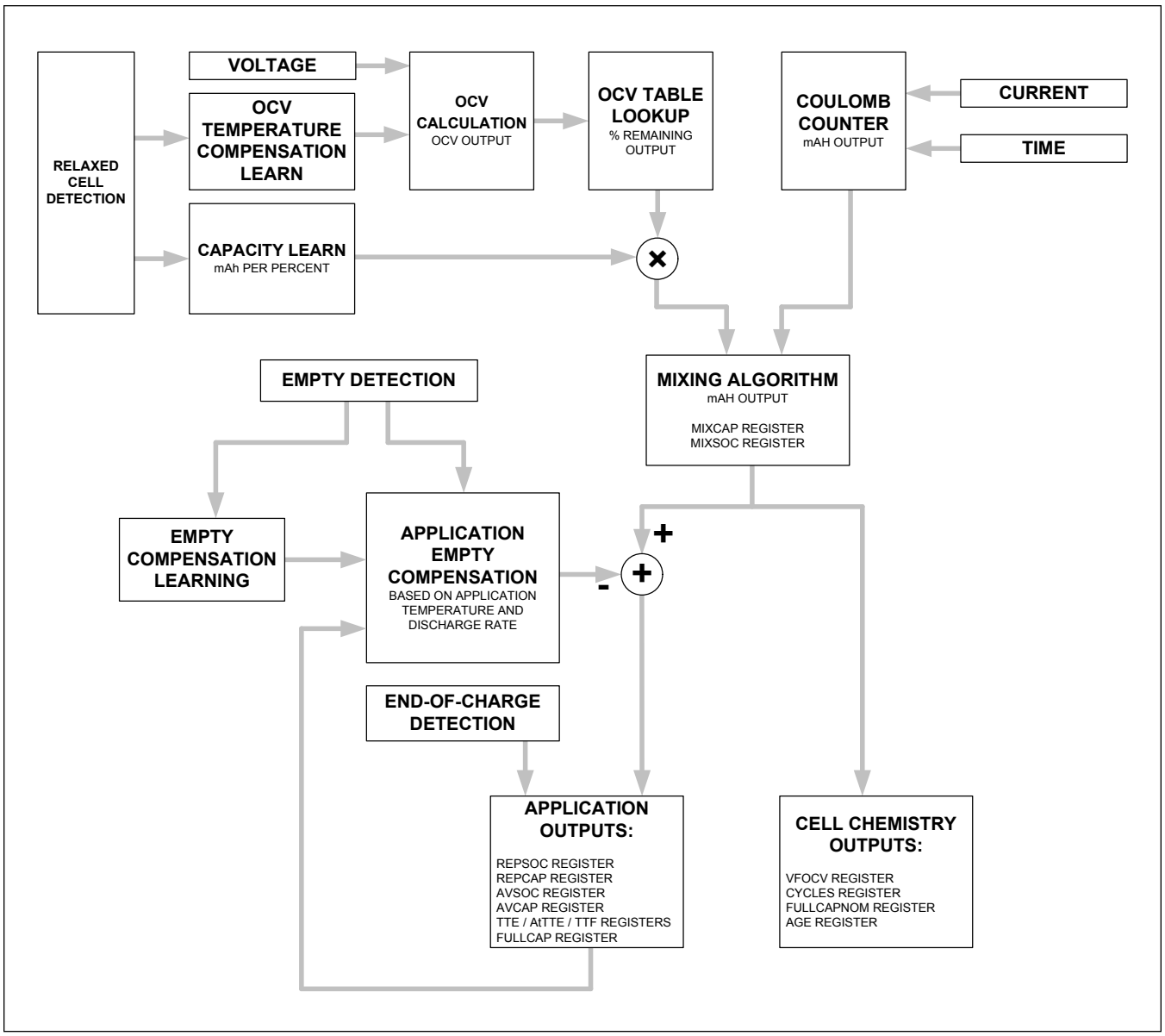


Figure 12. ModelGauge m5 Block Diagram

ModelGauge m5 EZ Performance

ModelGauge m5 EZ performance provides plug-and-play operation of the IC. While the IC can be custom tuned to the applications battery through a characterization process for ideal performance, the IC has the ability to provide reasonable performance for most applications with no custom characterization required.

While EZ performance provides reasonable performance for most cell types, some chemistries such as lithium-iron-phosphate ($LiFePO_4$) and Panasonic NCR/NCA series cells require custom characterization for best performance. EZ performance provides models for applications with empty voltages ranging from 3.0V to 3.4V through the EV kit GUI Configuration Wizard. Contact Maxim for details of the custom characterization procedure.

OCV Estimation and Coulomb Count Mixing

The core of the ModelGauge m5 algorithm is a mixing algorithm that combines the OCV state estimation with the coulomb

counter. After power-on reset of the IC, coulomb-count accuracy is unknown. The OCV state estimation is weighted heavily compared to the coulomb count output. As the cell progresses through cycles in the application, coulomb-counter accuracy improves and the mixing algorithm alters the weighting so that the coulomb-counter result is dominant. From this point forward, the IC switches to servo mixing. Servo mixing provides a fixed magnitude continuous error correction to the coulomb count, up or down, based on the direction of error from the OCV estimation. This allows differences between the coulomb count and OCV estimation to be corrected quickly. See Figure 13.

The resulting output from the mixing algorithm does not suffer accumulation drift from current measurement offset error and is more stable than a stand-alone OCV estimation algorithm. See Figure 14. Initial accuracy depends on the relaxation state of the cell. The highest initial accuracy is achieved with a fully relaxed cell.

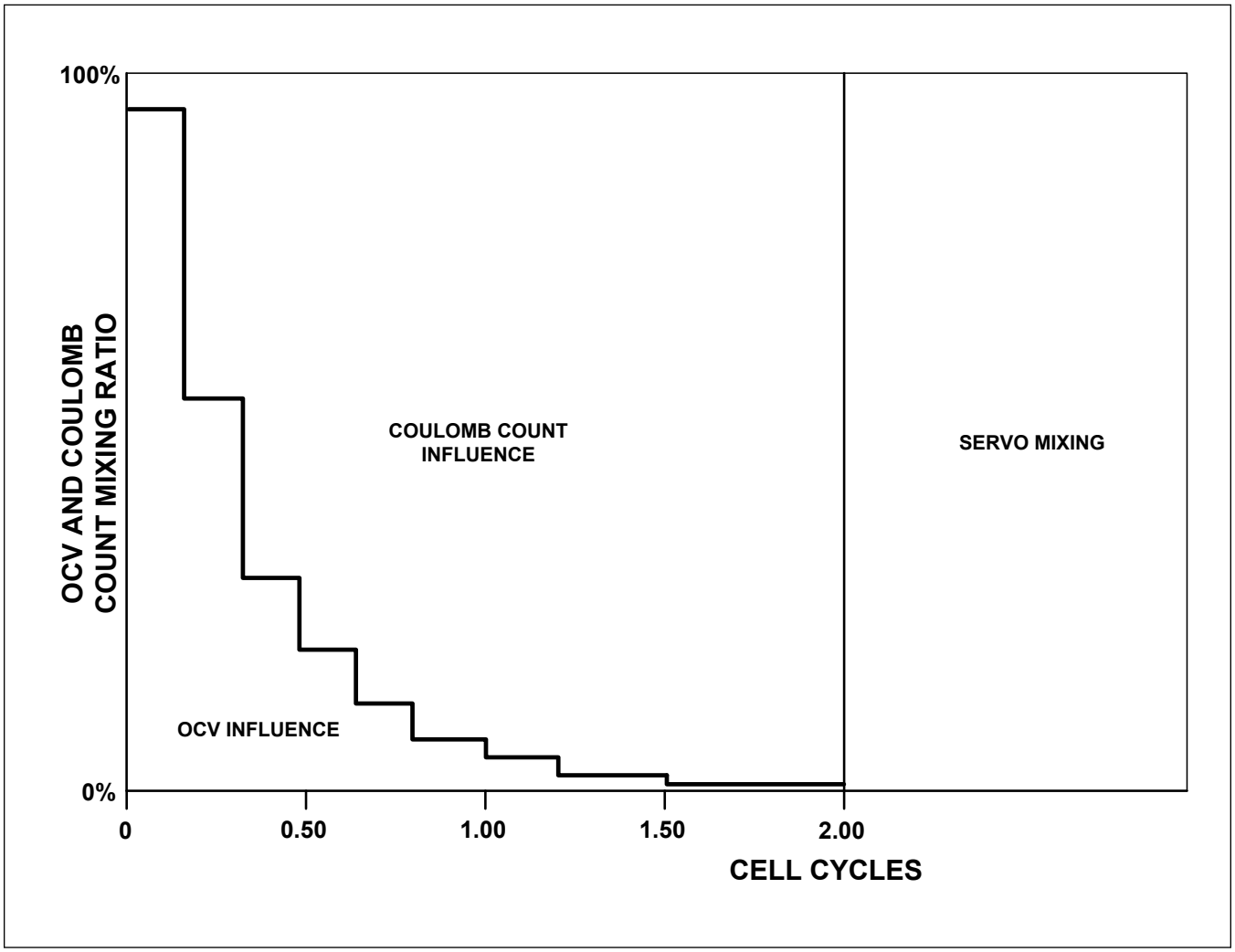


Figure 13. Voltage and Coulomb Count Mixing

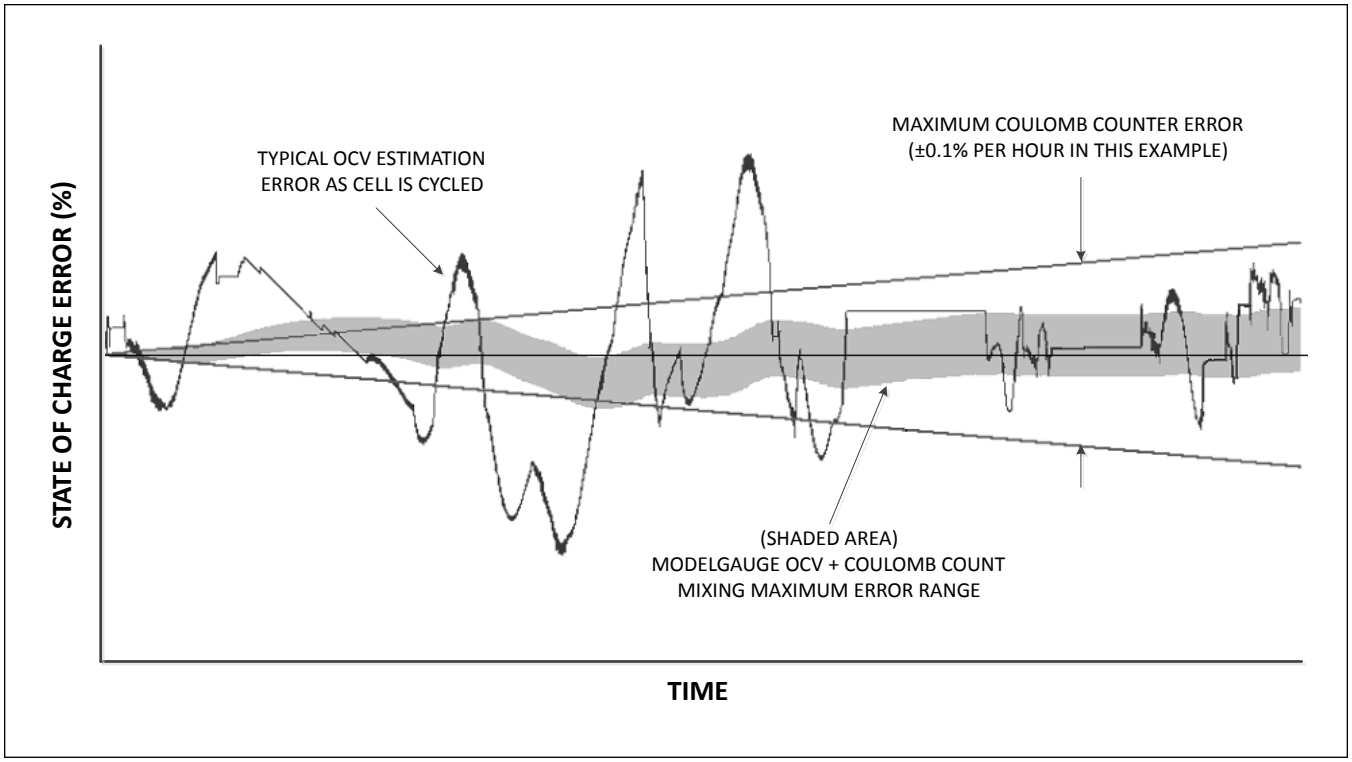


Figure 14. ModelGauge m5 Typical Accuracy Example

Empty Compensation

As the temperature and discharge rate of an application changes, the amount of charge available to the application also changes. The ModelGauge m5 algorithm distinguishes between the remaining capacity of the cell, remaining capacity of the application, and reports both results to the user.

The MixCap output register tracks the charge state of the cell. This is the theoretical mAh of charge that can be removed from the cell under ideal conditions—extremely low discharge current and independent of cell voltage. This result is not affected by application conditions such as cell impedance or minimum operating voltage of the application. ModelGauge m5 continually tracks the expected empty point of the application in mAh. This is the amount of charge that cannot be removed from the cell by the application because of the minimum voltage requirements and internal losses of the cell. The IC subtracts the amount of charge not available to the application from the MixCap register and reports the result in the AvCap register.

Since the available remaining capacity is highly dependent on the discharge rate, the AvCap register can be subject to large instantaneous changes as the application load current changes. The result can increase, even while discharging if the load current suddenly drops. This result, although correct, can be very counter-intuitive to the host software or end-user. The RepCap output register contains a filtered version of AvCap that removes any abrupt changes in remaining capacity. RepCap converges with AvCap over time to correctly predict the application empty point while discharging or the application full point while charging. Figure 15 shows the relationship of these registers.

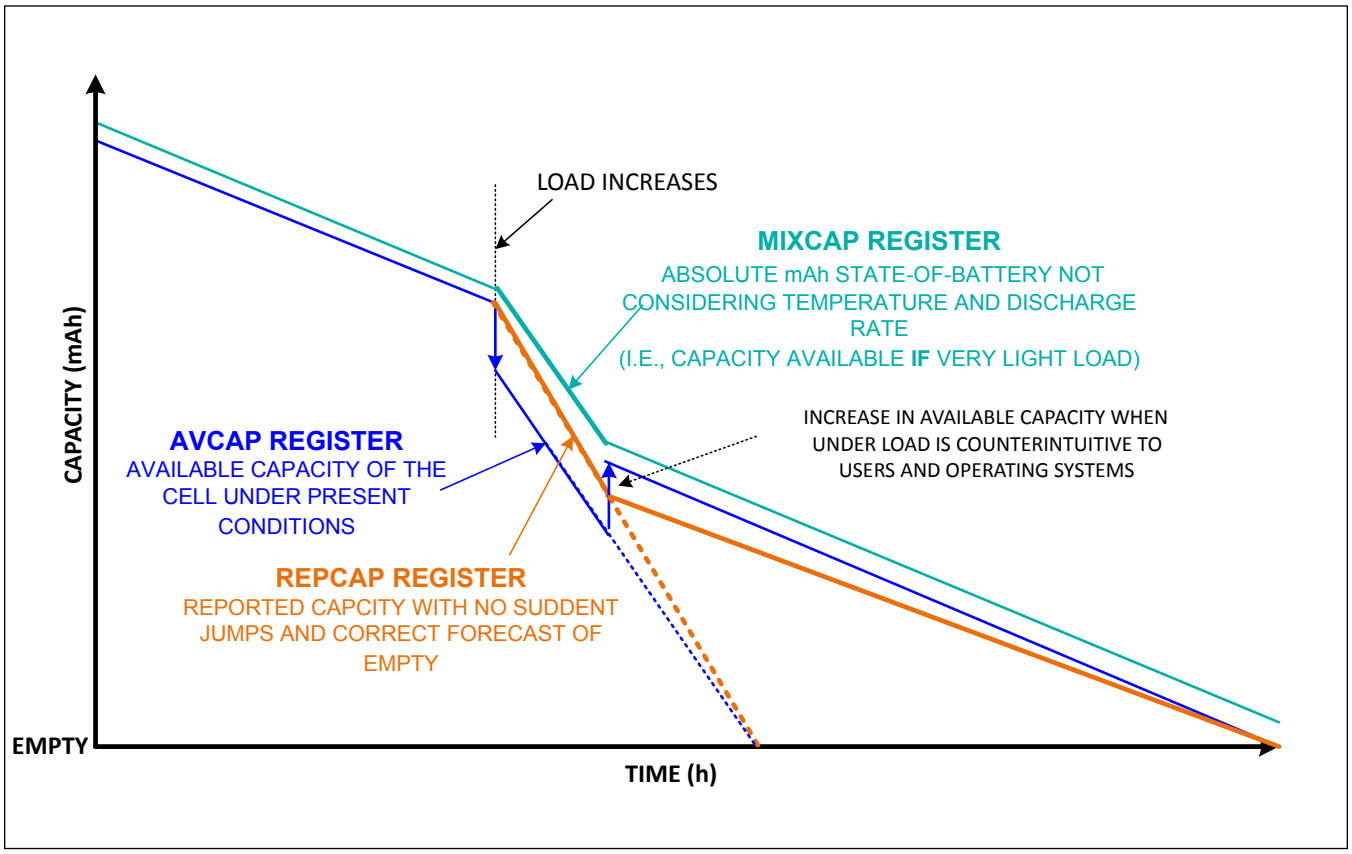


Figure 15. Handling Changes in Empty Calculation

End-of-Charge Detection

The IC detects the end of a charge cycle when the application current falls into the band set by the IChgTerm register value while the VFSOC value is above the FullSOCThr register value. By monitoring both the Current and AvgCurrent registers, the device can reject false end-of-charge events such as application load spikes or early charge-source removal. See the End-of-Charge Detection graph in the *Typical Operating Characteristics* and Figure 16. When a proper end-of-charge event is detected, the device learns a new FullCapRep register value based on the RepCap register output. If the old FullCapRep value was too high, it is adjusted on a downward slope near the end-of-charge as defined by the MiscCfg.FUS setting until it reaches RepCap. If the old FullCapRep was too low, it is adjusted upward to match RepCap. This prevents the calculated state-of-charge from ever reporting a value greater than 100%. See Figure 17.

Charge termination is detected by the IC when the following conditions are met:

- VFSOC register > FullSOCThr register
- AND IChgTerm x 0.125 < Current register < IChgTerm x 1.25
- AND IChgTerm x 0.125 < AvgCurrent register < IChgTerm x 1.25

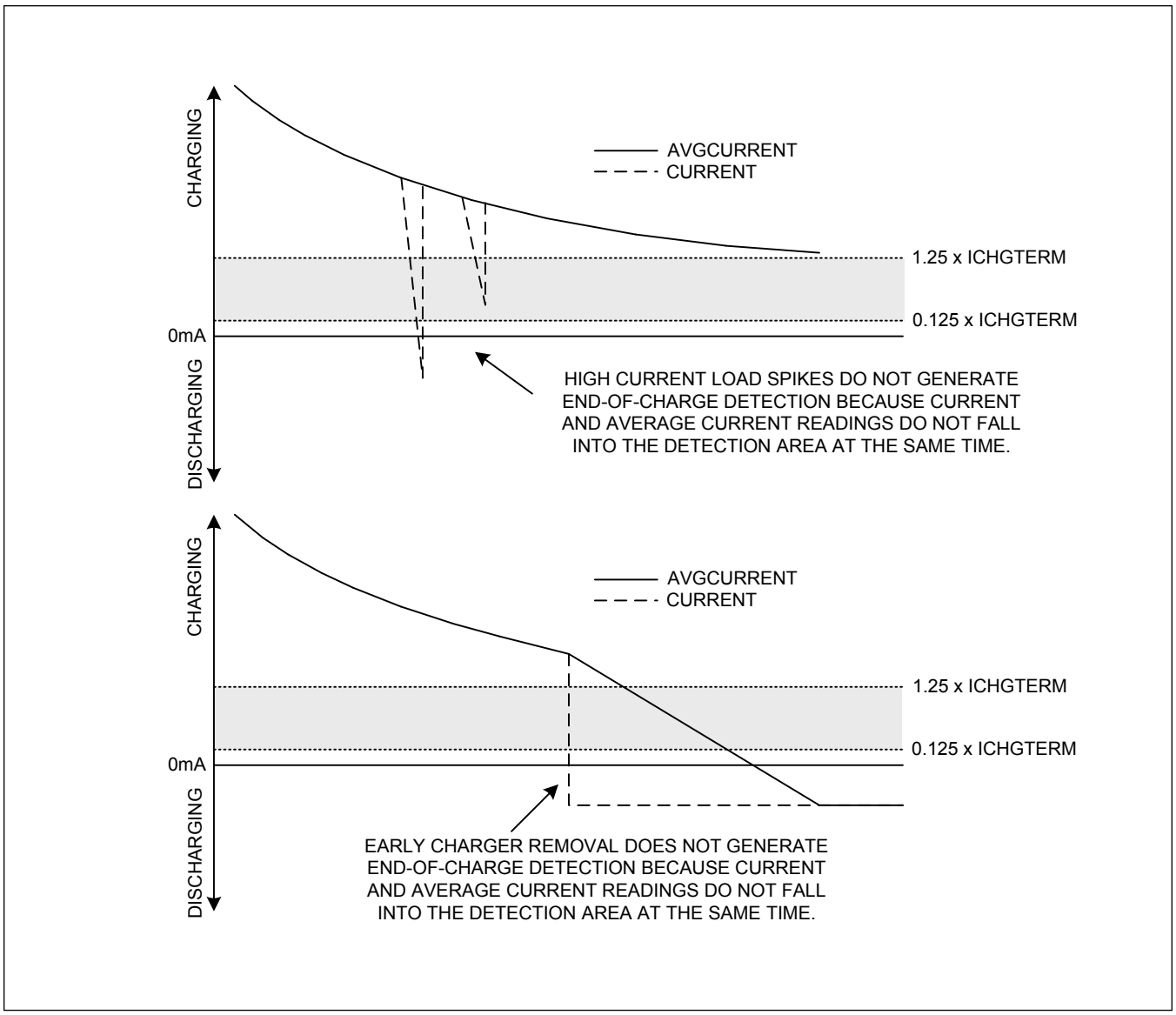


Figure 16. False End-of-Charge Events

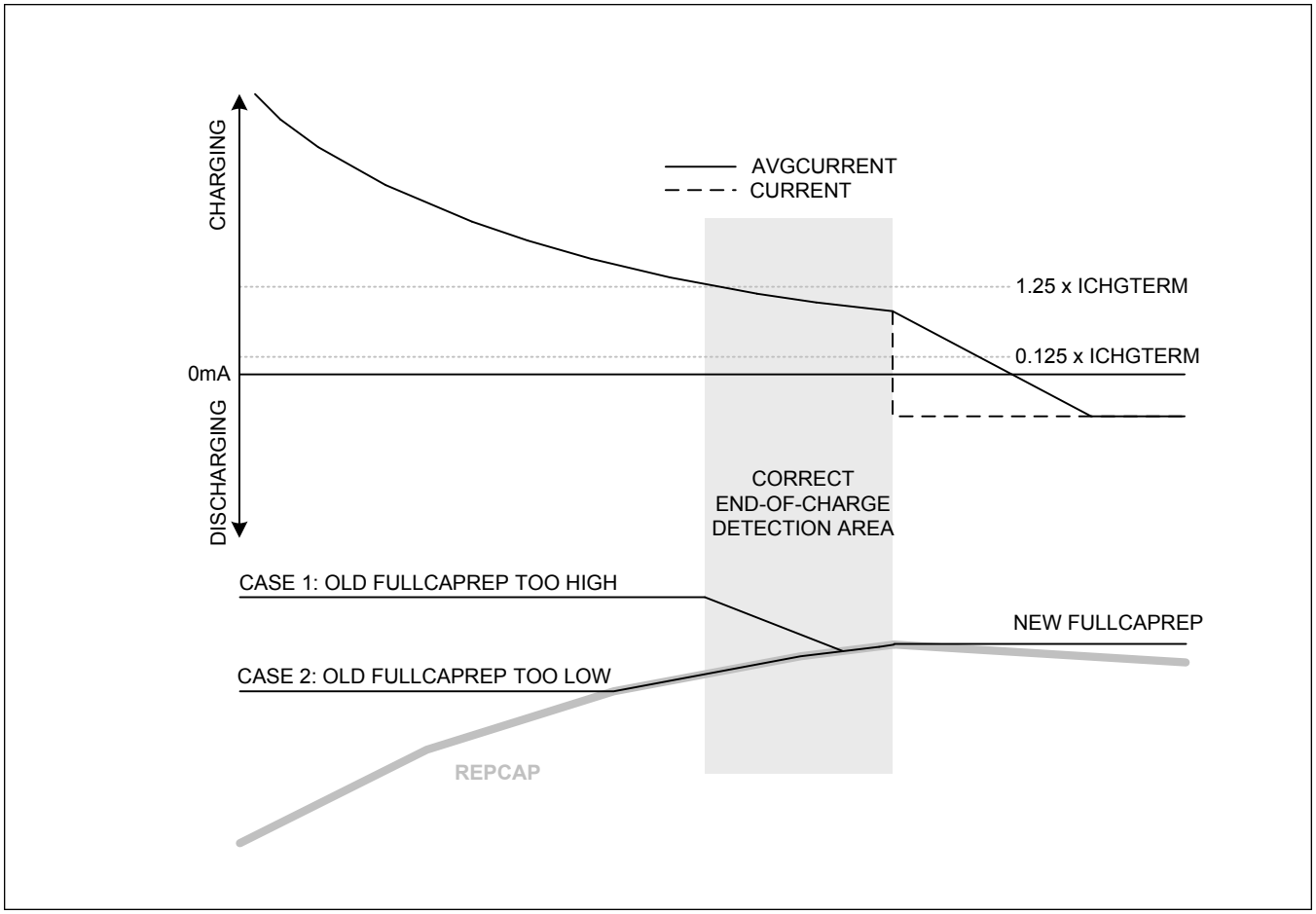


Figure 17. FullCapRep Learning at End-of-Charge

Fuel Gauge Learning

The IC periodically makes internal adjustments to cell characterization and application information to remove initial error and maintain accuracy as the cell ages. These adjustments always occur as small under-corrections to prevent instability of the system and prevent any noticeable jumps in the fuel-gauge outputs. Learning occurs automatically without any input from the host. In addition to estimating the battery's state-of-charge, the IC observes the battery's relaxation response and adjusts the dynamics of the voltage fuel gauge. Registers used by the algorithm include:

• **Application Capacity (FullCapRep Register).** This is the total capacity available to the application at full, set through the IChgTerm and FullSOCThr registers as described in the *End-of-Charge Detection* section. See the FullCapRep register description.

• **Cell Capacity (FullCapNom Register).** This is the total cell capacity at full, according to the voltage fuel gauge. This includes some capacity that is not available to the application at high loads and/or low temperatures. The IC periodically compares percent change based on an open circuit voltage measurement vs. coulomb-count change as the cell charges and discharges, maintaining an accurate estimation of the pack capacity in mAh as the pack ages. See Figure 18.

• **Voltage Fuel-Gauge Adaptation.** The IC observes the battery's relaxation response and adjusts the dynamics of the voltage fuel gauge. This adaptation adjusts the RComp0 register during qualified cell relaxation events.

• **Empty Compensation.** The IC updates internal data whenever cell empty is detected (VCell < VEmpty) to account for cell age or other cell deviations from the characterization information.

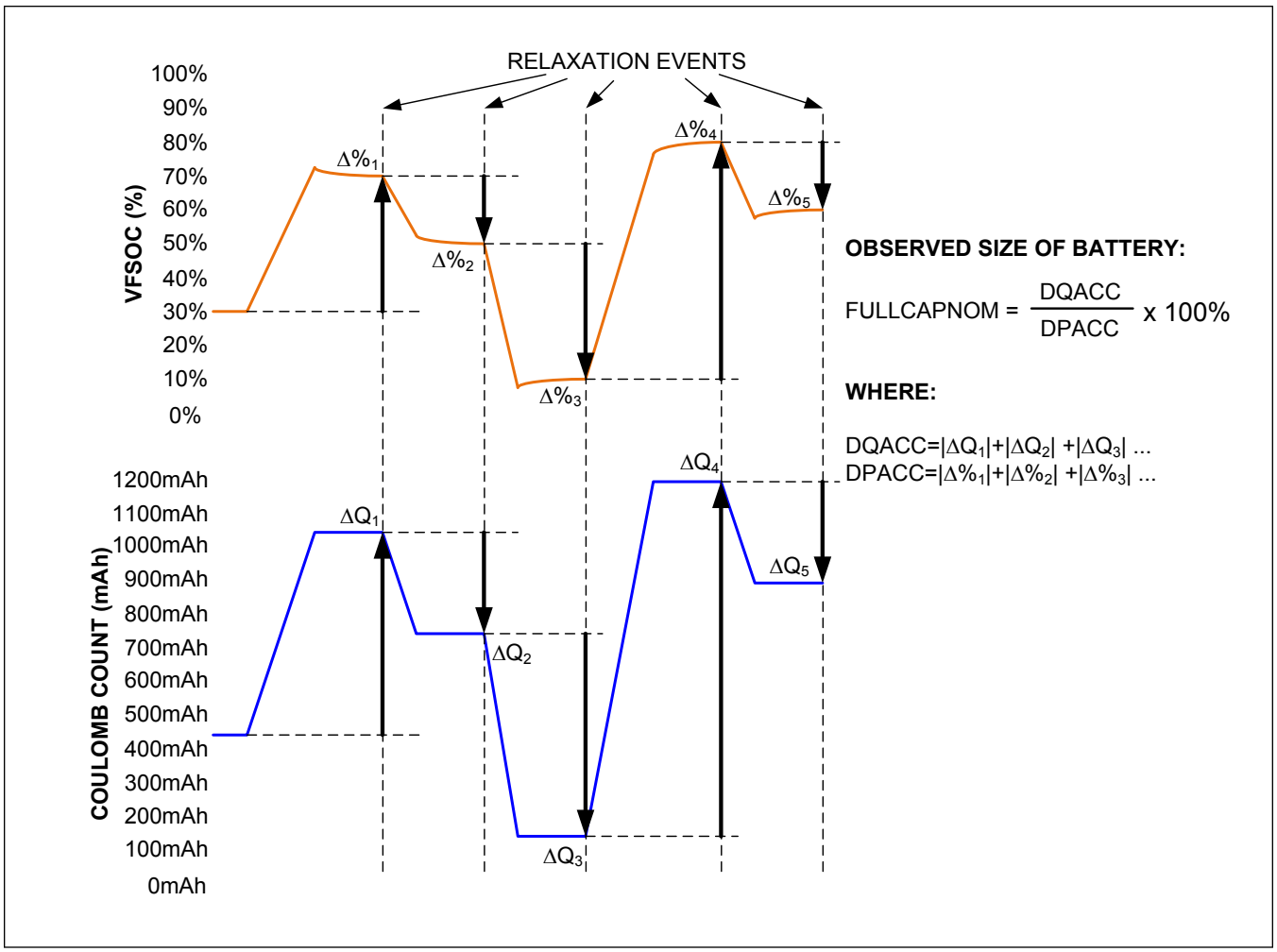


Figure 18. FullCapNom Learning

Converge-To-Empty

The IC includes a feature that guarantees the fuel gauge output converges to 0% as the cell voltage approaches the empty voltage. As the cell's voltage approaches the expected empty voltage (AvgVCell approaches VEmpty) the IC smoothly adjusts the rate of change of RepSOC so that the fuel gauge reports 0% at the exact time the cell's voltage reaches empty. This prevents minor over or under-shoots in the fuel gauge output. See Figure 19.

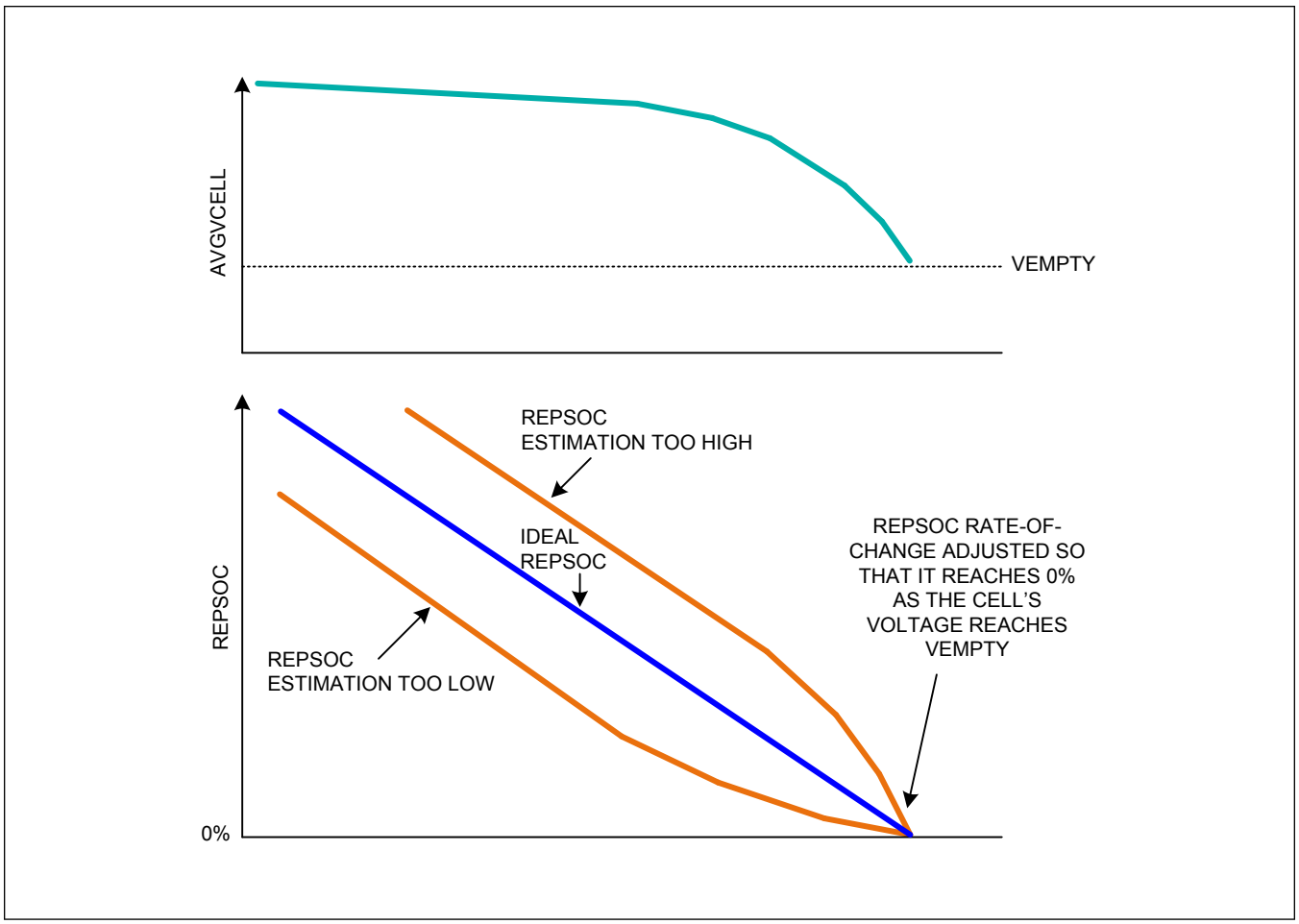


Figure 19. Converge-to-Empty

Determining Fuel-Gauge Accuracy

To determine the true accuracy of a fuel gauge, as experienced by end-users, the battery should be exercised in a dynamic manner. The end-user accuracy cannot be understood with only simple cycles. To challenge a correction-based fuel gauge, such as a coulomb counter, test the battery with partial loading sessions. For example, a typical user may operate the device for 10 minutes and then stop use for an hour or more. A robust test method includes these kinds of sessions many times at various loads, temperatures, and duration. Refer to the Application Note 4799: *Cell Characterization Procedure for a ModelGauge m3/ModelGauge m5 Fuel Gauge*.

Initial Accuracy

The IC uses the first voltage reading after power-up or after cell is connected to the IC to determine the starting output of the fuel gauge. It is assumed that the cell is fully relaxed prior to this reading; however, this is not always the case. If there is a load or charge current at this time, the initial reading is compensated using the characterized internal impedance of the cell to estimate the cell's relaxed voltage. If the cell was recently charged or discharged, the voltage measured by the IC may not represent the true state-of-charge of the cell, resulting in initial error in the fuel gauge outputs. In most cases, this error is minor and is quickly removed by the fuel-gauge algorithm during the first hour of normal operation.

Cycle+ Age Forecasting

A special feature of the ModelGauge m5 algorithm is the ability to forecast the number of cycles a user is able to get out of the cell during its lifetime. This allows an application to adjust a cell's charge profile over time to meet the cycle life requirements of the cell. See Figure 20. The algorithm monitors the change in cell capacity over time and calculates the number of cycles it takes for the cell's capacity to drop to a predefined threshold of 85% of the original. Remaining cycles below 85% of the original capacity are unpredictable and not managed by age forecasting.

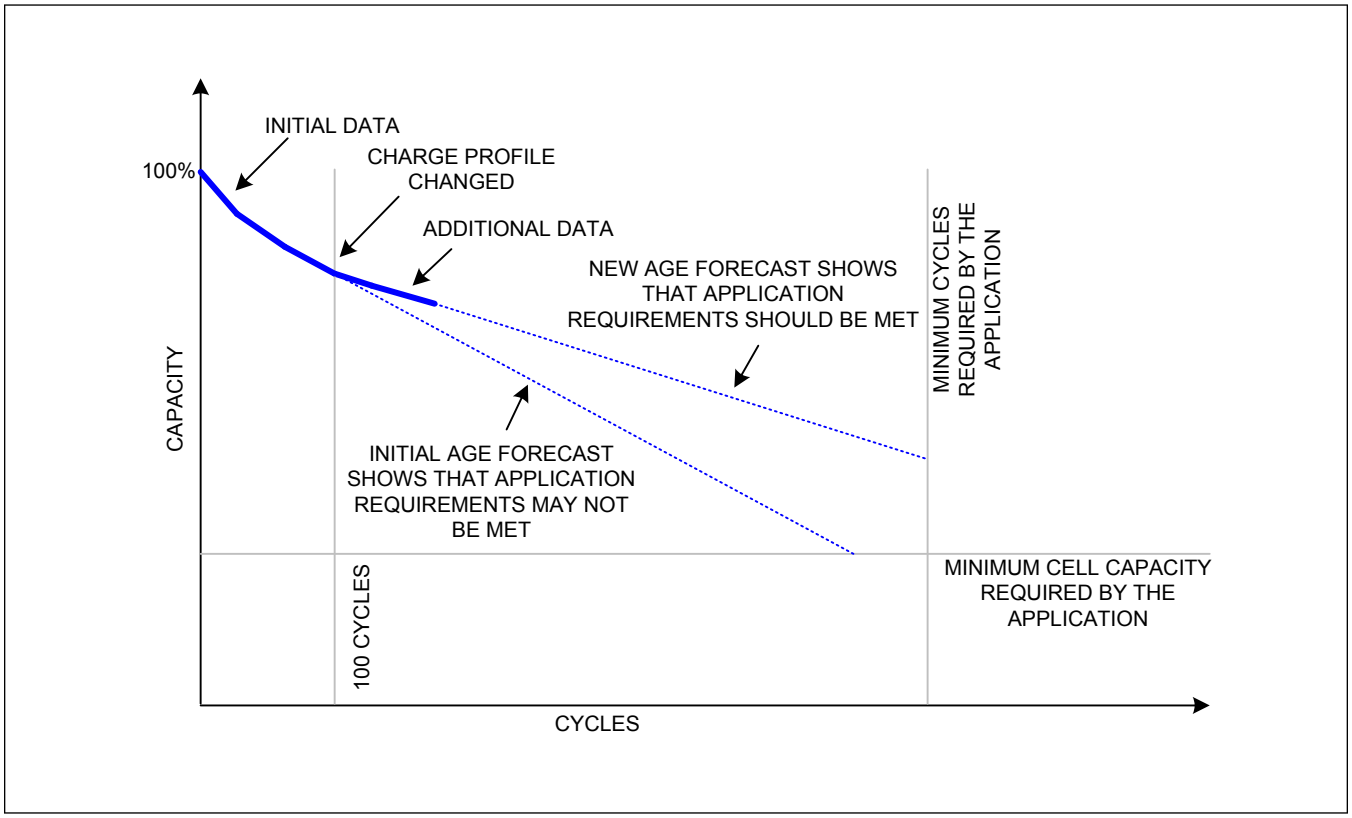


Figure 20. Benefits of Age Forecasting

nAgeFcCfg Register (1E2h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nAgeFcCfg register is used to configure the age forecasting functionality. Register data is nonvolatile and is typically configured only once during pack assembly. Table 6 shows the register format.

Table 6. nAgeFcCfg Register (1E2h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DeadTargetRatio				CycleStart							0	0	0	1	1

DeadTargetRatio: Sets the remaining percentage of initial cell capacity where the cell is considered fully aged. DeadTargetRatio can be adjusted between 75% and 86.72% with an LSb of 0.7813%. For example, if age forecasting was configured to estimate the number of cycles until the cell's capacity dropped to 85.1574% of when it was new, DeadTargetRatio should be programmed to 1101b.

CycleStart: Sets the number of cell cycles before age forecasting calculations begin. CycleStart has a range of 0.00 to 81.92 cycles with an LSb of 0.64 cycles. Since age forecasting estimation becomes more accurate over time, most applications use a default value of 30 cycles.

0: Always write this location 0.

1: Always write this location 1.

AgeForecast Register (0B9h)

Register Type: Special

Nonvolatile Backup: None

The AgeForecast register displays the estimated cycle life of the application cell. The AgeForecast value should be compared against the Cycles (017h) register to determine the estimated number of remaining cell cycles. This is accomplished by accumulating the capacity loss per cycle as the cell ages. The result becomes more accurate with each cycle measured. The AgeForecast register has a full range of 0 cycles to 16383 cycles with a 25% LSb. This register is recalculated from learned information at power-up.

Age Forecasting Requirements

There are several requirements for proper operation of the age forecasting feature as follows:

1. There is a minimum and maximum cell size that the age forecasting algorithm can handle. Table 7 shows the allowable range of cell sizes that can be accurately age forecasted depending on the size of the sense resistor used in the application. Note this range is different from the current and capacity measurement range for a given sense resistor. See the *Current Measurement* section for details.

2. Age forecasting requires a minimum of 100 cycles before achieving reasonable predictions. Ignore the age forecasting output until then.

3. Age forecasting requires a custom characterized battery model to be used by the IC. Age forecasting is not valid when using the default model.

Table 7. Minimum and Maximum Cell Sizes for Age Forecasting

SENSE RESISTOR (Ω)	MINIMUM CELL SIZE FOR FORECASTING (mAH)	MAXIMUM CELL SIZE FOR FORECASTING (mAH)
0.005	1600	5000
0.010	800	2500
0.020	400	1250

Enabling Age Forecasting

The following steps are required to enable the age forecasting feature:

1. Set nNVCfg2.enVT = 0. This function conflicts with age forecasting and must be disabled.

2. Set nFullCapFlt to the value of nFullCapNom.

3. Set nVoltTemp to 0001h.

4. Set nNVCfg0.enAF = 1 to begin operation.

Battery Life Logging

The IC has the ability to log learned battery information providing the host with a history of conditions experienced by the cell pack over its lifetime. The IC can store up to 100 snapshots of page 1Ah in nonvolatile memory. Individual registers from page 1Ah are summarized in Table 8. Their nonvolatile backup must be enabled and LOCK1 unlocked in order for logging to occur. See each register's detailed description in other sections of this data sheet. The logging rate follows the "Fibonacci Saving" interval to provide recurring log-saving according to the expected battery lifespan and is configured as shown in Table 99. See the *100 Record Life Logging* section for more details.

Table 8. Life Logging Register Summary

REGISTER ADDRESS	REGISTER NAME	FUNCTION
1A0h	nQRTable00	Learned characterization information used to determine when the cell pack is empty under application conditions.
1A1h	nQRTable10	
1A2h	nQRTable20	
1A3h	nQRTable30	
1A4h	nCycles	Total number of equivalent full cycles seen by the cell since assembly.
1A5h	nFullCapNom	Calculated capacity of the cell independent of application conditions.
1A6h	nRComp0	Learned characterization information related to the voltage fuel gauge.
1A7h	nTempCo	
1A8h	nBattStatus	Contains the permanent battery status information and, if enabled, the leakage current.
1A9h	nFullCapRep	Calculated capacity of the cell under present application conditions.
1AAh	nVoltTemp	The average voltage and temperature seen by the IC at the instance of learned data backup. If Age Forecasting is enabled, this register contains different information.
1ABh	nMaxMinCurr	Maximum and minimum current, voltage, and temperature seen by the IC during this logging window.
1ACh	nMaxMinVolt	
1ADh	nMaxMinTemp	
1AEh	nFaultLog	If Fault Logging is enabled, this register indicates which protection events happened during each history log period. If Age Forecasting is enabled, this register contains a highly filtered nFullCapNom.
1AFh	nTimerH	Total elapsed time since cell pack assembly not including time spent in shutdown mode.

Life Logging Data Example

Figure 21 shows a graphical representation of sample history data read from an IC. Analysis of this data can provide information about cell performance over its lifetime as well as to detect any application anomalies that may have affected performance.

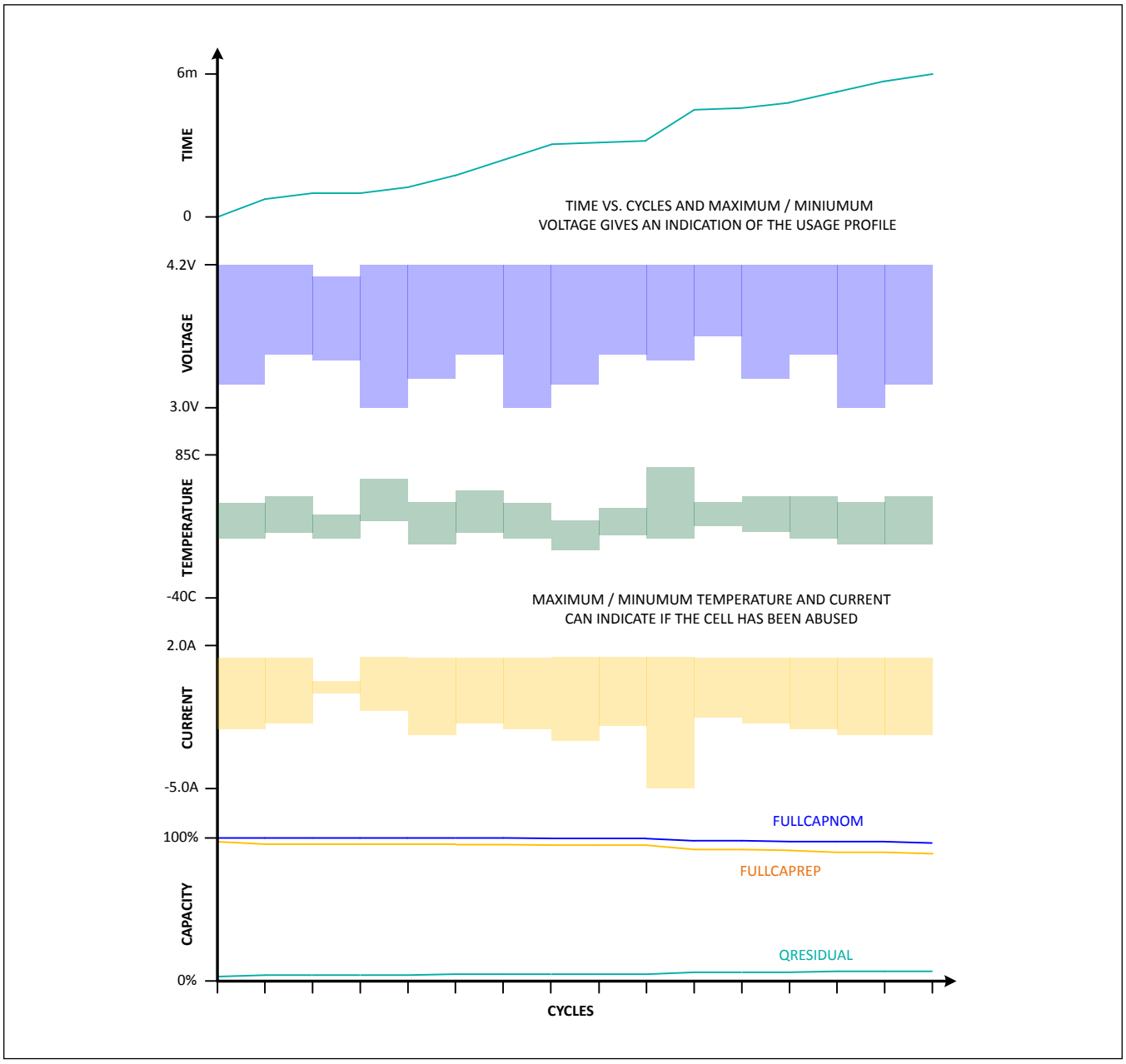


Figure 21. Sample Life Logging Data

Determining Number of Valid Logging Entries

While logging data, the IC begins on history page 1 and continues until all history memory has been used at page 100. Prior to reading history information out of the IC, the host must determine which history pages has been written and which, if any, had write errors and should be ignored. Each page of history information has two associated write flags that indicate if the page has been written and two associated valid flags which indicate if the write was successful. The HISTORY RECALL command [E2XXh] is used to load the history flags into page 1Fh of IC memory where the host can then read their state. Table 9 shows which command and which page 1Fh address has the flag information for a given history page. For example, to see the write flag information of history pages 1-8, send the E29Ch command then read address 1F2h. To see the valid flag information of pages 1-8, send the E29Ch command and then read address 1FFh.

Table 9. Reading History Page Flags

ASSOCIATED HISTORY PAGES	COMMAND TO RECALL WRITE FLAGS	WRITE FLAG ADDRESS	COMMAND TO RECALL VALID FLAGS	VALID FLAG ADDRESS
1-8	E29Ch	1F2h	E29Ch	1FFh
9-16		1F3h	E29Dh	1F0h
17-24		1F4h		1F1h
25-32		1F5h		1F2h
33-40		1F6h		1F3h
41-48		1F7h		1F4h
49-56		1F8h		1F5h
57-64		1F9h		1F6h
65-72		1FAh		1F7h
73-80		1FBh		1F8h
81-88		1FCh		1F9h
89-96		1FDh		1FAh
97-100		1FEh		1FBh

Once the write flag and valid flag information are read from the IC, it must be decoded. Each register holds two flags for a given history page. Figure 22 shows the register format. The flags for a given history page are always spaced 8-bits apart from one another. For example, history page 1 flags are always located at bit positions D0 and D8, history page 84 flags are at locations D3 and D11, etc. Note that the last flag register contains information for only 3 pages, in this case, the upper 5-bits of each byte should be ignored.

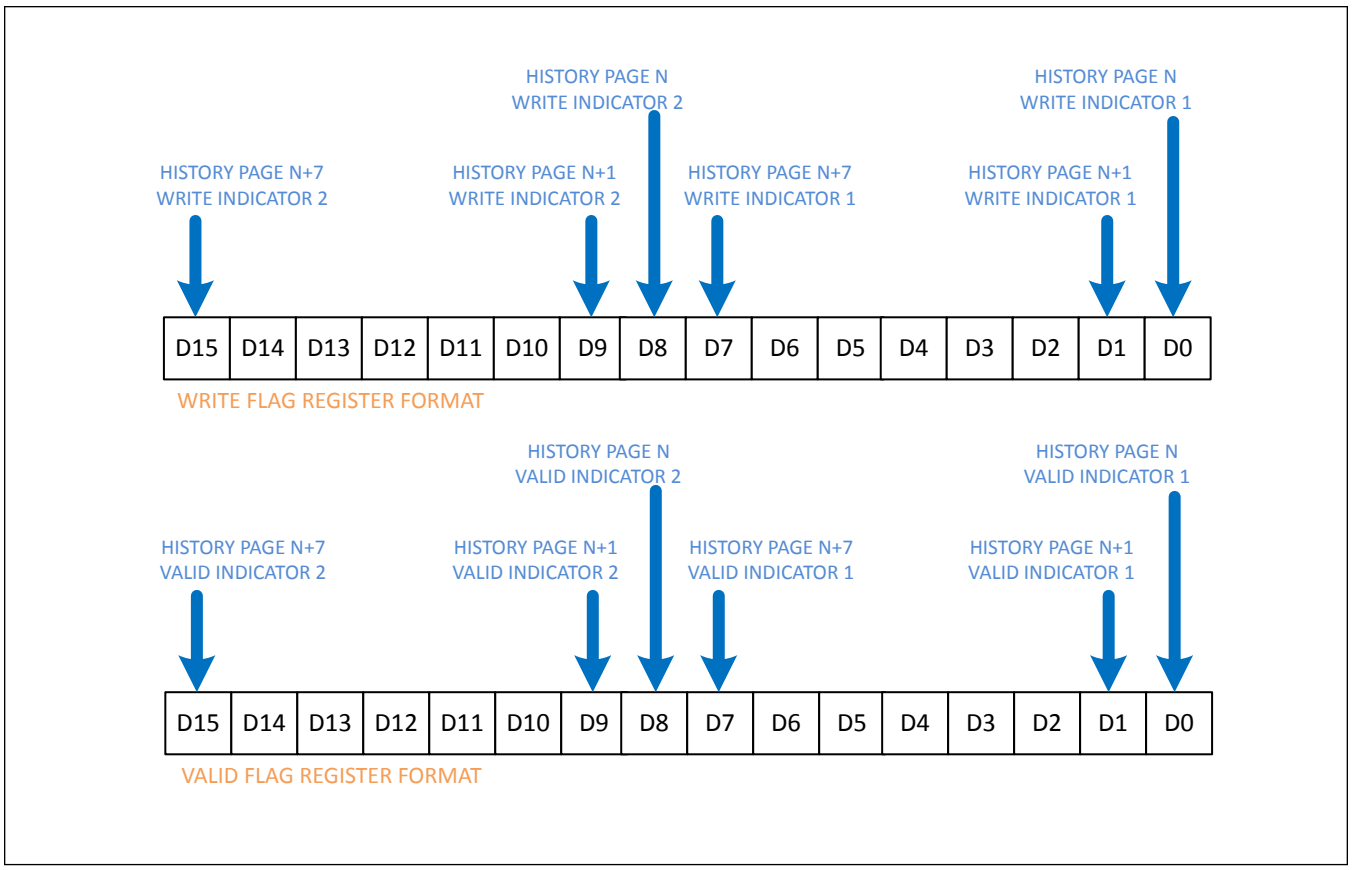


Figure 22. Write Flag Register and Valid Flag Register Formats

Once all four flags for a given history page are known, the host can determine if the history page contains valid data. If either write flag is set then data has been written to that page by the IC. If both write flags are clear, the page has not yet been written. Due to application conditions, the write may not have been successful. Next check the valid flags. If either valid flag is set, the data should be considered good. If both valid flags are clear then the data should be considered bad and the host should ignore it. Table 10 shows how to decode the flags.

Table 10. Decoding History Page Flags

WRITE INDICATOR 1	WRITE INDICATOR 2	VALID INDICATOR 1	VALID INDICATOR 2	PAGE STATUS
0	0	X	X	Page empty.
1	X	0	0	Write failure. Page has invalid data.
		1	X	Write success. Page has valid data.
		X	1	
X	1	0	0	Write failure. Page has invalid data.
		1	X	Write success. Page has valid data.
		X	1	

Reading History Data

Once all pages of valid history data have been identified, they can be read from the IC using the HISTORY RECALL

command. Table 11 shows the command and history page relationship. After sending the command, wait t_{RECALL}, then read the history data from IC page 1Fh. Each page of history data has the same format as page 1Ah. For example, nCycles is found at address 1A4h and nCycles history are at 1F4h, nTimerH is located at address 1AFh and nTimerH history is located at address 1FFh, etc.

Table 11. Reading History Data

COMMAND	HISTORY PAGE RECALLED TO PAGE 1EH
E22Eh	Page 1
E22Fh	Page 2
...	...
E291h	Page 100

History Data Reading Example

The host would like to read the life-logging data from a given IC. The host must first determine how many history pages have been written and if there are any errors. To start checking history page 1, the host sends E29Ch to the command register, wait t_{RECALL}, then read location 1F2h. If either the D0 or the D8 bit in the read data word is a logic 1, the host knows that history page 1 contains history data. The host can then check page 2 (bits D1 and D9) up to page 7 (bits D7 and D15). The host continues on to pages 8 to 16 by reading location 1F3h and then repeating individual bit testing. This process is repeated for each command and address listed in Table 9 until the host finds a history page where both write flags read logic 0. This is the first unwritten page. All previous pages contain data, all following pages are empty.

The host must now determine which, if any, of the history pages have bad data and must be ignored. The above process is repeated for every location looking at the valid flags instead of the write flags. Any history page where both valid flags read logic 0 is considered bad due to a write failure and that page should be ignored. Once the host has a complete list of valid written history pages, commands E22Eh to E291h can be used to read the history information from page 1Fh for processing.

Note that this example was simplified in order to describe the procedure. A more efficient method would be for the host to send a history command once and then read all associated registers. For example, the host could send the E29Ch command once and then read the entire memory space of 1F0h to 1FFh which would contain all write flags for pages 1 to 100 (1F2h to 1FEh) and all valid flags for pages 1 to 8 (1FFh). This applies for all E2XXh history commands.

See *Appendix A: Reading History Data Pseudo-Code Example* section for a psuedo-code example of reading history data.

Analog Measurements

The IC monitors individual cell and pack voltages, current, and temperatures as shown in Table 12. This information is used to protect the battery pack, provided to the fuel gauge algorithm to predict cell capacity and also made available to the user. See the *Analog Measurement Registers* section for more details.

Table 12. Analog Measurement Registers

	REGISTER NAME	ADDRESS	PURPOSE/CONTENTS
Voltage Registers	*VCell*	01Ah	Lowest cell voltage
	Cell1, Cell2, Cell3, Cell4	0D8h,0D7h, 0D6h,0D5h	Direct cell measurements of selected number of cells
	Batt, *PCKP*	0DAh, 0DBh	The Batt registers contains the total pack voltage measured inside the protector and PCKP register contains the voltage between PACK+ and GND
	AvgVCell	019h	Average VCell
	AvgCell1, AvgCell2, AvgCell3, AvgCell4	0D4h, 0D3h, 0D2h, 0D1h	Average of voltages
Temperature Registers	*Temp*	01Bh	The highest thermistor temperature if enabled, and the die-temperature if the thermistors are disabled
	Temp1, Temp2, Temp3, Temp4 *DieTemp*	13Ah, 139h, 138h, 137h 034h	Individual temperature measurements from the enabled thermistors and internal die temperature
	AvgTA, *AvgTemp1, AvgTemp2, AvgTemp3, AvgTemp4* *AvgDieTemp*	016h, 136h, 135h, 134h, 133h 040h	Average of temperatures
Current Registers	*Current*	01Ch	Battery current
	AvgCurrent	01Dh	Average current
Other	Power, AvgPower	0B1h, 0B3h	Power
	TimerH, Timer nTimerH	0BEh, 03Eh 1AFh	32-bit 23.9 year timer 23.9 year nonvolatile timer
	QH, QL	04Dh, 04Eh	32-bit coulomb counter

Cell Balancing

If cells are imbalanced, then one cell might reach full or empty earlier than others, limiting the maximum capacity of the pack. The IC balances the cells using internal MOSFETs. While charging, if the IC detects that the voltage of a cell or cells is higher than the average voltage of the cell pack as determined by nBalTh.BALCFG setting, the IC enables an internal FET to shunt current away from the corresponding cell. The small difference in charging current balances all cells in the pack over time.

Cell Balancing Window of Operation

Cell balancing occurs when cell balancing is enabled and there is a voltage mismatch between the maximum and minimum cell voltages greater than the balancing threshold and if either of the following conditions are met:

- The AvgCurrent register value must be above nProtMiscTh.CurrDet, which indicates the battery is charging.
- The Voltage Fuelgauge State of Charge (VFSOC) register value must be larger than the FullSOCThr register value indicating the pack is nearly full.

Cell balancing continues after the charge has stopped and even into discharge as long as VFSOC remains above FullSOCThr. This can extend the balancing opportunity beyond the typical charging window. Figure 23 shows the opportunity of when cell balancing may occur.

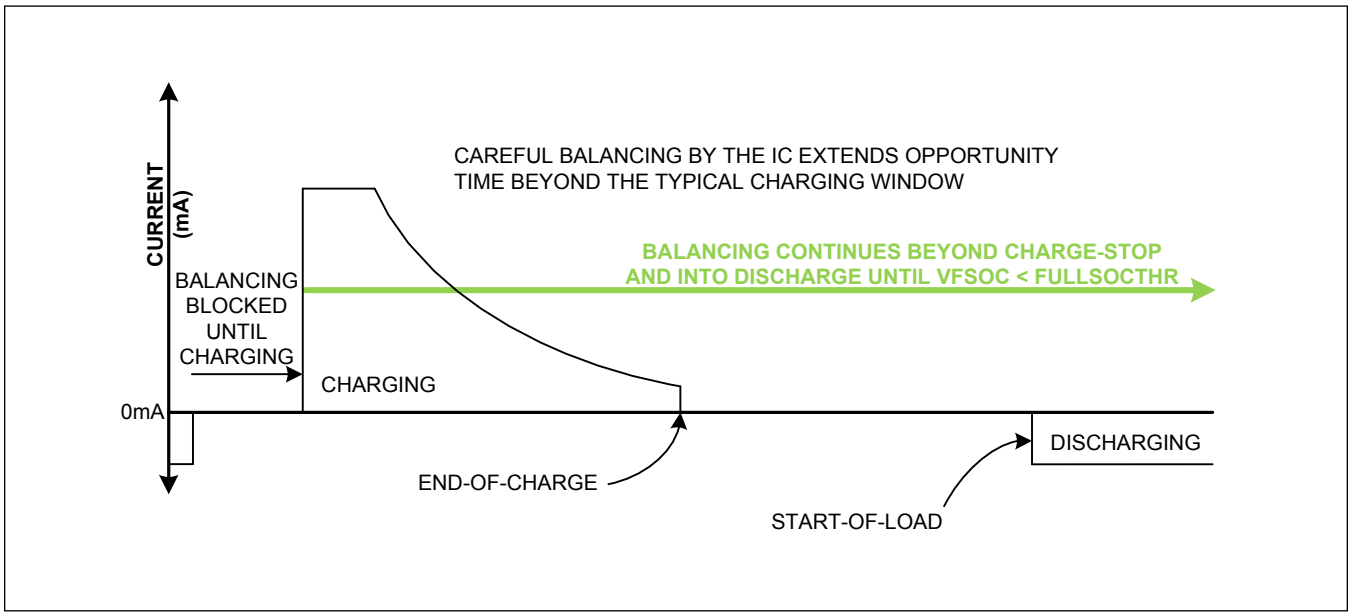


Figure 23. Cell Balancing Window of Operation

Cell Balancing Order and Thresholds

As soon as the cell balancing window is entered the maximum and minimum average cell voltages are calculated. If the difference from max to min is more than the threshold defined by the nBalTh.BALCFG and nBalTh.RMismatch settings, the corresponding internal balancing switch is enabled to reduce charging current flowing through the cell with the highest voltage. Table 13 shows all balancing threshold levels determined by BALCFG. The recommended balancing threshold is 011b or 10.0mV.

Table 13. Cell Balancing Thresholds

BALCFG VALUE	BALANCING THRESHOLD
000b	Balancing Disabled (Factory Default)
001b	2.5mV
010b	5.0mV
011b	10.0mV
100b	20.0mV
101b	40.0mV
110b	80.0mV
111b	160.0mV

RMismatch

The IC determines when there is a voltage mismatch by comparing the maximum and minimum cell voltages.

$$VOLTAGE_{MISMATCH} = MaxCellVoltage - MinCellVoltage$$

In order for balancing to occur, the voltage mismatch must be greater than a configurable threshold.

$$VOLTAGE_{MISMATCH} > 1.25mV \times 2^{nBalTh.BalCfg} + |AverageCurrent| \times Rmismatch$$

Rmismatch is used for balancing to tolerate resistance mismatch between cells, which normally is larger at low states of charge, and exclude balancing during higher current. Rmismatch should be selected in mΩ approximately 20% of nominal battery resistance. Default recommendation is nBalTh.Rmismatch = 3 corresponding with 11.7mΩ.

Cell Balancing Circuits

Figure 24 shows the equivalent balancing circuits for 2S-, 3S-, and 4S-cell packs. Internal cell-balancing FETs allow current to be drawn from an individual cell in the pack during charge. To limit current during cell balancing, an external resistor must be added in series with the CELL1, CELL2, CELL3 and BATTS pins. If these resistors are not installed, power in excess of the IC package maximum rating could be drawn leading to failure.

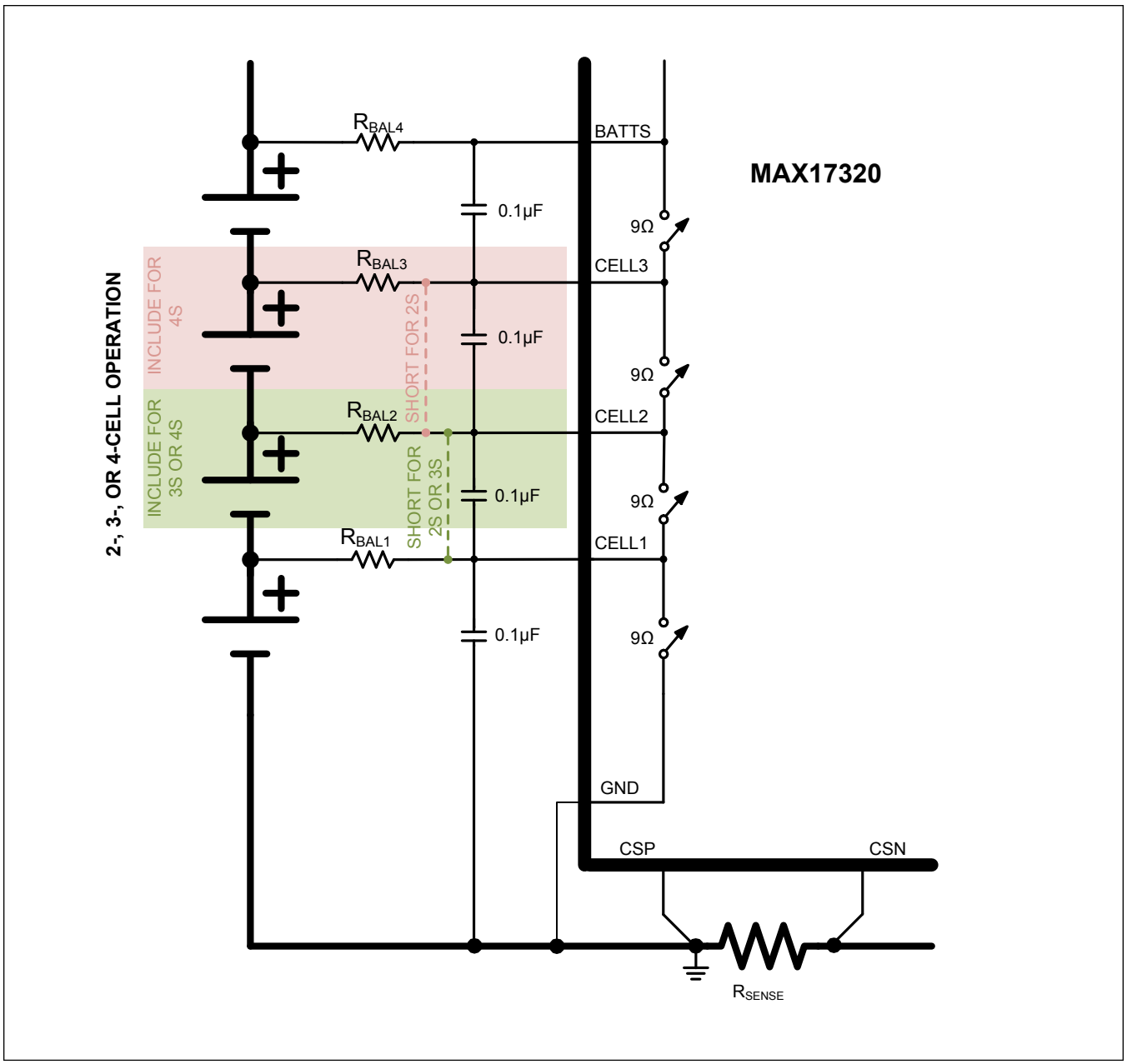


Figure 24. Cell Balancing Configuration

Cell Balancing Current

External series resistors on the CELL1, CELL2, CELL3 and BATTS pins are required to limit the current flow when balancing. The value of these resistors should be selected to prevent exceeding 100mA, the maximum rated current for these pins. The balancing currents can be calculated as follows. Remember to size these resistors to handle the power dissipated by balancing.

CELL1: $IBAL_{MAX} = V_{CELLMAX} / (R_{BAL} + R_{SWITCH})$

CELL2, CELL3, BATTS: $IBAL_{MAX} = V_{CELLMAX} / (2 \times R_{BAL} + R_{SWITCH})$

Where:

R_{SWITCH} is 9Ω typical

$V_{CELLMAX}$ is the maximum cell voltage during charging

R_{BAL} is the external series resistor to limit current

Cell Balancing Duty Cycle

The IC temporarily interrupts cell balancing to prevent interference with voltage and current measurements. Balancing is disabled 45ms minimum prior to making a measurement to allow for settling of the external filter on the pin. This pause occurs once every task period and has minimal impact on the average balancing current as shown in Figure 25.

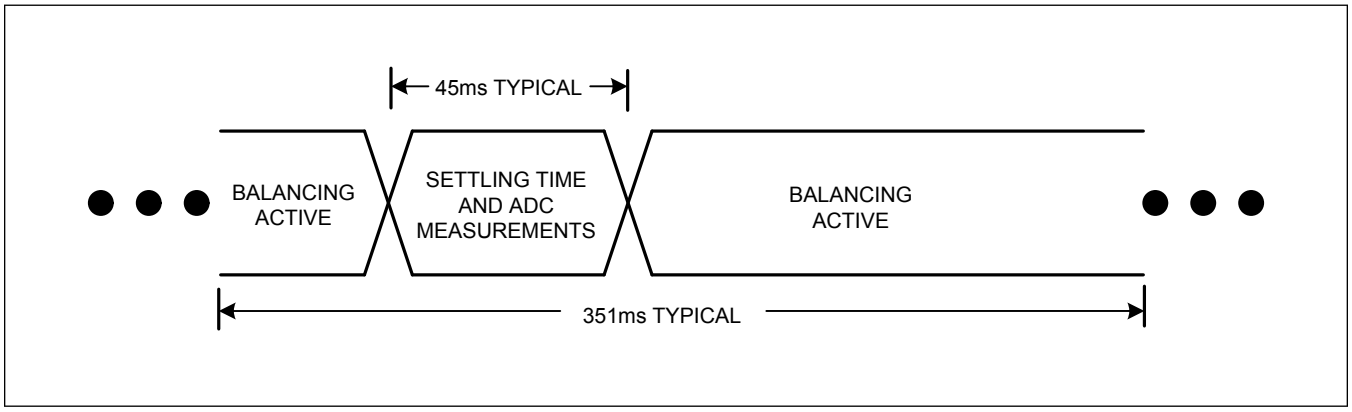


Figure 25. Cell Balancing Duty Cycle

Internal Self-Discharge Detection Interaction with Cell Balancing

Cell balancing is compatible with the IC's internal self-discharge detection function without any special user considerations. The internal self-discharge algorithm uses the coulomb counter, which corresponds to the state of the lowest state cell, so it is immune from the balancing of the cells with higher voltages.

Backup and Always-On LDO

The IC provides a configurable always-on LDO (1.8V or 3.4V) that can power small critical loads (less than 2mA). The always-on LDO remains on during undervoltage protection events and permanent failure events as well as remains on when the IC is in ship mode. To conserve power in deepship mode, the LDO is turned off.

Applications:

- Real-Time Clock
- Replace any coin cell
- Always-on security/tamper detection
- Payment terminals/mobile point-of-sale

The host can turn on/off the LDO as well as change the output voltage between 1.8V and 3.4V by writing the *nPackCfg* register if the memory location is unlocked and the write protection is disabled.

SHA-256 Authentication

The IC supports authentication which is performed using a FIPS 180-4 compliant SHA-256 one-way hash algorithm on a 512-bit message block. The message block consists of a 160-bit secret, a 160-bit challenge, and 192 bits of constant data. Optionally, the 64-bit ROM ID replaces 64 of the 192 bits of constant data used in the hash operation. Contact Maxim for details of the message block organization.

The host and the IC both calculate the result based on the mutually known secret. The result of the hash operation is known as the message authentication code (MAC) or message digest. The MAC is returned by the IC for comparison to the host's MAC. Note that the secret is never transmitted on the bus and thus cannot be captured by observing bus traffic. Each authentication attempt is initiated by the host system by writing a 160-bit random challenge into the SHA memory address space 0C0h to 0C9h. The host then issues the compute MAC or compute MAC with ROM ID command. The MAC is computed per FIPS 180-4 and stored in address space 0C0h to 0CFh overwriting the challenge value.

The IC introduces the new MAC key derivation function (MKDF), a 2-stage authentication scheme that utilizes an intermediate secret for an added layer of security.

See the *SHA-256 Authentication Procedures* section for details of all of the SHA-256 procedures.

Note that the results of the authentication attempt are determined by host verification. The operation of the IC is not affected by authentication success or failure.

Wake-Up/Shutdown

Modes of Operation

The MAX17320 supports five power modes (two active modes and three shutdown modes) as shown in Table 14 with descriptions of the features available, the typical current consumption, and the method to enter and exit each mode.

Table 14. Modes of Operation

MODE	CONSUMPTION (TYPICAL)	DESCRIPTION
Full Active	38µA	Full functionality. The protection FETs, charge pump, and ADC are on. Firmware tasks execute every 351ms.
Protect	16µA	ADC is on. The FETs and charge pump are disabled due to a protection event, disconnecting the battery from the system. RAM is preserved and the gauge continues to monitor the battery until the fault is removed. Firmware remains awake and ready to communicate. Firmware tasks execute every 1.4s.
Ship*	16µA	Similar state as "Protect" except the firmware is responsive to wake-up events such as charger connection, communications wake-up, or pushbutton wake-up (depending on which wake-ups are enabled by configuration). Firmware tasks execute every 1.4s.
DeepShip*	2.2µA	FETs, charge pumps, ADC, and firmware are all placed into a shutdown state. The only activity alive relates to analog circuits that monitor for wake-up conditions (charger detection, communications, or pushbutton, depending on which are enabled).
Undervoltage Shutdown	2.2µA	FETs, charge pumps, ADC, firmware, and most wake-up circuits are powered down. Only the charger-detection wake-up circuit remains powered in this mode to best conserve the small remaining battery capacity and prevent deep discharge.

**On the I^2C shutdown command (setting Config.SHDN = 1) or when the I^2C SCL/SDA lines collapse (and depending on whether COMMSH is enabled), the MAX17320 either enters Ship (if nProtCfg.DeepShpEn = 0) or DeepShip (if nProtCfg.DeepShpEn = 1).*

The MAX17320 can be awoken with a variety of methods depending on the configuration. If pushbutton wake-up is enabled (nConfig.PBen = 1), then consistently pulling the ALRT/PIO pin low, either by pushbutton or system configuration, wakes up the device. A high-to-low transition on any of the communication lines wakes up the device. A consistent connection to a charger wakes up the device.

The MAX17320 prevents accidental wake-up when the system is boxed and shipped. When awoken by any source, it debounces all wake-up sources (button, communications, and charger detection) to ensure that the wake-up is valid. If no valid wake-up is discovered, the device returns to Ship or DeepShip.

Power Mode Transition State Diagram

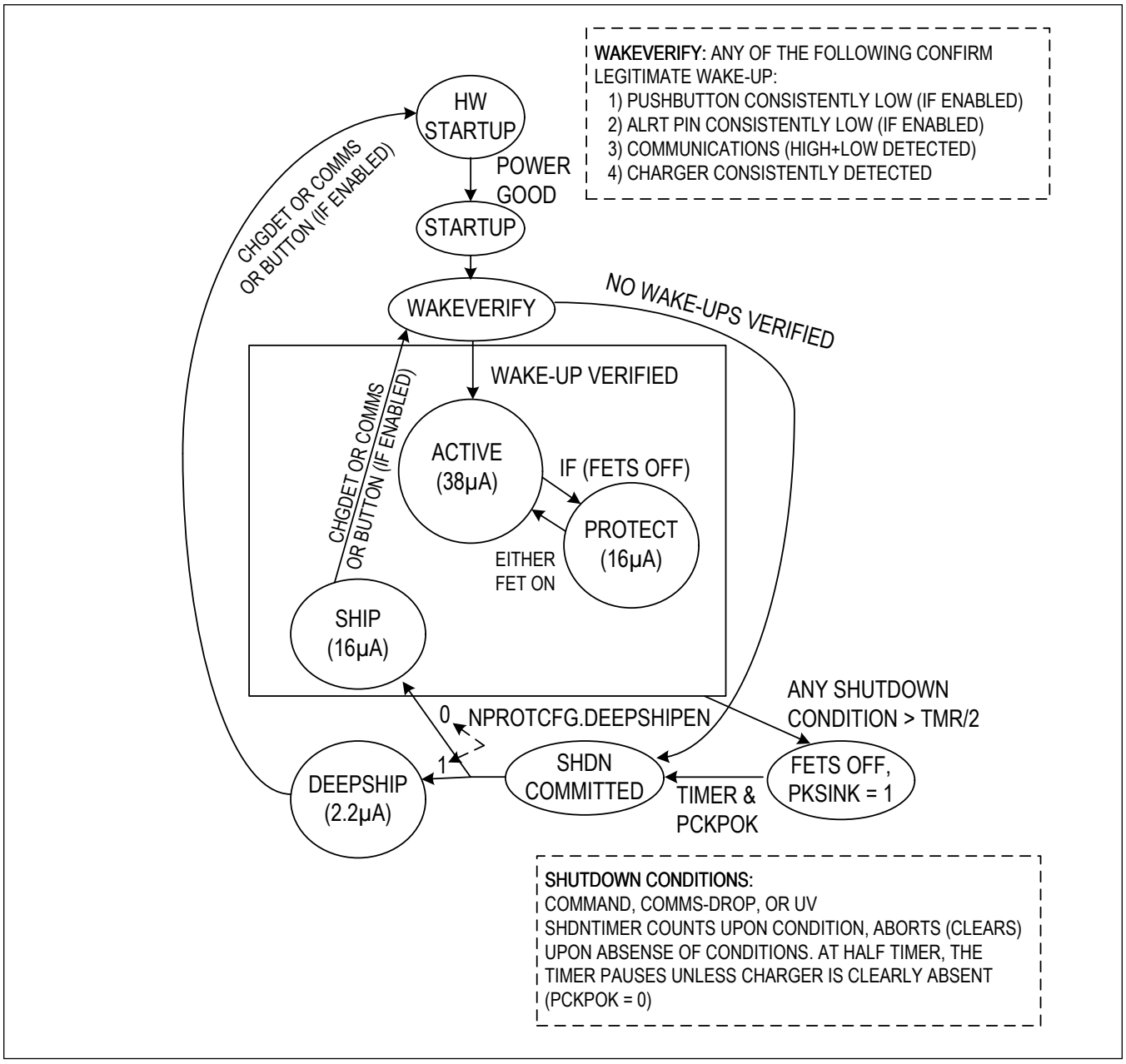


Figure 26. Power Modes Transition State Diagram

Pushbutton Wake-Up

The ALRT/PIO pin can be used to wake up the device by enabling the pushbutton wake-up function by setting the nConfig.PBen. The pushbutton can be implemented in the system to wake up the device and the system as shown in the *Pushbutton Schematic*.

Register Description

Register Description Conventions

The following sections define standard conventions used throughout the data sheet to describe register functions and device behavior. Any register that does not match one of the following data formats is described as a special register.

Standard Register Formats

Unless otherwise stated during a given register's description, all IC registers follow the same format depending on the type of register. Refer to Table 15 for the resolution and range of any register described hereafter. Note that current and capacity values are displayed as a voltage and must be divided by the sense resistor to determine amps or amp-hours. It is strongly recommended to use the nRSense (1CFh) register to store the sense resistor value for use by host software.

Table 15. ModelGauge Register Standard Resolutions

REGISTER TYPE	LSB SIZE	MINIMUM VALUE	MAXIMUM VALUE	NOTES
Capacity	5.0µVh/ R_{SENSE}	0.0µVh	327.675mVh/ R_{SENSE}	Equivalent to 1.0mAh with a 0.005Ω sense resistor.
Percentage	1/256%	0.0%	255.9961%	1% LSb when reading only the upper byte.
Voltage	0.078125mV	0.0V	5.11992V	
Current	1.5625µV/ R_{SENSE}	-51.2mV/ R_{SENSE}	51.1984mV/ R_{SENSE}	Signed 2's complement format. Equivalent to 312.5µA with a 0.005Ω sense resistor.
Temperature	1/256°C	-128.0°C	127.996°C	Signed 2's complement format. 1°C LSb when reading only the upper byte.
Resistance	1/4096Ω	0.0Ω	15.99976Ω	
Time	5.625s	0.0s	102.3984hr	
Special				Format details are included with the register description.

Device Reset

Device reset refers to any condition that would cause the IC to recall nonvolatile memory into RAM locations and restart operation of the fuel gauge. Device reset refers to the initial power-up of the IC, temporary power loss, or reset through the software power-on-reset command.

Nonvolatile Backup and Initial Value

All configuration register locations have nonvolatile memory backup that can be enabled with control bits in the nNVCfg0, nNVCfg1, and nNVCfg2 registers. If enabled, these registers are initialized to their corresponding nonvolatile register value after device reset. If the nonvolatile backup is disabled, the register restores to an alternate initial value instead. See each register description for details.

Register Naming Conventions

Register addresses are described throughout the document as 9-bit internal values from 000h to 1FFh. These addresses must be translated to 16-bit external values for the 1-Wire version or 8-bit values for the I^2C version. See the *Memory* section for details.

Register names that start with a lowercase 'n', such as nPackCfg for example, indicate the register is a nonvolatile memory location. Register names that start with a lowercase 's' indicate the register is part of the SBS compliant register block.

Protection Registers

nPackCfg Register (1B5h)

Configure nPackCfg register according to the application schematic.

Register Type: Special

Factory Default Value: 0004h

The nPackCfg register configures the number of cells and thermistors (and thermistor type) in the battery pack. It also configures the charge pump and backup regulator voltage levels. nPackCfg configuration must match the pack hardware for the proper operation of the IC. See the *Typical Application Circuits* section for recommended nPackCfg settings based on operating circuit configuration. Table 16 shows the register format.

Table 16. nPackCfg (1B5h) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AOCfg		BtPkEn	0	THType	0	CPCfg		0	0	0	NThrms			NCELLS	

0: Always write 0

NCELLS: Number of Cells. This field configures the IC for the number of cells in series in the cell pack. Set NCELLS = cellcount-2.

NThrms: Number of Thermistor Channels. 000b: only die temp, 001b: die temp and TH1 thermistor channel enabled, 010b: die temp and TH1 and TH2 thermistor channels enabled, 011b: die temp and TH1, TH2, and TH3 thermistor channels enabled, 100b: die temp and TH1, TH2, TH3 and TH4 thermistor channels enabled.

THType: If using 10kΩ NTC thermistor, set THType = 0. If using 100kΩ NTC thermistor, set THType = 1.

CPCfg: Charge Pump Voltage Configuration (DevName 420Ah or newer). Set according to the desired gate drive. Note that there is a trade-off in quiescent vs. gate-drive. Set CPCfg = {00b,01b,10b} for {6V, 8V, 10V} settings.

AOCfg: Always-on Regulator Configuration.

AOCfg VALUE	DESCRIPTION
00b	AOLDO is disabled.
01b	AOLDO is enabled. Output is 3.4V.
10b	AOLDO is enabled. Output is 1.8V.
11b	AOLDO is enabled. Output is 3.4V.

BtPkEn: Enable Pckp and Batt Channels update. If set to 0 Pckp/Batt channels updates every 22.4s. If set to 1 Pckp/Batt channels update after all cell measurements are completed.

Voltage Protection Registers

nUVPrtTh Register (1D0h)

Factory Default Value: 508Ch

The nUVPrtTh register shown in Table 17 sets undervoltage protection, deep-discharge-state protection, and undervoltage-shutdown thresholds.

Table 17. nUVPrtTh Register (1D0h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
UVP						0	UOCVP					UVShdn			

UVP: UnderVoltage Protection threshold. The IC opens the discharge FET when VCell < UVP. UVP can be configured from 2.2V to 3.46V in 20mV steps. UVP is unsigned.

UOCVP: Under Open Circuit Voltage Protection Threshold (also refered to as *SmartEmpty*). The IC opens the discharge FET when VFOCV < UOCVP. UOCVP is relative to UVP and can be configured from UVP to UVP + 1.28V in 40mV steps. UOCVP is unsigned.

UVShdn: UnderVoltage Shutdown Threshold. The IC shutdowns when VCell < UVShdn. UVShdn is relative to UVP and can be configured from UVP - 0.32V to UVP + 0.28V in 40mV steps.

nPReserved0 Register (1C0h)

Factory Default Value: 0000h

The nPReserved register shown in Table 18 is reserved for internal operation and also sets undervoltage charge blocking threshold,.

Table 18. nPReserved Register (1C0h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	UV_ChargeBlockThr			X	X	X	X	X	X	X	X	X	X

UV_ChargeBlockThr: UnderVoltage Charge Block threshold. (DevName 420Ah or newer) Enable this function to block charging if any of the cell voltages fall below this threshold. The UV_ChargeBlockThr can be set from 1.25V to 2.75V in steps of 0.25V. Set 000b to disable.

UV_ChargeBlockThr Value(V) = 1V + (UV_ChargeBlockThr x .25V)

nJEITAV Register (1D9h)

Factory Default Value: 0059h

The nJEITAV register, shown in Table 19, sets the JEITA Charge Voltage configuration for the IC. The JEITA charge voltage can be read from a charger to set the appropriate charge voltage based on the temperature. Also, this value is used to determine the overvoltage-protection threshold.

Each charge voltage register is an offset with a 5 or 20mV resolution. The RoomChargeV offset is defined relative to a normal standard charge setting of 4.2V. The additional charge voltages are relative to RoomChargeV based on the temperature. To disable the temperature dependence and create a flat charging voltage across the temperature range, set dWarmChargeV, dColdChargeV, and dHotChargeV to a value of 00b.

Table 19. nJEITAV Register (1D9h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RoomChargeV								dWarmChargeV		dColdChargeV			dHotChargeV		

RoomChargeV: RoomChargeV defines the charge voltage between temperatures T2 "Cold" and T3 "Warm", relative to a standard 4.2V setting, providing a range of 3.56V to 4.835V in 5mV steps. RoomChargeV is a signed configuration. Set to 00h to configure for standard 4.2V.

dColdChargeV: ColdChargeV defines the delta charge voltage (relative to RoomChargeV) between temperatures T1

and T2, relative to the room setting, providing a range of RoomChargeV to (RoomChargeV-140mV) in -20mV steps. dColdChargeV configuration is unsigned.

dWarmChargeV: WarmChargeV defines the delta charge voltage (relative to RoomChargeV) between temperatures TWarm and T3, relative to the room setting, providing a range of RoomChargeV to (RoomChargeV-60mV) in -20mV steps. dWarmChargeV configuration is unsigned.

dHotChargeV: HotChargeV defines the delta charge voltage (relative to WarmChargeV) between temperatures T3 and T4, relative to the room setting, providing a range of WarmChargeV to (WarmChargeV-140mV) in -20mV steps. dHotChargeV configuration is unsigned.

nOVPrtTh Register (1DAh)

Factory Default Value: B754h

The nOVPrtTh register shown in Table 20 sets the permanent overvoltage protection threshold, the charge-detection threshold, the overvoltage-protection threshold, and the overvoltage-protection-release threshold. dOVP and dOVPR are relative to the Charge Voltage that is set in the nJEITAV register and have a 10mV resolution.

Table 20. nOVPrtTh Register (1DAh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OVPPermFail					ChgDetTh			dOVP				dOVPR			

dOVP: Delta from ChargeVoltage to Overvoltage Protection. dOVP sets JEITA overvoltage protection relative to ChargeVoltage (see *nJEITAV*). If nNVCfg1.enJP is disabled, then OVP voltage is calculated from RoomChargeV across all temperature zones. This is a positive number with 10mV resolution and 150mV range. Overvoltage protection is calculated as:

$$OVP = ChargeVoltage + dOVP \times 10mV$$

dOVPR: Delta from Overvoltage Protection to the Overvoltage-Release Threshold. dOVPR sets overvoltage-protection release relative to the overvoltage-protection setting. This is a positive number with 10mV resolution and is translated to a negative offset relative to OVP. Overvoltage-protection release is calculated as:

$$OVPR = OVP - dOVPR \times 10mV$$

OVPPermFail: Permanent Failure OVP (permanent overvoltage protection) Threshold. Permanent failure overvoltage protection occurs when any cell voltage register reading exceeds this value. The OVPPermFail range is $OVP\_threshold_{Room}$ + 40mV to $OVP\_threshold_{Room}$ + 340mV with a 20 mV lsb.

$$OVP\_PermFail\_Threshold = OVP_{Room} + 40mV + (OVPPermFail \times 20mV)$$

ChgDetTh: Charger Detection Threshold. The IC determines that a charger is connected when PCKP > (BATT + ChgDetTh). ChgDetTh has a range of 10mV to 80mV with a 10mV lsb.

nBalTh Register (1D4h)

Factory Default Value: 0000h

The nBalCfg register shown in Table 21 sets the balancing and imbalance settings and thresholds.

Table 21. nBalTh Register (1D4h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	Zener	BALCFG			Rmismatch					Imbalance				

0: Set 0, do not set 1.

Zener: Zener Balancing Enable. Set to 1 to enable the Zener Balancing functionality. Set to 0 to disable the Zener Balancing. When Zener Balancing is enabled, the IC acts as if a Zener diode is placed in parallel with each cell. The reverse breakdown voltage of the virtual Zener diode is the ChargingVoltage register. Whenever nBalTh.Zener = 1, the IC enables an internal FET to shunt current away from the highest voltage cell with a voltage higher than the ChargingVoltage register.

BALCFG: Balancing Configuration. This field sets the cell balancing voltage threshold. When set to 0, cell balancing is disabled. When BALCFG bits are set to any nonzero value, cell balancing begins when inside the cell balancing window

as shown in Figure 23. See *RMismatch* section for details.

Rmismatch: Rmismatch is set according to the following equation:

nBalTh.Rmismatch = 32 x Rmismatch(mΩ)/125mΩ (maximum settable Rmismatch is 121mΩ)

Choose Rmismatch in mΩ approximately 20% of nominal battery resistance. The default recommendation is nBalTh.Rmismatch = 3 corresponding with 11.7mΩ. See the *RMismatch* section for details.

Imbalance: Cell Imbalance Protection Threshold. Set the amount of cell imbalance that creates a charge protection fault. Set Imbalance to 0 to disable cell imbalance protection. The LSB size is 10mV.

Current Protection Registers

nODSCTh Register (1DDh)

Factory Default Value: 0EAFh

The nODSCTh register sets the current thresholds for each overcurrent alert. The format of the registers is shown in Table 22.

Table 22. nODSCTh Register (1DDh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	OCTH					SCTH					ODTH				

X: Don't Care.

SCTH: Short-Circuit Threshold Setting. Sets the short-circuit threshold to a value between 0mV and -155mV with a step size of -5mV. The SCTH bits are stored such that 1Fh = 0mV and 00h = -155mV. Short-circuit threshold is calculated as -155mV + (SCTH x 5mV)).

ODTH: Overdischarge Threshold Setting. Sets the overdischarge threshold to a value between 0mV and -77.5mV with a step size of -2.5mV. The ODTH bits are stored such that 1Fh = 0mV and 00h = -77.5mV. Overdischarge threshold is calculated as -77.5mV + (ODTH x 2.5mV)).

OCTH: Overcharge Threshold Setting. Sets the overcharge threshold to a value between 0mV and 38.75mV with a step size of 1.25mV. The OCTH bits are stored such that 1Fh = 0mV and 00h = 38.75mV. Overcharge threshold is calculated as 38.75mV - (OCTH x 1.25mV)).

Table 23 shows sample values of calculated mV thresholds for OCTH, SCTh, and ODTH. Equivalent current thresholds are shown assuming a 5mΩ sense resistor.

Table 23. OCTH, SCTh, and ODTH Sample Values

	OCTH		SCTH		ODTH	
00h	38.75mV	7.75A	-155mV	-31.00A	-77.5mV	-15.50A
01h	37.50mV	7.50A	-150mV	-30.00A	-75.0mV	-15.00A
02h	36.25mV	7.25A	-145mV	-29.00A	-72.5mV	-14.50A
04h	33.75mV	6.75A	-135mV	-27.00A	-67.5mV	-13.50A
08h	28.75mV	5.75A	-115mV	-23.00A	-57.5mV	-11.50A
10h	18.75mV	3.75A	-75mV	-15.00A	-37.5mV	-7.50A
14h	13.75mV	2.75A	-55mV	-11.00A	-27.5mV	-5.50A
18h	8.75mV	1.75A	-35mV	-7.00A	-17.5mV	-3.50A
1Eh	1.25mV	0.25A	-5mV	-1.00A	-2.5mV	-0.50A
1Fh	0.00mV	0.000A	0mV	0.00A	0.0mV	0.00A

nODSCCfg Register (1DEh)

Factory Default Value: 4355h

The nODSCCfg register configures the delay behavior for the short-circuit, overdischarge-current, and overcharge-current comparators. The format of the register is shown in Table 24.

Table 24. nODSCCfg Register (1DEh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	1	X	X	SCDLY				X	1	X	1	OCDLY			

X: Don't Care.

SCDLY: Short-Circuit Delay. Configure from 0h to Fh to set short circuit detection debouncing delay between 70µs and 985µs (70µs + 61µs x SCDLY). There may be up to 31µs of additional delay before the short-circuit's alert affects the discharge FET.

OCDLY: Overdischarge and Overcharge Current Delay. Configure from 1h to Fh to set overdischarge/overcharge detection debouncing delay between 70µs and 14.66ms (70µs + 977µs x OCDLY).

nIPrtTh1 Register (1D3h)

Factory Default Value: 4BB5h

The nIPrtTh1 register shown in Table 25 sets upper and lower limits for overcurrent protection when current exceeds the configuration threshold. The upper 8-bits set the overcharge current-protection threshold and the lower 8-bits set the overdischarge current-protection threshold. Protection threshold limits are configurable with 400µV resolution over the full operating range of the current register.

Table 25. nIPrtTh1 Register (1D3h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OCCP								ODCP							

OCCP: Overcharge Current-Protection Threshold at Room Temperature. Overcharge current-protection occurs when the current register reading exceeds this value. This field is signed 2's complement with 400µV LSb resolution to match the upper byte of the current register. HotCOEF, WarmCOEF, and ColdCOEF re-scales nIPrtTh1.OCCP in hot, warm, and cold zone.

For example, in warm zone, overcharge current-protection threshold updates to OCCP x WarmCOEF.

See the *nJEITAC* register for HotCOEF, WarmCOEF, and ColdCOEF definitions and the *nTPrtTh2* and *nTPrtTh3* registers for temperature zone definitions.

ODCP: Overdischarge Current-Protection Threshold. Overdischarge current-protection occurs when current register reading exceeds this value. This field is signed 2's complement with 400µV LSb resolution to match the upper byte of the current register.

The fault delay for OCCP and ODCP is configured in nDelayCfg.OverCurrTimer.

nJEITAC Register (1D8h)

Factory Default Value: 644Bh

The nJEITAC register shown in Table 26 sets the nominal room temperature charging current and the coefficients to scale the charging current across the temperature zones shown in Figure 3. The WarmCOEF, ColdCOEF, and HotCOEF coefficients impact the charging current as well as OCCP and ODCP (See *nIPrtTh1*).

To disable the temperature dependence and create a flat charging current across the temperature range, set the lower byte of nJEITAC to a value of FFh.

Table 26. nJEITAC Register (1D8h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RoomChargingCurrent								WarmCOEF		ColdCOEF			HotCOEF		

RoomChargingCurrent: Sets the nominal room-temperature charging current. The LSB is 200µV. This value is unsigned with a range of 00h (0mV) to FFh (51.2mV).

HotCOEF: Coefficient 12.5% to 100% relative to ChargingCurrent for controlling the charge current at hot. HotCOEF has a 12.5% LSB resolution. The resulting HotChargingCurrent is controlled by the following equation:

$$HotChargingCurrent = RoomChargingCurrent \times (HotCOEF+1)/8$$

WarmCOEF: Coefficient 62.5% to 100% relative to ChargingCurrent for controlling the charge current at warm. WarmCOEF has a 12.5% LSB resolution. The resulting WarmChargingCurrent is controlled by the following equation:

$$WarmChargingCurrent = RoomChargingCurrent \times (WarmCOEF+5)/8$$

ColdCOEF: Coefficient 12.5% to 100% relative to ChargingCurrent for controlling the charge current at cold. ColdCOEF has a 12.5% LSB resolution. The resulting ColdChargingCurrent is controlled by the following equation:

$$ColdChargingCurrent = RoomChargingCurrent \times (ColdCOEF+1)/8$$

HotCOEF, WarmCOEF, and ColdCOEF also rescale nIPrtTh1.OCCP.

Temperature Protection Registers

The IC has five thresholds for charging protection as well as overdischarge temperature protection and overtemperature permanent failure protection. The standard register format for each of these thresholds is a signed 2's compliment number with 1°C resolution. The IC has 2°C of hysterisis for releasing temperature faults.

nTPrtTh1 Register (1D1h)

Factory Default Value: 3700h

The nTPrtTh1 register shown in Table 27 sets T1 "Too-Cold" and T4 "Too-Hot" thresholds which control JEITA and provide charging (Too-Hot or Too-Cold) protection. nProtMiscTh.TooHotDischarge provides discharging (Too-Hot only) protection.

Table 27. nTPrtTh1 Register (1D1h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T4 ("Too-Hot")								T1 ("Too-Cold")							

T1-T4 follow JEITA's naming convention for temperature ranges.

T1: JEITA "Too-Cold" temperature threshold. When Temp < T1, charging is considered unsafe and unhealthy, and the IC blocks charging.

T4: JEITA "Too-Hot" temperature threshold. When Temp > T4, charging is blocked by the IC.

nTPrtTh2 Register (1D5h)

Factory Default Value: 2D0Ah

The nTPrtTh2 register shown in Table 28 sets T2 "Cold" and T3 "Hot" thresholds which control JEITA and modulate charging (Hot or Cold) guidance and protection.

Table 28. nTPrtTh2 (1D5h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T3 ("Hot")								T2 ("Cold")							

T1-T4 follow JEITA's naming convention for temperature ranges.

T2: JEITA "Cold" temperature threshold. When Temp < T2, charging current/voltage should be reduced, and the charge-protection thresholds are adjusted accordingly.

T3: JEITA "Hot" temperature threshold. When Temp > T3, charging current/voltage should be reduced and the charge-protection thresholds are adjusted accordingly.

nTPrtTh3 Register (1D2h) (beyond JEITA)

Factory Default Value: 5528h

The nTPrtTh3 register shown in Table 29 sets Twarm and TpermFailHot thresholds which control JEITA and modulate charging (Warm) guidance and protection.

Table 29. nTPrtTh3 Register (1D2h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TpermFailHot								Twarm							

nTPrtTh3 defines protection thresholds beyond standard JEITA definition.

Twarm: Warm temperature threshold (between 'normal' and THot), giving an extra temperature region for changing charging current and charging voltage control.

TpermFailHot: If enabled, the IC goes into permanent failure mode, and permanently disables the charge FET as well as trips the secondary protector (if installed) or blows the fuse (if installed).

nProtMiscTh Register (1D6h)

Factory Default Value: 7A28h

The nProtMiscTh register is shown in Table 30 and sets a few miscellaneous protection thresholds.

Table 30. nProtMiscTh Register (1D6h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
QovflwTh				TooHotDischarge				CurrDet				DieTempTh			

DieTempTh: Sets the Dietemp Overtemperature-Protection Threshold. DieTempTh is used as a proxy for FET temperature and controls the FET overtemperature fault. The range is 50°C and 125°C with a 5°C LSB.

CurrDet: CurrDet is configurable from 25µV/R_{SENSE} to 400µV/R_{SENSE} in 25µV/R_{SENSE} steps (equivalent to 5mA to 80mA in 5mA steps with a 5mΩ sense resistor). It is a threshold to detect discharging and charging events. If current > CurrDet then charging; if current < -CurrDet then discharging.

CurrDet Threshold = (CurrDet + 1) x 5mA (i.e., 0 = 5mA for 5mΩ R_{SENSE})

TooHotDischarge: Sets the Overtemperature-Protection Threshold Associated with Discharge. TooHotDischarge has 2°C LSB's and defines the delta between Over-Temp-Charge (nTPrtTh1.T4) and Over-Temp-Discharge. The range is nTPrtTh1.T4(TooHot) to nTPrtTh1.T4(TooHot) + 30°C.

QovflwTh: Capacity Overflow Threshold. QovflwTh sets the coefficient for the capacity overflow-protection threshold. Capacity overflow protection threshold = designCap x coefficient. The IC monitors the delta coulomb count (deltaQ) between the coulomb count at the start-of-charge and the present coulomb count. If the delta Q exceeds the capacity overflow-protection threshold, indicating that the charger has charged more than the expected capacity of the battery, then a ProtStatus.Qovrflw fault is generated. The coefficient is calculated as: coefficient = 1.0625 + (QovflwTh x 0.0625).

nProtMiscTh2 Register (1CBh)

Factory Default Value: 0000h

The nProtMiscTh2 register is shown in [[nProtMiscTh2 Register (1D6h) Format]] and sets a few miscellaneous protection thresholds.

Table 31. nProtMiscTh2 Register (1CBh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved							UVPFEn	UVPFTh				TooColdDischarge			

TooColdDischarge: Sets the Undertemperature-Protection Threshold Associated with Discharge and is enabled by setting nProtCfg.BlockCDisEn. TooColdDischarge has 2°C LSB's and defines the delta between Under-Temp-Charge (nTPrtTh1.T1 'Too-Cold') and Under-Temp-Discharge. The range is nTPrtTh1.T1(TooCold) to nTPrtTh1.T1(TooCold) - 30°C. There is a 2.5°C hysteresis to release this fault. (DevName 420Bh or newer)

TooColdDischarge Threshold = nTPrtTh1.T1(TooCold) - (nProtMiscTh2.TooColdDischarge x 2)

UVPFen: Enables the Under Voltage Permanent Failure Function. Set to 1 to enabled the Under Voltage Permanent Failure Function. Set to 0 to disable the function. (DevName 420Bh or newer)

UVPFTh: Sets the Under Voltage Permanent Failure Threshold. (DevName 420Bh or newer). The threshold is relative to the UVP threshold with an LSB of 135mV.

UVPFTh = UVP - UVPFTh = (2.2V + nUVPrtTh.UVP x 20mV) - nProtMiscTH2.UVPFTh x 135mV.

Fault Timer Registers

nDelayCfg Register (1DCh)

Factory Default Value: AB3Dh

Set nDelayCfg to configure debounce timers for various protection faults. A fault state is concluded only if the condition persists throughout the duration of the timer. All delay times start when the ADC first measures the value to exceed the protection threshold which could be up to an additional 351ms of delay between the time the fault is observed externally and the time the ADC first measures the fault

Table 32. nDelayCfg (1DCh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHGWDT		FullTimer			OVPTimer		OverCurrTimer			PermFailTimer		TempTimer		UVPTimer	

UVPTimer: Set UVPTimer to configure the Undervoltage-Protection timer.

Shutdown Timer: Set UVPTimer to configure the Shutdown timer.

Table 33. UVPTimer Settings

UVPTIMER SETTING	0	1	2	3
UVPTimer Configuration	0 to 351ms	2.8s to 5.625s	5.625s to 11.25s	11.25s to 22.5s
Shutdown Timer Configuration	22.5s to 45s	45s to 90s	90s to 180s	3min to 6min

TempTimer: Set TempTimer to configure the fault-timing for the following faults: Too-Cold-Charging (TooColdC), Too-Hot-Charging (TooHotC), Die-Hot (DieHot), and Too-Hot-Discharging (TooHotD).

The TempTimer setting also controls the temperature transition delay. If the IC detects a change in temperature zone that results in the OVP level being reduced to a lower level due to the JEITA configuration. There is a delay equal to the TempTrans Configuration before the new lower OVP threshold goes into effect.

Table 34. TempTimer/TempTrans Setting

TEMPTIMER SETTING	0	1	2	3
Application	No debouncing	Debounce 1 thermistor	Debounce up to 2 thermistors	Debounce up to 4 thermistors
TempTimer Configuration	0 to 351ms	1.4s to 2.8s	2.8s to 5.625s	5.625s to 11.25s
TempTrans Configuration	3.151s to 4.55s	5.951s to 8.75s	11.55s to 17.15s	23.351s to 34.851s

PermFailTimer: Set PermFailTimer to configure the fault-timing for permanent failure detection. PermFailTimer must be set to 3 for permanent failure detection to function properly.

Table 35. PermFailTimer Settings

PERMFAILTIMER SETTING	0 (NOT RECOMMENDED)	1	2	3
Configuration	0 to 351ms	351ms to 0.7s	0.7s to 1.4s	1.4s to 2.8s

OverCurrTimer: OverCurrTimer configures the fault timing for the slow overcharge-current detection (OCCP) as well as overdischarge-current detection (ODCP). The additional fast hardware protection thresholds are described in nODSCCfg and nODSCTh.

Table 36. OverCurrTimer Settings

OVERCURRTIMER SETTING	0	1	2	3	4	5	6	7
Configuration	0-351ms	0.351s to 0.7s	0.7s to 1.4s	1.4s to 2.8s	2.8s to 5.6s	5.6s to 11.25s	11.25s to 22.5s	22.5s to 45s

OVPTimer: Set OVPTimer to configure the fault timing for Overvoltage-Protection.

Imbalance Timer: Set OVPTimer to configure the Imbalance fault timer.

Table 37. OVPTimer Settings

OVPTIMER/IMBALANCE SETTING	0	1	2	3
OVPTimer Configuration	0 to 351ms	2.8s to 5.625s	5.625s to 11.25s	11.25s to 22.5s
Imbalance Timer Configuration	0 to 351ms	2.8s to 5.625s	5.625s to 11.25s	11.25s to 22.5s

FullTimer: Set FullTimer to configure the timing for full-detection. When charge-termination conditions are detected and after the timeout, the CHG FET turns off (if feature is enabled).

Prequal Timer: Set FullTimer to configure the timing for prequal charging. Prequal Timer and FullTimer share the same bits in the nDelayCfg register.

Table 38. FullTimer/Prequal Settings

FULLTIMER SETTING	0	1	2	3	4	5	6	7
FullTimer Configuration	33s to 44s	67s to 90s	2.25min to 3min	4.5min to 6min	9min to 12min	18min to 24min	36min to 48min	72min to 96min
Prequal Timer Configuration	16.875s to 22.5s	33s to 44s	67s to 90s	2.25min to 3min	4.5min to 6min	9min to 12min	18min to 24min	36min to 48min

CHGWDT: Set CHGWDT to configure the charger communication watchdog timer. If enabled, the IC charge-protects whenever the host has stopped communicating longer than this timeout.

Table 39. ChgWDT Settings

CHGWDT SETTING	0	1	2	3
Configuration	11.2s to 22.5s	22.5s to 45s	45s to 90s	90s to 3min

Battery Internal Self-Discharge Detection Registers

Factory Default nProtCfg2 Value: A065h

Factory Default nTCurve Value: 0000h

To enable the ISD feature using the coulombic-efficiency (CE) method, configure LeakFaultCfg, LeakCurrTh, and CEEn as shown in Table 40 and Table 41. Choose the alert and fault mode with LeakFaultCfg and configure the thresholds with LeakCurrTh, as shown in Table 42. When the ISD alerts are enabled, any leakage current detected beyond the threshold is indicated by the *ProtAlrt*.LDET bit and Status.PA bit (if *nConfig*.ProtAlrtEn = 1). If the ALRT pin is enabled for alerts (*nConfig*.Aen = 1 and *nConfig*.ProtAlrtEn = 1), then the pin indicates the ISD alert. To service the alert, first clear the *ProtAlrt* register and then clear Status.PA. The event is also indicated in *nBattStatus*.LDET, which is recorded in the permanent lifelog.

The reported leakage-current measurement can be read from two different different registers:

- LeakCurrRep = 15-bit unsigned left-justified value with an LSB of 1.5625µV/16 (or 0.3125mA/16 with 5mΩ sense resistor)
- *nBattStatus*.LeakCurr = 8-bit unsigned value with an LSB of 3.125µV (or 0.625mA with 5mΩ sense resistor)

Contact Analog Devices for configuring the ISD feature.

Table 40. nProtCfg2 Register (1DFh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	CEEn	0	LeakCurrTh				CheckSum							

Table 41. nTCurve Register (0x1C9) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	LeakFaultCfg		

Table 42. Alert and Fault Mode Settings

LEAKFAULTCFG SETTING	DESCRIPTION	LEAKCURRTH RESOLUTION	ALERT RANGE	FAULT RANGE
		Note: Leakage current above LeakCurrTh triggers an alert/fault. Currents refer to the 5mΩ R_{SENSE}		
000	Disabled			
001	Alert only	0.625mA	0.625mA to 10mA	
010	Fault = Alert + 5mA			5.625mA to 15mA
011	Fault = Alert + 10mA			10.625mA to 20mA
100	Fault Only (+5mA offset)	1.25mA		6.25mA to 25mA
101	Alert Only		1.25mA to 20mA	
110	Fault = Alert + 5mA			6.25mA to 25mA
111	Fault = Alert + 20mA			21.25mA to 40mA

X: Don't Care

CEEn: Coulombic-efficiency (CE) method enable. Set to 1 to enable self-discharge detection

LeakFaultCfg: Leakage Fault Configuration. Set LeakFaultCfg to configure the alert and fault behavior as shown in Table 42.

LeakCurrTh: Leakage Current Threshold is an unsigned 4-bit threshold for leakage current alert and fault generation. The LSB resolution is either 0.625mA or 1.25mA based on the LeakCurrCfg setting as shown in Table 42. When alerts and faults are both enabled, the fault threshold is either 5mA, 10mA or 20mA above the alert threshold as shown in the Description column of Table 42.

CheckSum: Protector NVM CheckSum. CheckSum is the checksum value of the protection registers for validating NVM at startup when *nNVCfg1*.enProtChksm = 1.

LeakCurrRep Register (0x16F)

The LeakCurrRep register contains the reported leak current when it is enabled with nProtCfg2.F2FEn as shown in Table 43.

Table 43. LeakCurrRep Register (0x16F) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Reported LeakCurrent														

Reported LeakCurrent: Reported Leak Current is an unsigned 15-bit leakage current. This register stores the reported leakage current with an LSB of 1.5625µV/16 (or 0.3125mA/16 with a 5mΩ sense resistor). The range is 0mA to 639.98mA.

Status/Configuration Protection Registers

The following registers configure and report various protection and alert statuses as measured by the IC.

nProtCfg Register (1D7h)

Factory Default Value: 0900h

The Protection Configuration register contains enable bits for various protection functions.

Table 44. nProtCfg Register (1D7h) Format

D15	D14	D13	D12	D11	D10	D9	D8
ChgWDTEn	0	0	SCTest		CmOvrdEn	0	PreqEn
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved	PFEn	DeepShpEn	OvrdEn	$\overline{\text{UVRdy}}$	FetPFEn	BlockDisCEn	Reserved

PFEn: PermFail Enable. Set PFEn = 1 to enable the detection of a Permanent Failure to permanently turn the FETs off. All types of permanent failures operate only if PFEn = 1 and are all disabled if PFEn = 0. PFEn must be enabled for the PFAIL pin to be operational. See the *Permanent Fail* section for more details.

FetPFEn: FET PermFail Enable. Set to 1 to enable Charge FET and Discharge FET open or short failure detection, which registers a permanent failure and permanently turn the FETs off and drive the PFAIL pin high. PFEn must also be set for the FET PermFail Enable to operate.

$\overline{\text{UVRdy}}$: Undervoltage-Ready. In the undervoltage-protected state (but higher than undervoltage shutdown), this bit chooses whether or not the CHG FET remains enabled. Configure $\overline{\text{UVRdy}}$ = 0 to keep the CHG FET and corresponding pumps powered during undervoltage protection. In this state, the pack is quickly responsive to charger connection, but the quiescent consumption remains 38µA. Configure $\overline{\text{UVRdy}}$ = 1 to disable the CHG FET and corresponding charge pumps during undervoltage protection. In this state, the consumption drops to 16µA, but there may be hibernate latency between when the charger is applied and the battery begins charging.

OvrdEn: Override Enable. Set OvrdEn = 1 to enable the Alert pin to be an input to turn disable the protection FETs. See the *Disabling FETs by Pin-Control or I²C Command* for more details.

CmOvrdEn: Comm Override Enable. This bit when set to 1, allows the ChgOff and DisOff bits in CommStat to be set by I²C/1Wire communication to turn off the protection FETs. See the *Disabling FETs by Pin-Control or I²C Command* for more details.

DeepShpEn: Deepship Enable. Set DeepShpEn = 1 to associate shutdown actions (I²C shutdown command or communication removal) with 2.2µA shutdown. All registers power down in this mode. Set DeepShpEn = 0 to continue full calculations but with protector disabled (CHGEn = 0, DISEn = 0, pump off), operating at 6µA consumption.

PreqEn: PreQual Enable. Set PreqEn = 1 to enable the Pre-Qual enable functionality.

SCTest: Set SCTest = 01b to source 30µA from BATT to PCKP for testing the presence/removal of any overload/short-circuit at PCKP. SCTest is only used during special circumstances when DIS = off. Particularly if an overdischarge current fault has been tripped. The IC sets SCTest to push 30µA into PCKP. If PCKP rises above the 1.5V SCDet threshold, then the overload is considered "removed" and safe to reconnect the DIS FET. Because of this, the PCKP resistor must be 10kΩ or less for proper short-circuit removal detection. Set SCTest = 00b to disable.

ChgWDEn: Charger WatchDog Enable. If the charger watchdog feature is enabled, the protector disallows charging unless communication has not been detected for more than the Charger WatchDog delay that is configured in nDelayCfg.ChgWdg.

BlockDisCEn: Block Discharge at TooCold Enable. If the block discharge at cold is enabled, the protector also disallows discharging when the temperature is below the TooCold Threshold (nTPrtTh1). (DevName 420Ah only)

Status Register (000h)

Register Type: Special

Nonvolatile Backup: None

Initial Value: 0x0002

The Status register maintains all flags related to alert thresholds and battery insertion or removal. Table 45 shows the Status register format.

Table 45. Status Register (000h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PA	Smx	Tmx	Vmx	X	Smn	Tmn	Vmn	dSOCi	Imx	X	X	X	Imn	POR	X

POR: Power-On Reset. This bit is set to a 1 when the device detects that a software or hardware POR event has occurred. This bit must be cleared by system software to detect the next POR event. POR is set to 1 at power-up.

Imn: Minimum Current Alert Threshold Exceeded. This bit is set to a 1 whenever a Current register reading is below the minimum *IAlrtTh* value. This bit is cleared automatically when Current rises above minimum *IAlrtTh* value. Imn is set to 0 at power-up.

Imx: Maximum Current Alert Threshold Exceeded. This bit is set to a 1 whenever a Current register reading is above the maximum *IAlrtTh* value. This bit is cleared automatically when Current falls below maximum *IAlrtTh* value. Imx is set to 0 at power-up.

dSOCi: State-of-Charge 1% Change Alert. This is set to 1 whenever the *RepSOC* register crosses an integer percentage boundary such as 50.0%, 51.0%, etc. Must be cleared by host software. dSOCi is set to 0 at power-up.

Vmn: Minimum Voltage Alert Threshold Exceeded. This bit is set to a 1 whenever a VCell register reading is below the minimum *VAlrtTh* value. This bit may or may not need to be cleared by system software to detect the next event. See *Config.VS* bit description. Vmn is set to 0 at power-up.

Tmn: Minimum Temperature Alert Threshold Exceeded. This bit is set to a 1 whenever a Temperature register reading is below the minimum *TAlrtTh* value. This bit may or may not need to be cleared by system software to detect the next event. See *Config.TS* bit description. Tmn is set to 0 at power-up.

Smn: Minimum SOC Alert Threshold Exceeded. This bit is set to a 1 whenever SOC falls below the minimum *SAlrtTh* value. This bit may or may not need to be cleared by system software to detect the next event. See *Config.SS* and *MiscCFG.SACFG* bit descriptions. Smn is set to 0 at power-up.

Vmx: Maximum Voltage Alert Threshold Exceeded. This bit is set to a 1 whenever a VCell register reading is above the maximum *VAlrtTh* value. This bit may or may not need to be cleared by system software to detect the next event. See *Config.VS* bit description. Vmx is set to 0 at power-up.

Tmx: Maximum Temperature Alert Threshold Exceeded. This bit is set to a 1 whenever a Temperature register reading is above the maximum *TAlrtTh* value. This bit may or may not need to be cleared by system software to detect the next event. See *Config.TS* bit description. Tmx is set to 0 at power-up.

Smx: Maximum SOC Alert Threshold Exceeded. This bit is set to a 1 whenever SOC rises above the maximum *SAlrtTh* value. This bit may or may not need to be cleared by system software to detect the next event. See *Config.SS* and *MiscCFG.SACFG* bit descriptions. Smx is set to 0 at power-up.

PA: Protection Alert. This bit is set to a 1 when there is a protection event. The details of which protection event can be found in the *ProtAlrts* register. This bit must be cleared by system software to detect the next protection event. However, prior to clearing this bit, the ProtAlrts register must first be written to 0x0000. ProtAlrt is set to 0 at power-up.

X: Don't Care. This bit is undefined and can be logic 0 or 1.

Status2 Register (0B0h)

Register Type: Special

Nonvolatile Backup: None

Initial Value: 0x0000

The Status2 register maintains status of hibernate mode. Table 46 shows the Status2 register format.

Table 46. Status2 Register (0B0h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hib	x

Hib: Hibernate Status. This bit is set to a 1 when the device is in hibernate mode or 0 when the device is in active mode. Hib is set to 0 at power-up.

X: Don't Care. This bit is undefined and can be logic 0 or 1.

nBattStatus Register (1A8h)

Battery Status Nonvolatile Register

The Battery Status register contains the permanent battery status information. If nProtCfg.PFen = 1, then a permanent fail results in permanently turning the FETs off to ensure the safety of the battery and the PFAIL pin is driven high.

Table 47. nBattStatus Register (1A8h) Format

D15	D14	D13	D12	D11	D10	D9	D8
PermFail	OVPF	OTPF	CFETFs	DFETFs	FETFo	LDet	ChksumF/UVPF
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LeakCurr							

PermFail—Permanent Failure. This bit is set if any permanent failure is detected.

CFETFs—ChargeFET failure-short detected. If the IC detects that the charge FET is shorted and cannot be opened, it sets the CFETFs bit and the PermFail bit. This function is enabled with nProtCfg.FetPFEn.

DFETFs—DischargeFET failure-short detected. If the IC detects that the discharge FET is shorted and cannot be opened, it sets the DFETFs and the PermFail bit. This function is enabled with nProtCfg.FetPFEn.

FETFo—FET Failure Open. If the IC detects an open FET failure it sets FETFo. In this case, if the IC detects either CHG or DIS FET to have failed open, then it sets FETFo. This function is enabled with nProtCfg.FetPFEn.

LDet—Leakage Detection Fault. This bit is set when a leakage detection fault has been detected.

ChksumF—Checksum Failure. ChksumF protection related NVM configuration registers checksum failure. In the case of a checksum failure, the device sets the PermFail bit but does not write it to NVM in order to prevent using an additional NVM write. This allows the PermFail bit to be cleared by the host so that the INI file can be reloaded.

UVPF—UnderVoltage Permanent Failure. This bit is set when VCell is less than the UnderVoltage Permanent Failure Threshold

LeakCurr—Leakage Current. Leakage current is an unsigned 8-bit result of leakage current from self-discharge in a cell. This field saves the leakage current from the LeakCurrRep register. The LSB for this field is 3.125µV (or 0.625mA with a 5mΩ R_{SENSE} with a range of 0mA to 159.375mA).

nFaultLog Register (1AEh)

This register has dual functionality depending on configuration settings. If nNVCfg2.enFL = 1, the nFaultLog register contains a history of protection events that have been logged at any moment by the device during the log interval and is formatted as shown in Table 48.

Alternatively, if *nNVCfg0*.enAF = 1, the register becomes repurposed for Age Forecasting data. If neither option is enabled, this register can be used as general-purpose user memory.

This register is periodically saved to nonvolatile memory as part of the life-logging function.

Table 48. nFaultLog Register (1AEh) Format

D15	D14	D13	D12	D11	D10	D9	D8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TooHotC	TooColdC	OVP	OCCP	DieHot	Imbalance	UVP	ODCP

ProtStatus Register (0D9h)

The Protection Status register contains the fault states of the protection state machine

Table 49. ProtStatus Register (0D9h) Format

D15	D14	D13	D12	D11	D10	D9	D8
ChgWDT	TooHotC	Full	TooColdC	OVP	OCCP	Qovflw	PreqF
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Imbalance	PermFail	DieHot	TooHotD	UVP	ODCP	ResDFault	Ship

Ship—A flag to indicate the ship state.

PermFail—Permanent Failure Detected. See the *Permanent Failure* section for details.

Discharging Faults:

ODCP - Overdischarge current

UVP - Undervoltage

TooHotD - Overtemperature for discharging

DieHot - Overtemperature for die temperature

Charging Faults:

TooHotC- Overtemperature for charging

OVP - Overvoltage

OCCP - Overcharge current

Qovrflw - Capacity overflow

TooColdC - Undertemperature for charging

Full - Full detection

ChgWDT - Charge communication watchdog timer

DieHot - Overtemperature for die temperature

Imbal - Multicell imbalance

PreqF - Prequal timeout

See the *Protector* section for details of each fault.

ProtAlrt Register (0AFh)

The Protection Alerts register contains a history of any protection events that have been logged by the device and is formatted as shown in Table 50. If any bit of ProtAlrt is 1, then the Status.PA bit is also 1 if Config.ProtAlrtEn = 1. Once a bit is set, it remains set until cleared by the host. The Alert pin is driven low if Config.AEn = 1 and Config.ProtAlrtEn = 1. The bits in ProtAlrt mirror the bits in ProtStatus with the exception of the LDET bit.

Table 50. ProtAlrt Register (0AFh) Format

D15	D14	D13	D12	D11	D10	D9	D8
ChgWDT	TooHotC	Full	TooColdC	OVP	OCCP	Qovflw	PreqF
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Imbalance	PermFail	DieHot	TooHotD	UVP	ODCP	ResDFault	LDet

HProtCfg2 Register (0F1h)

Register Type: Special

Nonvolatile Backup: None

POR Value: 0x0000

The HProtCfg2 Register provides the status of the protection FETs and a variety of other functions as shown in Table 51.

Table 51. HProtCfg2 Register (0F1h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AOLDO							CommOvrd		CPCfg			PBEN		DISs	CHGs

CHGs: CHG FET Status, 1 = On, 0 = Off.

DISs: DIS FET Status, 1 = On, 0 = Off.

PBEN: Pushbutton Enable. 1 = Pushbutton wakeup on ALRT pin is enabled. 0 = Disabled.

CPCfg: Charge Pump Gate Drive Voltage Configuration. 00b = 6V, 01b = 8V, 10b = 10V.

CommOvrd: Command Override Enable. 1 = FET override function enabled. Allows communication to turn off CHG, DIS FETs by writing the CommStat register. 0 = FET override function disabled.

AOLDO: Always-on LDO Configuration.

AOLDO VALUE	DESCRIPTION
00b	AOLDO is disabled.
01b	AOLDO is enabled. Output is 3.4V
10b	AOLDO is enabled. Output is 1.8V.
11b	AOLDO is enabled. Output is 3.4V.

Nonvolatile Memory Status

The IC reports the status of nonvolatile memory operations by updating the NVBusy and NVError bits in the *CommStat* register to indicate when the nonvolatile memory is busy, idle, or if there has been an error.

Analog Measurement Registers

The IC monitors cell pack voltage, cell pack current, cell pack temperature, and the voltage of the cell. This information is provided to the fuel gauge algorithm to predict cell capacity and also made available to the user. Note that ADC related register information is not maintained while the IC is in shutdown mode. The following register information is invalid until the first measurement cycle after the IC returns to active mode of operation.

Voltage Measurement

VCell Register (01Ah)

Register Type: Voltage

Nonvolatile Backup: None

Each update cycle, the lowest reading from all cell voltage measurements is placed in the VCell register. VCell is used as the voltage input to the fuel gauge algorithm.

AvgVCell Register (019h)

Register Type: Voltage

Nonvolatile Backup: None

The AvgVCell register reports an average of the VCell register readings. The time period for averaging is configurable from a 12 second to 24 minute time period. See the *nFilterCfg* register description for details on setting the time filter. The first VCell register reading after power-up or exiting shutdown mode sets the starting point of the AvgVCell register. Note that when a cell relaxation event is detected, the averaging period changes to the period defined by the *RelaxCfg*.dt setting. The register reverts back to its normal averaging period when a charge or discharge current is detected.

Cell1-Cell4 Registers (0D8h-0D5h)

Register Type: Voltage

Nonvolatile Backup: None

Each update cycle, the cell voltage measurement for each cell is placed in appropriate the Cell1-Cell4 register.

AvgCell1-AvgCell4 Registers (0D4h-0D1h)

Register Type: Voltage

Nonvolatile Backup: None

The AvgCell1-AvgCell4 registers report an 8-sample filtered average of the corresponding Cell1-Cell4 register readings.

Batt Register (0DAh)

Register Type: Special

Nonvolatile Backup: None

The Batt registers contains the total pack voltage measured inside the protector on a 20.48V scale with an LSB of 0.3125mV.

PCKP Register (0DBh)

Register Type: Special

Nonvolatile Backup: None

The PCKP register contains the voltage between PACK+ and GND on a 20.48V scale with an LSB of 0.3125mV.

MaxMinVolt Register (0008h)

Register Type: Special

Nonvolatile Backup: Saves to nMaxMinVolt (1ACh) if *nNVCfg2*.enMMV is set (does not restore from nonvolatile).

Initial Value: 0x00FF

The MaxMinVolt register maintains the maximum and minimum of all cell voltage readings since device reset. Each time the voltage registers update, they are compared against these values. If a new voltage channel reading is larger than the maximum or less than the minimum, the corresponding value is replaced with the new reading. At power-up, the maximum voltage value is set to 00h (the minimum) and the minimum voltage value is set to FFh (the maximum). Therefore, both values are updated after the first update. Host software can reset this register by writing it to its power-up value of 0x00FF. The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution. Table 52 shows the register format.

Table 52. MaxMinVolt (008h)/nMaxMinVolt (1ACh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MaxVCELL								MinVCELL							

MaxVCELL: Maximum channel voltage reading (20mV resolution)

MinVCELL: Minimum VCell register reading (20mV resolution)

MaxMinVolt is not cumulative across the entire battery lifetime. After each periodic nonvolatile-memory save, MaxMinVolt resets to 0x00FF to find the next max/min volt across the next segment of battery life. This behavior helps provide a useful log across the battery lifetime where each log segment shows the maximum and minimum voltage experienced across only that segment.

Current Measurement

The IC is able to monitor the current flow through the cell pack by measuring the voltage between the CSN and CSP pins over a ±51.2mV range. While in active mode updates occur in intervals of 351.5ms. In hibernate mode, the update interval is set by the *nHibCfg* register. All ICs are calibrated for current-measurement accuracy at the factory. However, if the application requires, Current register readings can be adjusted by changing the nCGain register setting.

If the application uses a sense resistor with a large temperature coefficient such as a copper metal board trace, current readings can be adjusted based on the temperature measured by the IC. The *CGTempCo* register stores a percentage per degrees Celsius value that is applied to current readings if the *nNVCfg2*.enMet bit is set. If *nNVCfg1*.enMtl = 0, the default temperature coefficient of copper is used for temperature adjustments. If enMtl = 1, the *CGTempCo* register value is used for temperature adjustments.

Additionally, the IC maintains a record of the minimum and maximum current measured by the IC and an average current over a time period defined by the host. Contents of the Current and AvgCurrent registers are indeterminate for the first conversion cycle time period after IC power-up.

Current Measurement Timing

Current measurements are always enabled regardless of *nPackCfg* settings. Current is updated every 351ms.

Current Register (01Ch)

Register Type: Current

Nonvolatile Backup: None

The IC measures the voltage between the CSP and CSN pins and the result is stored as a two's complement value in the Current register. Voltages outside the minimum and maximum register values are reported as the minimum or maximum value. The register value should be divided by the sense resistance to convert to amps. The value of the sense resistor determines the resolution and the full-scale range of the current readings. Table 53 shows range and resolution values for typical sense resistances.

Table 53. Current Measurement Range and Resolution vs. Sense Resistor Value

BATTERY FULL CAPACITY (mAh)	SENSE RESISTOR (mΩ)	nRSENSE	CURRENT REGISTER RESOLUTION (µA)	CURRENT REGISTER RANGE (A)	CAPACITY RESOLUTION (mAh)	MAXIMUM CAPACITY (mAh)
> 4000	1	0064h	1562.5	±51.2	5	144360
> 2000	2	00C8h	781.25	±25.6	2.5	71680
> 800	5	01F4h	312.5	±10.24	1	28672
> 400	10	03E8h	156.25	±5.12	0.5	14336
> 200	20	07D0h	78.125	±2.56	0.25	7168

AvgCurrent Register (01Dh)

Register Type: Current

Nonvolatile Backup: None

The AvgCurrent register reports an average of Current register readings over a configurable 0.7 second to 6.4 hour time period. See the *nFilterCfg* register description for details on setting the time filter. The first Current register reading after returning to active mode sets the starting point of the AvgCurrent filter.

MaxMinCurr Register (00Ah)

Register Type: Special

Nonvolatile Backup: Periodically saves to nMaxMinCurr (1ABh) if *nNVCfg2*.enMMC is set, but does not restore from nonvolatile memory.

Alternate Initial Value: 0x807F

The MaxMinCurr register maintains the maximum and minimum Current register values since the last IC reset or until cleared by host software. Each time the Current register updates, it is compared against these values. If the reading is larger than the maximum or less than the minimum, the corresponding value is replaced with the new reading. At power-up, the maximum current value is set to 80h (the minimum) and the minimum current value is set to 7Fh (the maximum). Therefore, both values are changed to the Current register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum voltages are each stored as two's complement 8-bit values with 0.4mV/RSENSE resolution. Table 54 shows the register format.

Table 54. MaxMinCurr (00Ah)/nMaxMinCurr (1ABh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MaxCurrent								MinCurrent							

MaxCurrent: Maximum Current register reading (0.40mV resolution)

MinCurrent: Minimum Current register reading (0.40mV resolution)

MaxMinCurr is not cumulative across the entire battery lifetime. After each periodic nonvolatile-memory save, MaxMinCurr resets to 0x807F to find the next maximum and minimum current across the next segment of battery life. This behavior helps provide a useful log across the battery lifetime where each log segment shows the maximum and minimum current experienced across only that segment.

nCGain Register (1C8h)

Register Type: Special

Factory Default Value: 4000h

The nCGain register adjusts the gain and offset of the current measurement result. The current measurement ADC is factory trimmed to data-sheet accuracy without the need for the user to make further adjustments. The recommended default for the nCGain register is 0x4000 which applies no adjustments to the Current register reading.

For specific application requirements, the CGain and COff values can be used to adjust readings as follows:

Current Register = (Current ADC Reading × (CGain/256)) + COff

CGain and COff are combined into a single register formatted as shown in Table 55.

Table 55. nCGain Register (1C8h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CGain										COff					

COff: COff has a range of -32 to +31 LSbs. However, it is normally not recommended to calibrate COff. COff = 0 is recommended for most applications.

CGain: The recommended default value of CGain = 0x100 corresponds to a gain of 1. CGain can be calculated as follows: CGain = ((MeasuredCurrent/ReportedCurrent) × 0x0100). CGain is a signed value and can be negative.

CGTempCo (0B8h)/nCGTempCo (1C9h) Register

Register Type: Special

Factory Default Value: 0000h

Alternate Initial Value: 20C8h

Set *nNVCfg2*.enMet = 1 to use CGTempCo to adjust current measurements for temperature. CGTempCo has a range of 0% to 3.1224% per degrees Celsius with a step size of 3.1224/65536 percent per degrees Celsius. If the *nNVCfg1*.enMtl bit is clear, CGTempCo defaults to a value of 20C8h (compensation for copper) or 0.4% per degrees Celsius which is the approximate temperature coefficient of a copper trace. If the *nNVCfg1*.enMtl bit is set, CGTempCo restores from nCGTempCo (1C9h) after IC reset allowing a custom sense resistor temperature coefficient to be used.

nRSense Register (1CFh)

Register Type: Special

Factory Default Value: 01F4h

Nonvolatile Restore: There is no associated restore location for this register.

The nRSense register is the designated location to store the nominal sense resistor value used by the application. This value is not used by the IC as all current and capacity information is reported in terms of µV and µVH. Host software can use the nRSense register value to convert current and capacity information into mA and mAH. It is recommended that the sense resistor value be stored with an LSb weight of 10µΩ giving a range of 10µΩ to 655.35mΩ. Table 53 shows recommended register settings based on common sense resistor values.

Copper Trace Current Sensing

The IC has the ability to measure current using a copper board trace instead of a traditional sense resistor. The main difference being the ability to adjust to the change in sense resistance over temperature. To enable copper trace current sensing, set *nNVCfg2*.enMet = 1. The ICs default temperature adjustment is 0.4% per °C but can be adjusted using the nTCurve register if *nNVCfg1*.enMtl = 1. Note that copper trace current sensing cannot be enabled at the same time as thermistor curve adjustment. For 1-ounce copper, a length to width ratio of 6:1 creates a 0.0035Ω sense resistor which is suitable for most applications. Table 56 summarizes the IC setting for copper trace sensing.

Table 56. Copper Trace Sensing

PARAMETER	SETTING	RESULT
nNVCfg1.enMet	1	Sense resistor temperature compensation enabled.
nNVCfg2.enMlt	0	Sense resistor temperature compensation set to default of 0.4% per °C (typical copper).
nRense	0x012C	Sense resistor indicator to host software set to 0.0035Ω.
R_{SENSE} Size	6:1	A 6:1 length to width ratio of 1oz copper gives a resistance of 0.0035Ω.

Temperature Measurement

The IC measures its own internal die temperature and up to four thermistors. See the *nPackCfg* register for details.

Every 1.4s the IC biases a thermistor with an internal trimmed pullup. After the pullup is enabled, the IC waits for a settling period of tPRE prior to making measurements on the TH(1-4) pin. The active pullup is disabled when temperature

measurements are complete. This feature limits the time the external resistor-divider network is active and lowers the total amount of energy used by the system.

The ratiometric results are converted to temperature using the *nThermCfg* register each time one of the TH(1-4) pins are measured. Proper nThermCfg configuration is needed to achieve thermistor accuracy from -40°C to +85°C. Internal die temperature measurements are factory calibrated and are not affected by nThermCfg register settings.

Additionally, the IC maintains a record of the minimum and maximum temperature measured and an average temperature over a configurable time period. See the *nFilterCfg* for details.

Temperature Measurement Timing

Temperature measurement channels are individually enabled using the nPackCfg register. ADC measurement order and firmware post-processing determine when a valid reading becomes available to the user. In addition, not all channels are measured each time through the firmware task loop. Selection options for enabled channels create a large number of possible timing options. DieTemp is updated every 351ms. Each thermistor measurement is updated every 1.4s x NTherms.

Temp Register (01Bh)

Register Type: Temperature

Nonvolatile Backup: None

The Temp register is the input to the fuel gauge algorithm. The Temp register reflects the highest thermistor temperature if enabled, and the die-temperature if the thermistors are disabled.

AvgTA Register (016h)

Register Type: Temperature

Nonvolatile Backup: None

The AvgTA register reports an average of the readings from the Temp register. The averaging period is configurable from 6 minutes up to 12 hours as set by the FilterCfg register. The first Temp register reading after returning to active mode sets the starting point of the averaging filters.

MaxMinTemp Register (009h)

Register Type: Special

Nonvolatile Backup: Periodically saves to nMaxMinTemp (1ADh) if nNVCfg2.enMMT is set, but does not restore from nonvolatile memory.

Alternate Initial Value: 807Fh

The MaxMinTemp register maintains the maximum and minimum Temp register (01Bh) values since the last fuel-gauge reset or until cleared by host software. Each time the Temp register updates, it is compared against these values. If the reading is larger than the maximum or less than the minimum, the corresponding values are replaced with the new reading. At power-up, the maximum value is set to 80h (minimum) and the minimum value is set to 7Fh (maximum). Therefore, both values are changed to the Temp register reading after the first update. Host software can reset this register by writing it to its power-up value of 807Fh. The maximum and minimum temperatures are each stored as two's complement 8-bit values with 1°C resolution. Table 57 shows the format of the register.

Table 57. MaxMinTemp (009h)/nMaxMinTemp (1ADh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MaxTemperature								MinTemperature							

MaxTemperature: Maximum Temp register reading (1ºC resolution)

MinTemperature: Minimum Temp register reading (1ºC resolution)

MaxMinTemp is not cumulative across the entire battery lifetime. After each periodic nonvolatile memory save, MaxMinTemp resets to 807Fh to find the next maximum and minimum temperatures across the next segment of battery life. This behavior helps provide a useful log across the battery lifetime where each log segment shows the maximum and minimum temperature experienced across only that segment.

nThermCfg Register (1CAh)

Factory Default Value: 71BEh

External NTC thermistors generate a temperature related voltage measured at the TH(1-4) pins. Set nThermCfg register to compensate thermistor for accurate translation of temperature.

Table 58 lists common NTC thermistors with their associated Beta value and the nThermCfg value. The thermistors in the table translate within ±1°C from -40°C to +85°C. For other thermistors, use the equation to translate within ±2.5°C.

Table 58. Register Settings for Common Thermistor Types

THERMISTOR	R_{25C}(kΩ)	BETA @ 25°C-85°C	nTHERMCFG
Murata NCP15XH103F03RC	10	3435	71BEh
Semitec 103AT-2	10	3435	91C3h
TDK B57560G1103 7003	10	3610	5183h
Murata NCU15WF104F6SRC	100	4250	48EBh
NTC TH11-4H104F	100	4510	08D9h
TDK NTCG064EF104FTBX	100	4225	58EFh
Other 10K	10	nThermCfg = 7000h + (3245919/Beta[1] - 512)	
Other 100K	100	nThermCfg = 3000h + (3245919/Beta[1] - 512)	

1. Use Beta 25°C-85°C.

DieTemp Register (034h)

Register Type: Temperature

Nonvolatile Backup: None

This register displays temperature in degrees Celsius, ±128°C or 1°C in the high-byte or 1/256°C LSB.

AvgDieTemp Register (040h)

Register Type: Temperature

Nonvolatile Backup: None

The AvgDieTemp register reports a 4-sample filtered average of the DieTemp register.

Temp1/2/3/4 Registers (13Ah-137h)

Register Type: Temperature

Nonvolatile Backup: None

These registers display temperature readings from thermistor 1/2/3/4 (if enabled) in degrees Celsius, ±128ºC or 1°C in the high-byte or 1/256°C LSB.

AvgTemp1/2/3/4 Registers (136h-133h)

Register Type: Temperature

Nonvolatile Backup: None

The AvgTemp1/2/3/4 registers report a 4-sample filtered average of the Temp1/2/3/4 registers.

Power

Power Register (0B1h)

Instantaneous power calculation from immediate current and voltage. LSB is 1.6mW with a 5mΩ sense resistor.

AvgPower Register (0B3h)

Filtered Average Power from the power register. LSB is 1.6mW with a 5mΩ sense resistor. Filter bits located in Config2.POWR.

Charge Control Registers

ChargingCurrent Register (028h)

Register Type: Current

Nonvolatile Backup: None

The ChargingCurrent register reports the prescribed charging current. See the *Charging Prescription* section for more details.

ChargingVoltage Register (02Ah)

Register Type: Voltage

Nonvolatile Backup: None

The ChargingVoltage register reports the prescribed charging voltage. See the *Charging Prescription* section for more details.

nStepChg Register (1DBh)

Factory Default Value: C884h

The nStepChg register defines the step-charging prescription as shown in Figure 10.

Note: This only effects the ChargingCurrent output register which prescribes a charge current controlled by the external charger. To disable step-charging prescription, set nStepChg = FF00h.

Table 59. nStepChg Register (1DBh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
StepCurr1				StepCurr2				StepdV0				StepdV1			

StepCurr1 and **StepCurr2:** Both of these register bit-fields scale the JEITA zone charge current down by a 4-bit ratio from 1/16 to 16/16.

StepCurrent1 = $ChargingCurrent_{JEITAZONE}$ x StepCurr1/16 = 2000mA x 12/16 = 1500mA

StepCurrent2 = $ChargingCurrent_{JEITAZONE}$ x StepCurr2/16 = 2000mA x 8/16 = 1000mA

StepdV0 and **StepdV1:** These register bit-fields configure StepVolt0 and StepVolt1 relative to the JEITA zone charge voltage. Both registers are negative offsets relative to JEITA ChargeVoltage, and both registers support 10mV LSB.

StepV0 = $ChargingVoltage_{JEITAZONE}$ - (StepdV0 x 10mV) = 4.2V - (8 x 10mV) = 4.12V

StepV1 = $ChargingVoltage_{JEITAZONE}$ - (StepdV1 x 10mV) = 4.2V - (4 x 10mV) = 4.16V

nChgCfg (1C2h) Prequal Configuration

Set nProtCfg.PreqEn to enable the prequal charging feature and configure the settings as shown in Table 60. Set nChgCtl (1C3h) = 00E1h for proper operation.

Factory Default nChgCfg Value: 2061h

Factory Default nChgCtl Value: 00E1h

The IC regulates the CHG gate voltage in order to control/limit the following:

- Charge Current
- CHG FET and DIS FET Temperature (using DieTemp)

When a charge source is applied, the charge FET is slowly turned on by the IC to allow the current to flow. It may take approximately 1 minute for the charge current to begin to flow when in prequal mode.

Table 60. nChgCfg Register (1C2h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	PreQualVolt					HeatLim			PreChgCurr				

PreQualVolt: Sets the prequal voltage. Prequal Voltage = UVP + PreQualVolt x 20mV, PreQualVolt is a signed 2's compliment value with range of UVP – 320mV to UVP + 300mV.

PreChgCurr: Sets the precharging current for the ChargingCurrent register. Precharge current is calculated as:

PreChargeCurrent = nJEITAC.RoomChargingCurrent x (PreChgCurr + 1)/128 (range from RoomChargingCurrent/128 to RoomChargingCurrent/4)

HeatLim: Set HeatLim to limit the thermal dissipation in the protection FETs during prequal regulation. Set HeatLim from 102mW to 819mW in 102mW steps. The effective power-dissipation limit is (HeatLim + 1) x 102mW.

ModelGauge m5 Algorithm Registers

ModelGauge m5 Registers

For accurate results, ModelGauge m5 uses information about the cell and the application as well as the real-time information measured by the IC. Figure 27 shows inputs and outputs to the algorithm grouped by category. Analog input registers are the real-time measurements of voltage, temperature, and current performed by the IC. Application-specific registers are programmed by the customer to reflect the operation of the application. The Cell Characterization Information registers hold characterization data that models the behavior of the cell over the operating range of the application. The Algorithm Configuration registers allow the host to adjust the performance of the IC for its application. The Learned Information registers allow an application to maintain the accuracy of the fuel gauge as the cell ages. The register description sections describe each register function in detail.

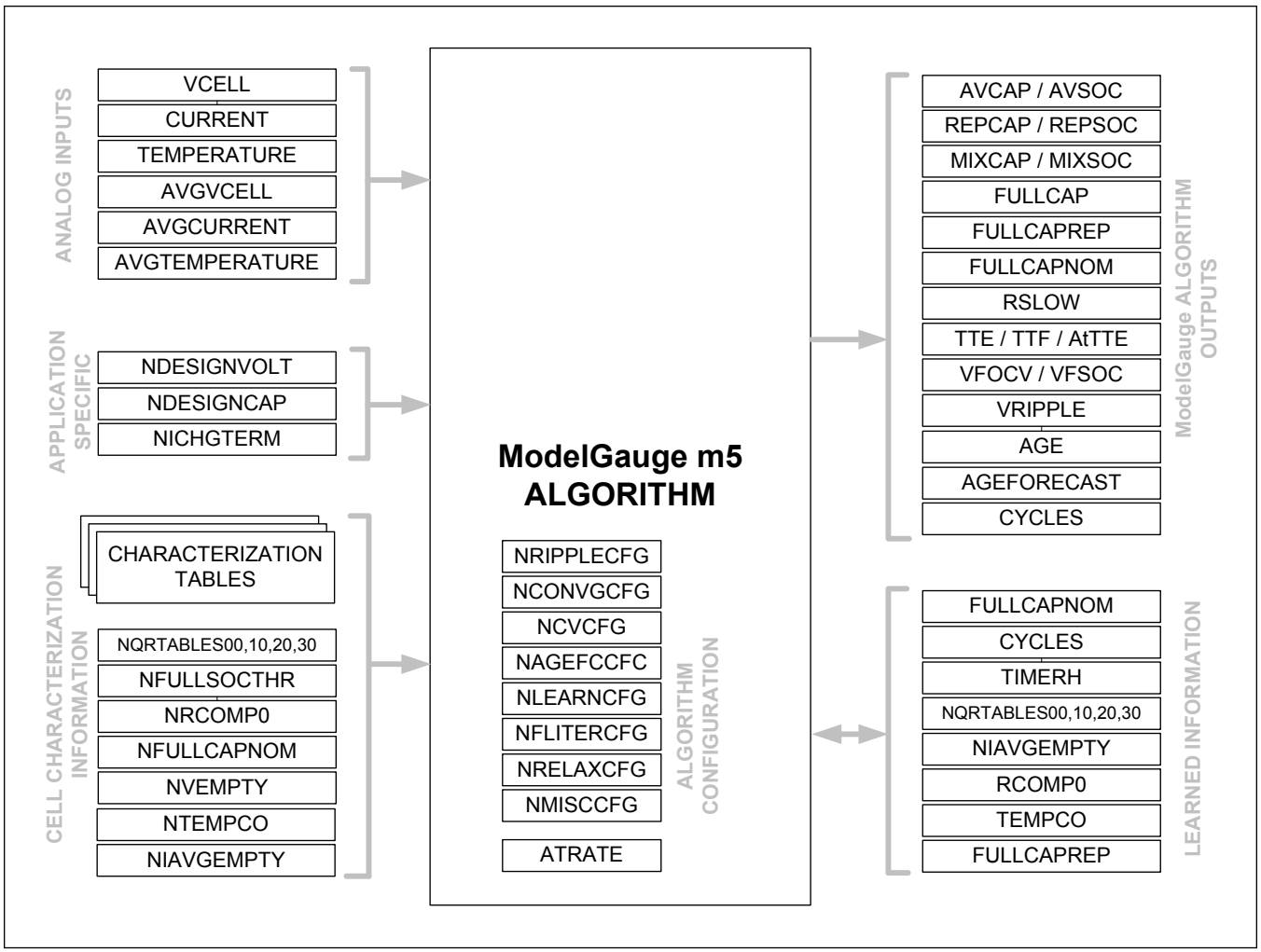


Figure 27. ModelGauge m5 Registers

ModelGauge m5 Algorithm Output Registers

The following registers are outputs from the ModelGauge m5 algorithm. The values in these registers become valid 480ms after the IC is reset.

RepCap Register (005h)

Register Type: Capacity

Nonvolatile Backup: None

RepCap or Reported Capacity is a filtered version of the AvCap register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in temperature or load current. See the *Fuel-Gauge Empty Compensation* section for details.

RepSOC Register (006h)

Register Type: Percentage

Nonvolatile Backup: None

RepSOC is a filtered version of the AvSOC register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in load current. RepSOC corresponds to RepCap and FullCapRep. RepSOC

is intended to be the final state-of-charge percentage output for use by the application. See the *Fuel-Gauge Empty Compensation* section for details.

FullCapRep Register (010h)

Register Type: Capacity

Nonvolatile Backup and Restore: nFullCapRep (1A9h) or nFullCapNom (1A5h)

This register reports the full capacity that goes with RepCap, generally used for reporting to the user. A new full-capacity value is calculated at the end of every charge cycle in the application.

TTE Register (011h)

Register Type: Time

Nonvolatile Backup: None

The TTE register holds the estimated time-to-empty for the application under present temperature and load conditions. The TTE value is determined by dividing the AvCap register by the AvgCurrent register. The corresponding AvgCurrent filtering gives a delay in TTE empty, but provides more stable results. The TTE register has a maximum value of 102.3 hours. When TTE is larger than the maximum value, the TTE register saturates and contains the maximum value (FFFFh). The host can calculate times longer than the maximum value with the following equation:

$$TTE_{CALCULATED}\ (hours) = AvCap(mAh)/AvgCurrent(mA)$$

See the *Typical Operating Characteristics* for sample performance.

TTF Register (020h)

Register Type: Time

Nonvolatile Backup: None

The TTF register holds the estimated time-to-full for the application under present conditions. The TTF value is determined by learning the constant current and constant voltage portions of the charge cycle based on experience of prior charge cycles. Time-to-full is then estimated by comparing the present charge current to the charge termination current. Operation of the TTF register assumes all charge profiles are consistent in the application. See the *nTTFCfg* for configuration and the *Typical Operating Characteristics* for sample performance.

Age Register (007h)

Register Type: Percentage

Nonvolatile Backup: None

The Age register contains a calculated percentage value of the application's present cell capacity compared to its expected capacity. The result can be used by the host to gauge the battery pack health as compared to a new pack of the same type. The equation for the register output is:

$$Age\ Register = 100\% \times (FullCapNom\ Register/DesignCap\ Register)$$

Cycles Register (017h) and nCycles (1A4h)

Register Type: Special

Nonvolatile Backup and Restore: nCycles (1A4h)

The Cycles register maintains a total count of the number of charge/discharge cycles of the cell that have occurred. The result is stored as a percentage of a full cycle. For example, a full charge/discharge cycle results in the Cycles register incrementing by 100%. The Cycles register has a full range of 0 to 16383 cycles with a 25.0% LSb. Cycles is periodically saved to nCycles to provide a long term nonvolatile cycle count.

Table 61. Cycles Register (017h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CycleCount (LSb 25%)															

Table 62. nCycles Register (1A4h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CycleCount (LSb 25%, 50%, 100%, or 200%)													nFib		

The LSb of Cycles register is 25%.

The LSb of nCycles.CycleCount depends on the setting of nNVCfg2.fibScl as shown in Table 63.

Configure nFib = 0 for any new pack. nFib is a reset counter which controls Fibonacci-saving reset accelleration (see the *100 Record Life Logging* section). Each reset followed by any nonvolatile save increases by 1. Maximum value is 7 without overflow.

Table 63. nNVCfg2.FibScl Setting Determines LSb of nNVCfg2.CyclesCount

NNVCFG2.FIBSCL	NCYCLES.CYCLECOUNT LSB
00b	25%
01b	50%
10b	100%
11b	200%

Timer Register (03Eh)

Register Type: Special

Nonvolatile Backup: None

Initial Value: 0x0000

This register holds timing information for the fuel gauge. It is available to the user for debugging purposes. The Timer register LSb is equal to 175.8ms giving a full-scale range of 0 to 3.2 hours.

TimerH Register (0BEh)

Register Type: Special

Nonvolatile Backup and Restore: nTimerH (1AFh) if *nNVCfg2*.enT is set

Alternate Initial Value: 0000h

This register allows the IC to track the age of the cell. An LSb of 3.2 hours gives a full-scale range for the register of up to 23.94 years. If enabled, this register is periodically backed up to nonvolatile memory as part of the learning function.

FullCap Register (035h)

Register Type: Capacity

Nonvolatile Restore: Derived from nFullCapNom (1A5h)

This register holds the calculated full capacity of the cell based on all inputs from the ModelGauge m5 algorithm including empty compensation. A new full-capacity value is calculated continuously as application conditions change.

nFullCapNom Register (1A5h)

Register Type: Capacity

Nonvolatile Backup and Restore: FullCapNom (023h)

This register holds the calculated full capacity of the cell, not including temperature and empty compensation. A new full-capacity nominal value is calculated each time a cell relaxation event is detected. This register is used to calculate other outputs of the ModelGauge m5 algorithm.

RCell Register (014h)

Register Type: Resistance

Nonvolatile Backup: None

Initial Value: 0290h

The RCell register displays the calculated internal resistance of the cell or the average internal resistance of each cell in the cell stack. RCell is determined by comparing open-circuit voltage (VFOCV) against measured voltage (VCell) over a long time period while under load current.

VRipple Register (0B2h)

Register Type: Special

Nonvolatile Backup: None

Initial Value: 0000h

The VRipple register holds the slow average RMS value of the VCell register reading variation compared to the AvgVCell register. The default filter time is 22.5s. See the *nRippleCfg* register description. VRipple has an LSb weight of 1.25mV/128.

nVoltTemp Register (1AAh)

Register Type: Special

Nonvolatile Backup: AvgVCell and AvgTA registers if *nNVCfg2*.enVT = 1.

This register has dual functionality depending on configuration settings. If *nNVCfg2*.enVT = 1, this register provides nonvolatile back up of the AvgVCell and AvgTA registers as shown in Table 64.

Table 64. nVoltTemp Register (1AAh) Format when nNVCfg2.enVT = 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AvgVCell Upper 9 Bits									AvgTA Upper 7 Bits						

Alternatively, if *nNVCfg0*.enAF = 1, this register stores an accumulated age slope value to be used with the Age Forecasting algorithm. Regardless of which option is enabled, this register is periodically saved to nonvolatile memory as part of the learning function. If neither option is enabled, this register can be used as general-purpose user memory.

ModelGauge m5 Algorithm Input Registers

The following registers are inputs to the ModelGauge algorithm and store characterization information for the application cells as well as important application-specific specifications. They are described only briefly here. Contact Maxim for information regarding cell characterization.

nXTable0 (180h) to nXTable11 (18Bh) Registers

Register Type: Special

Nonvolatile Restore: There are no associated restore locations for these registers.

Cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions. This table comes from battery characterization data. These are nonvolatile memory locations.

nOCVTable0 (190h) to nOCVTable11 (19Bh) Registers

Register Type: Special

Nonvolatile Restore: There are no associated restore locations for these registers.

Cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions. This table comes from battery characterization data. These are nonvolatile memory locations.

nQRTable00 (1A0h) to nQRTable30 (1A3h) Registers

Register Type: Special

Nonvolatile Backup and Restore: QRTable00 to QRTable30 (012h, 022h, 032h, 042h)

Factory Default Values: QRTable00 to QRTable30 (1050h, 8002h, 078Ch, 0880h)

The nQRTable00 to nQRTable30 register locations contain characterization information regarding cell capacity that is not available under certain application conditions.

nFullSOCThr Register (1C6h)

Register Type: Percentage

Nonvolatile Restore: FullSOCThr (013h) if nNVCfg1.enFT is set.

Alternate Initial Value: 80%

The nFullSOCThr register gates detection of end-of-charge. VFSOC must be larger than the nFullSOCThr value before nIChgTerm is compared to the AvgCurrent register value. The recommended nFullSOCThr register setting for most custom characterized applications is 95% . For EZ performance applications, the recommendation is 80% (5005h). See the nIChgTerm register description and *End-of-Charge Detection* section for details. Table 65 shows the register format.

Table 65. nFullSOCThr (1C6h)/FullSOCThr (013h) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
nFullSOCThr													1	0	1

nVEmpty Register (19Eh)

Register Type: Special

Nonvolatile Restore: VEmpty (03Ah) if *nNVCfg0*.enVE is set.

Alternate Initial Value: 9659h (3.0V/3.56V)

The nVempty register sets thresholds related to empty detection during operation. Table 66 shows the register format.

Table 66. VEmpty (03Ah)/nVEmpty (19Eh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VE									VR						

VE: Empty Voltage. Sets the voltage level for detecting empty. A 10mV resolution gives a 0 to 5.11V range. This value is written to 3.3V after reset if nonvolatile backup is disabled.

VR: Recovery Voltage. Sets the voltage level for clearing empty detection. Once the cell voltage rises above this point, empty voltage detection is re-enabled. A 40mV resolution gives a 0 to 5.08V range. This value is written to 3.88V after reset if nonvolatile backup is disabled.

nDesignCap Register(1B3h)

Register Type: Capacity

Nonvolatile Restore: DesignCap (018h) if nNVCfg0.enDC is set

Alternate Initial Value: FullCapRep register value

The nDesignCap register holds the expected capacity of the cell. This value is used to determine age and health of the cell by comparing against the measured present cell capacity.

nIChgTerm Register (19Ch)

Register Type: Current

Nonvolatile Restore: IChgTerm (01Eh) if nNVCfg0.enICT is set

Alternate Initial Value: 1/3rd the value of the nFullCapNom register (corresponds to C/9.6)

The nIChgTerm register allows the device to detect when a charge cycle of the cell has completed. nIChgTerm should

be programmed to the exact charge termination current used in the application. The device detects end-of-charge if all the following conditions are met:

• VFSOC Register > FullSOCThr Register

• AND IChgTerm x 0.125 < Current Register < IChgTerm x 1.25

• AND IChgTerm x 0.125 < AvgCurrent Register < IChgTerm x 1.25

See the *End-of-Charge Detection* section for more details.

nRComp0 Register (1A6h)

Register Type: Special

Nonvolatile Restore: RComp0 (038h)

The nRComp0 register holds characterization information critical to computing the open circuit voltage of a cell under loaded conditions.

nTempCo Register (1A7h)

Register Type: Special

Nonvolatile Restore: TempCo (039h)

The nTempCo register holds temperature compensation information for the nRComp0 register value.

ModelGauge m5 Algorithm Configuration Registers

The following registers allow operation of the ModelGauge m5 algorithm to be adjusted for the application. It is recommended that the default values for these registers be used.

nConfig Register (1B0h)

Register Type: Special

Factory Default Value: 2290h

Nonvolatile Restore: Config (00Bh) and Config2 (0ABh)

The nConfig register holds all shutdown enable, alert enable, and temperature enable control bits. Writing a bit location enables the corresponding function within one task period. Table 67, Table 68, and Table 69 show the register formats.

Table 67. nConfig Register (1B0h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PAen	SS	TS	VS	FIFOen	PBen	DisBlockRead	0	AtRateEn	COMMSH	ALSH	1	FTHRM	Aen	dSOCen	TAlrtEn

Table 68. Config Register (00Bh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	SS	TS	VS	DisLDO	PBen	DisBlockRead	0	SHIP	COMMSH	0	ETHRM	FTHRM	Aen	0	PAen

Table 69. Config2 Register (0ABh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
POR_CMD	0	AtRtEn	ADCFIFOen	POWR				dSOCen	TAlrtEn	0	1	DRCfg		0	0

0: Bit must be written 0. Do not write 1.

1: Bit must be written 1. Do not write 0.

PAen: Protection Alert Enable. Set PAen = 1 to enable this feature that saves the protector faults (TooHotC, TooColdC, OVP, OCCP, DieHot, TooHotD, UVP, ODCP, LDet) into the low byte of the nBattStatus register. After each life logging write to NVM, the low byte of nBattStatus is cleared.

PBEn: PushButton Enable. Set PBEn = 1 to enable wakeup by pushbutton. This application allows a product to be completely sealed with battery disconnected until a shared system button is pressed.

Aen: Enable Alert on Fuel-Gauge Outputs. When Aen = 1, violation of any of the alert threshold register values by temperature, voltage, or SOC triggers an alert. This bit affects the ALRT pin operation only. The Smx, Smn, Tmx, Tmn, Vmx, Vmn, Imx, and Imn bits of the Status register (000h) are not disabled. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.

FTHRM: Force Thermistor Bias Switch. This allows the host to control the bias of the thermistor switch or enable fast detection of battery removal. Set FTHRM = 1 to always enable the thermistor bias switch. With a standard 10kΩ thermistor, this adds an additional 200µA, approximately, to the current drain of the circuit.

ETHRM: Enable Thermistor. Set to logic 1 to enable the automatic TH output bias and TH measurement.

COMMSH: Communication Shutdown. Set to logic 1 to force the device to enter shutdown mode if both SDA and SCL are held low (I^2C version) or DQ is held low (1-Wire version) for more than the timeout of the ShdnTimer register. This also configures the device to wake up on a rising edge of any communication. Note that if COMMSH is set to 0, the device wakes up an edge of any of the SDA/DQ or SCL/OD pins. See the *Modes of Operation* section.

SHIP: Ship or Deepship Command. Write this bit to logic 1 to force into ship or deepship mode based on nProtCfg.DeepShpEn. Both FETs open within 1.4s and the IC will fully enter ship or deepship after timeout of the Shutdown Timer register which is configured in *nDelayCfg.UVPTimer*. SHIP is reset to 0 at power-up and upon exiting ship or deepship mode.

VS: Voltage ALRT Sticky. When VS = 1, voltage alerts can only be cleared through software. When VS = 0, voltage alerts are cleared automatically when the threshold is no longer exceeded.

TS: Temperature ALRT Sticky. When TS = 1, temperature alerts can only be cleared through software. When TS = 0, temperature alerts are cleared automatically when the threshold is no longer exceeded.

SS: SOC ALRT Sticky. When SS = 1, SOC alerts can only be cleared through software. When SS = 0, SOC alerts are cleared automatically when the threshold is no longer exceeded.

POR_CMD: Firmware Restart. Set this bit to 1 to restart IC firmware operation without performing a recall of nonvolatile memory into RAM. This allows different IC configurations to be tested without changing nonvolatile memory settings. This bit is set to 0 at power-up and automatically clears itself after firmware restart.

TAlrten: Temperature Alert Enable. Set this bit to 1 to enable temperature based alerts. Write this bit to 0 to disable temperature alerts. This bit is set to 1 at power-up.

dSOCen: SOC Change Alert Enable. Set this bit to 1 to enable the Status.dSOCi bit function. Write this bit to 0 to disable the Status.dSOCi bit. This bit is set to 0 at power-up.

DRCfg: Deep Relax Time Configuration. 00b for 0.8 hours to 1.6 hours, 01b for 1.6 hours to 3.2 hours, 10b for 3.2 hours to 6.4 hours and 11b for 6.4 hours to 12.8 hours.

POWR: Sets the time constant for the AvgPower register. The default POR value of 0000b gives a time constant of 0.7s. The equation setting the period is:

$$\text{AvgPower time constant} = 45s \times 2^{(POWR-6)}$$

FIFOen: ADC FIFO Enable. See the *16-reading ADC FIFO* section for details. Set nConfig.ADCFIFOen = 1 to enable continuous acquisition mode for ADC FIFO. Set nConfig.ADCFIFOen = 0 to disable continuous acquisition mode for ADC FIFO. If continuous mode is disabled, a single-cycle acquisition mode for ADC FIFO is enabled by setting Config2.ADCFIFOen = 1.

DisLDO: Disable AOLDO. Set DisLDO to 1 to disable the Always-On LDO if it is enabled in *nPackCfg.AOCfg*.

DisBlockRead: Disable SBS Block Read. Set DisBlockRead to 1 for normal read access in the 16h memory space. Clear DisBlockRead to 0 to enable SBS block reads when SBS Mode is enabled with nNVCfg0.SBSen. The default setting for DisBlockRead is 1.

nNVCfg0 Register (1B8h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

Factory Default Value: 0A00h

The nNVCfg0 register manages nonvolatile memory backup of device and fuel gauge register RAM locations. Each bit of the nNVCfg0 register, when set, enables a given register location to be restored from a corresponding nonvolatile memory location after reset of the IC. If nonvolatile restore of a given register is not enabled, that location initializes to a default value after reset instead. See the individual register descriptions for details. Table 70 shows the nNVCfg0 register format.

Table 70. nNVCfg0 Register (1B8h) Format

D15	D14	D13	D12	D11	D10	D9	D8
enOCV	enX	enSHA	0	1	enFCfg	enRCfg	enLCfg
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
enICT	enDP	enVE	enDC	enMC	enAF	SBSen2	enSBS

enSBS: Enable SBS on DevName 4209h. This bit enables SBS functions of the IC with DevName 4209h. See the *SBS* section. When set, all registers accessed with the SBS 2-Wire address are regularly updated. When this bit and SBSen2 are clear, all SBS related nonvolatile configuration register locations can be used as general-purpose user memory. In addition, setting enSBS = 1 enables the bus timeout hardware required for proper SMBus support. If enSBS = 1, set SBSen2 = 0.

SBSen2 : Enable SBS on DevName 420Ah or newer. This bit enables SBS functions of the IC with DevName 420Ah or newer. See the *SBS* section. When set, all registers accessed with the SBS 2-Wire address are regularly updated. When this bit and SBSen are clear, all SBS related nonvolatile configuration register locations can be used as general-purpose user memory. In addition, setting SBSen2 = 1 enables the bus timeout hardware required for proper SMBus support. If SBS2en = 1, set enSBS = 0.

enAF: Enable Age Forecasting. Set this bit to enable Age Forecasting functionality. When this bit is clear, *nAgeFcCfg* can be used for general-purpose data storage. When set, *nVoltTemp* becomes repurposed for Age Forecasting data. When enAF is set to 1, *nNVCfg2.enVT* and *nNVCfg2.enFL* must be 0 for proper operation.

enMC: Enable *MiscCfg* restore. Set this bit to enable *MiscCfg* register to be restored after reset by the *nMiscCfg* register. When this bit is clear, MiscCfg restores with its alternate initialization value and nMiscCfg can be used for general-purpose data storage.

enDC: Enable DesignCap restore. Set this bit to enable DesignCap register to be restored after reset by the *nDesignCap* register. When this bit is clear, DesignCap restores with its alternate initialization value and nDesignCap can be used for general-purpose data storage.

enVE: Enable VEmpty restore. Set this bit to enable VEmpty register to be restored after reset by the *nVEmpty* register. When this bit is clear, VEmpty restores with its alternate initialization value (3.0V) and nVEmpty can be used for general-purpose data storage.

enDP: Enable Dynamic Power. Set this bit to enable Dynamic Power calculations. When this bit is set to 0, Dynamic Power calculations are disabled and registers MaxPeakPower/SusPeakPower/MPPCurrent/SPPCurrent can be used as general-purpose memory.

enICT: Enable IChgTerm restore. Set this bit to enable IChgTerm register to be restored after reset by the *nIChgTerm* register. When this bit is clear, IChgTerm restores to a value of 1/3 C-rate (from FullCapNom) and nIChgTerm can be used for general-purpose data storage.

enLCfg: Enable LearnCfg restore. Set this bit to enable LearnCfg register to be restored after reset by the nLearnCfg register. When this bit is clear, LearnCfg restores with its alternate initialization value and nLearnCfg can be used for general-purpose data storage.

enRCfg: Enable RelaxCfg restore. Set this bit to enable RelaxCfg register to be restored after reset by the nRelaxCfg register. When this bit is clear, RelaxCfg restores with its alternate initialization value and nRelaxCfg can be used for

general-purpose data storage.

enFCfg: Enable FilterCfg restore. Set this bit to enable the FilterCfg register to be restored after reset by the nFilterCfg register. When this bit is clear, FilterCfg restores with its alternate initialization value and nFilterCfg can be used for general-purpose data storage.

enSHA: Set to 1 to configure the MTP at address 0x1DC to 0x1DF as SHA space. Set to 0 to configure address 0x1DC to 0x1DF as user MTP.

enX: Enable XTable restore. Set this bit to enable nXTable register locations to be used for cell characterization data. When this bit is clear, the IC uses the default cell model and all nXTable register locations can be used as general-purpose user memory.

enOCV: Enable OCVTable restore. Set this bit to enable nOCVTable register locations to be used for cell characterization data. When this bit is clear, the IC uses the default cell model and all nOCVTable register locations can be used as general-purpose user memory.

nNVCfg1 Register (1B9h)

Register Type: Special

Factory Default Value: 0182h

Nonvolatile Restore: There is no associated restore location for this register

The nNVCfg1 register manages nonvolatile memory restore of device and fuel gauge register RAM locations. Each bit of the nNVCfg1 register, when set, enables a given register location to be restored from a corresponding nonvolatile memory location after reset of the IC. If nonvolatile backup of a given register is not enabled, that location initializes to a default value after reset instead. See the individual register descriptions for details. Table 71 shows the nNVCfg1 register format.

Table 71. nNVCfg1 Register (1B9h) Format

D15	D14	D13	D12	D11	D10	D9	D8
0	enMtl	enFTh	0	0	enJP	enSC	enProt
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
enJ	enProtChksm	0	enTTF	enAT	0	enCTE	0

enProt: Enable Protector. Set this bit to enable the protector. When this bit is clear, protector is disabled.

enJ: Enable ChargingCurrent and ChargingVoltage. Set this bit to 1 to enable ChargingCurrent and ChargingVoltage update feature.

enJP: Enable Protection with JEITA (temperature region dependent). Set this bit to 1 to enable JEITA Protection. Clear this bit to disable JEITA protection and make OVP and OCCP thresholds become flat.

enSC: Enable special chemistry model. Set this bit to 1 if a special chemistry model is used. This bit enables the use of nScOcvLim.

enCTE: Enable Converge-to-Empty. Set this bit to enable the *nConvgCfg* register settings to affect the converge to empty functionality of the IC. When this bit is clear, converge-to-empty is disabled and nConvgCfg can be used for general-purpose data storage.

enAT: Enable Alert Thresholds. Set this bit to enable IAlrtTh, VAlrtTh, TAlrtTh, and SAlrtTh registers to be restored after reset by the nIAlrtTh, nVAlrtTh, nTAlrtTh, and nSAlrtTh registers respectively. When this bit is clear these registers restore with their alternate initialization values and the nonvolatile locations can be used for general-purpose data storage.

enTTF: Enable time-to-full configuration. Set to 1 to enable *nTTFCfg* (configures CVMixCap and CVHalftime) for tuning of Time-To-Full performance. Otherwise, CVMixCap and CVHalftime restore to their alternate initialization values and nTTFCfg can be used for general-purpose data storage.

enFTh: Enable FullSOCThr configuration restore. Set this bit to enable FullSOCThr register to be restored after reset by the *nFullSOCThr* register. When this bit is clear FullSOCThr restores with its alternate initialization value (80%) and nFullSOCThr can be used for general-purpose data storage.

enMtl: Enable CGTempCo restore. Set this bit to enable CGTempCo register to be restored after reset by the nTCurve register. When this bit is clear CGTempCo restores with its alternate initialization value (copper). nTCurve can be used for general-purpose data storage if enMtl is clear.

enProtChksm: Enable protector checksum function.

x: Don't care.

nNVCfg2 Register (1BAh)

Register Type: Special

Factory Default Value: BE2Dh

Nonvolatile Restore: There is no associated restore location for this register

The nNVCfg2 register manages nonvolatile memory backup and restore of device and fuel gauge register RAM locations. Each bit of the nNVCfg2 register, when set, enables a given register location to be restored from or backed up to a corresponding nonvolatile memory location after reset of the IC. If nonvolatile backup of a given register is not enabled, that location initializes to a default value after reset instead. See the individual register descriptions for details. Table 72 shows the nNVCfg2 register format.

Table 72. nNVCfg2 Register (1BAh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
enT	0	enMMT	enMMV	enMMC	enVT	enFC	0	enMet	0	enFL	FibMax			FibScl	

FibMax/FibScl: Set the FibMax and FibScl "Fibonacci Saving" interval to provide recurring log-saving according to the expected battery lifespan. See the *100 Record Life Logging* section for more details.

enFL: Fault Logging. Set EnFL to store protector faults into nFaultLog.LowByte as shown in Table 48. EnFL is not compatible with Age Forecasting. nFaultLog can be used as general-purpose memory if not used for fault logging or age forecasting.

enFC: Enable FullCap and FullCapRep backup and restore. Set this bit to enable FullCap and FullCapRep registers to be restored after reset by the *nFullCapRep* register and FullCapRep to backup to nFullCapRep. When this bit is clear FullCap and FullCapRep registers restore from the nFullCapNom register. nFullCapRep can then be used as general-purpose user memory.

enMMC: Enable MaxMinCurr Backup. Set this bit to enable storage of MaxMinCurr register information into the nMaxMinCurr register during save operations. When this bit is clear nMaxMinCurr can be used as general-purpose memory.

enMMV: Enable MaxMinVolt Backup. Set this bit to enable storage of MaxMinVolt register information into the nMaxMinVolt register during save operations. When this bit is clear nMaxMinVolt can be used as general-purpose memory.

enMMT: Enable MaxMinTemp Backup. Set this bit to enable storage of MaxMinTemp register information into the nMaxMinTemp register during save operations. EnMMT is incompatible with nNVCFG2.enFL. When enMMT and enFL bits are clear, nMaxMinTemp can be used as general-purpose memory.

enT: Enable TimerH backup and restore. Set this bit to enable TimerH register to be backed up and restored by the *nTimerH* register. When this bit is clear TimerH restores with its alternate initialization value and nTimerH can be used as general-purpose memory.

enVT: Enable Voltage and Temperature backup. Set this bit to enable storage of AvgVCell and AvgTA register information into the *nVoltTemp* register during save operations. When this bit and *nNVCfg0.enAF* are clear nVoltTemp can be used as general-purpose memory. Note that enVT should not be set simultaneously with *nNVCfg0.enAF* (AgeForecasting) and *nNVCfg2.enFL* (Fault Logging).

enMet: Enable metal current sensing. Setting this bit to 1 enables temperature compensation of current readings for allowing copper trace current sensing. See also *nNVCfg1.enMtl*, which enables nTCurve register operation for adjustment of the current sensing temperature coefficient.

nHibCfg Register (1BBh)

Register Type: Special

Factory Default Value: 0909h

Nonvolatile Restore: None

The nHibCfg register controls hibernate mode functionality. The IC enters hibernate mode, if the measured system current falls below the HibThreshold setting for longer than the HibEnterTime delay. While in hibernate mode the IC reduces its operating current by slowing down its task period as defined by the HibScalar setting. The IC automatically returns to active mode of operation if current readings go above the HibThreshold setting for longer than the HibExitTime delay. Table 73 shows the register format.

Table 73. nHibCfg Register (1BBh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EnHib	HibEnterTime			HibThreshold				0	0	0	HibExitTime		HibScalar		

0: Bit must be written 0. Do not write 1.

HibScalar: Sets the task period while in hibernate mode based on the following equation:

$$\text{Hibernate Mode Task Period(s)} = 702\text{ms} \times 2^{(\text{HibScalar})}$$

HibExitTime: Sets the required time period of consecutive current readings above the HibThreshold value before the IC exits hibernate and returns to active mode of operation.

$$\text{Hibernate Mode Exit Time(s)} = (\text{HibExitTime} + 1) \times 702\text{ms} \times 2^{(\text{HibScalar})}$$

HibThreshold: Sets the threshold level for entering or exiting hibernate mode. The threshold is calculated as a fraction of the full capacity of the cell using the following equation:

$$\text{Hibernate Mode Threshold(mA)} = (\text{FullCap(mAh)}/0.8\text{hr})/2^{(\text{HibThreshold})}$$

HibEnterTime: Sets the time period that consecutive current readings must remain below the HibThreshold value before the IC enters hibernate mode as defined by the following equation. The default HibEnterTime value of 000b causes the IC to enter hibernate mode if all current readings are below the HibThreshold for a period of 5.625 seconds, but the IC could enter hibernate mode as quickly as 2.812 seconds.

$$2.812\text{s} \times 2^{(\text{HibEnterTime})} < \text{Hibernate Mode Entry Time} < 2.812\text{s} \times 2^{(\text{HibEnterTime} + 1)}$$

EnHib: Enable Hibernate Mode. When set to 1, the IC enters hibernate mode if conditions are met. When set to 0, the IC always remains in active mode of operation.

nFilterCfg Register (19Dh)

Register Type: Special

Nonvolatile Restore: FilterCfg (029h) if *nNVCfg0.enFCfg* is set.

Alternate Initial Value: 0EA4h

The nFilterCfg register sets the averaging time period for all ADC readings, for mixing OCV results, and coulomb count results. It is recommended that these values are not changed unless absolutely required by the application. Table 74 shows the nFilterCfg register format.

Table 74. FilterCfg (029h)/nFilterCfg (19Dh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	TEMP			MIX				VOLT			CURR			

CURR: Sets the time constant for the AvgCurrent register. The default POR value of 0100b gives a time constant of 5.625s. The equation setting the period is:

$$\text{AvgCurrent time constant} = 45\text{s} \times 2^{(\text{CURR}-7)}$$

VOLT: Sets the time constant for the AvgVCell register. The default POR value of 010b gives a time constant of 45.0s. The equation setting the period is:

$$\text{AvgVCell time constant} = 45s \times 2^{(VOLT-2)}$$

MIX: Sets the time constant for the mixing algorithm. The default POR value of 1101b gives a time constant of 12.8 hours. The equation setting the period is:

$$\text{Mixing Period} = 45s \times 2^{(MIX-3)}$$

TEMP: Sets the time constant for the AvgTA register. The default POR value of 0001b gives a time constant of 1.5 minutes. The equation setting the period is:

$$\text{AvgTA time constant} = 45s \times 2^{TEMP}$$

0: Write these bits to 0.

nMiscCfg Register (1B2h)

Register Type: Special

Nonvolatile Restore: MiscCfg (00Fh) if *nNVCfg0.enMC* is set

Alternate Initial Value: 0x3070

The nMiscCfg control register enables various other functions of the device. The nMiscCfg register default values should not be changed unless specifically required by the application. Table 75 shows the register format.

Table 75. MiscCfg (00Fh)/nMiscCfg (1B2h) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FUS				0	0	MR					1	0	0	SACFG	

0: Bit must be written 0. Do not write 1.

1: Bit must be written 1. Do not write 0.

SACFG: SOC Alert Config. SOC Alerts can be generated by monitoring any of the SOC registers as follows. SACFG defaults to 00 at power-up:

- 00: SOC Alerts are generated based on the RepSOC register.
- 01: SOC Alerts are generated based on the AvSOC register.
- 10: SOC Alerts are generated based on the MixSOC register.
- 11: SOC Alerts are generated based on the VFSOC register.

MR: Mixing Rate. This value sets the strength of the servo mixing rate after the final mixing state has been reached (> 2.08 complete cycles). The units are MR0 = 6.25µV, giving a range up to 19.375mA with a standard 0.010Ω sense resistor. Setting this value to 00000b disables servo mixing and the IC continues with time-constant mixing indefinitely. The default setting is 18.75µV or 1.875mA with a standard sense resistor.

FUS: Full Update Slope. This field prevents jumps in the RepSOC and FullCapRep registers by setting the rate of adjustment of FullCapRep near the end of a charge cycle. The update slope adjustment range is from 2% per 15 minutes (0000b) to a maximum of 32% per 15 minutes (1111b).

nRelaxCfg Register (1B6h)

Register Type: Special

Nonvolatile Restore: RelaxCfg (0A0h) if *nNVCfg0.enRCfg* is set.

Alternate Initial Value: 0x2039

The nRelaxCfg register defines how the IC detects if the cell is in a relaxed state. See Figure 28. For a cell to be considered relaxed, current flow through the cell must be kept at a minimum while the change in the cell's voltage over time, dV/dt, shows little or no change. If AvgCurrent remains below the LOAD threshold while VCell changes less than the dV threshold over two consecutive periods of dt, the cell is considered relaxed. Table 76 shows the nRelaxCfg register format.

Table 76. RelaxCfg (0A0h)/nRelaxCfg (1B6h) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LOAD							dV					dt			

LOAD: Sets the threshold, which the AvgCurrent register is compared against. The AvgCurrent register must remain below this threshold value for the cell to be considered unloaded. Load is an unsigned 7-bit value where 1 LSb = 50µV. The default value is 800µV.

dV: Sets the threshold, which VCell is compared against. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed; dV has a range of 0 to 40mV where 1 LSb = 1.25mV. The default value is 3.75mV.

dt: Sets the time period over which change in VCell is compared against dV. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed. The default value is 1.5 minutes. The comparison period is calculated as:

$$\text{Relaxation period} = 2^{(dt-8)} \times 45s$$

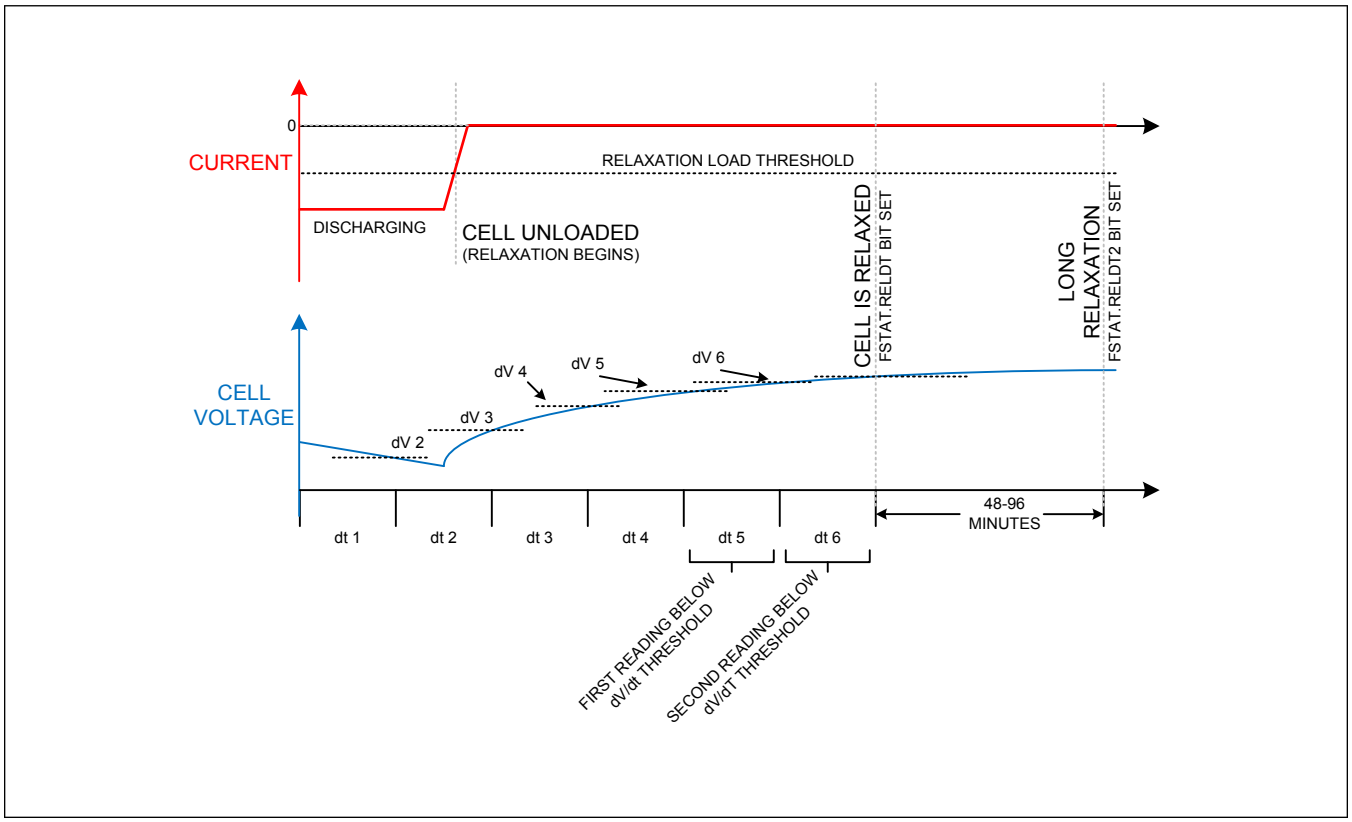


Figure 28. Cell Relaxation Detection

nLearnCfg Register (19Fh)

Register Type: Special

Nonvolatile Restore: LearnCfg (0A1h) if *nNVCfg0.enLCfg* is set

Alternate Initial Value: 0x4686

The nLearnCfg register controls all functions relating to adaptation during operation. Table 77 shows the register format:

Table 77. LearnCfg (0A1h)/nLearnCfg (19Fh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	1	LS			0	1	1	0

0: Bit must be written 0. Do not write 1.

1: Bit must be written 1. Do not write 0.

LS: Learn Stage. The Learn Stage value controls the influence of the voltage fuel gauge on the mixing algorithm. Learn Stage defaults to 0h, making the voltage fuel gauge dominate. Learn Stage then advances to 7h over the course of two full cell cycles to make the coulomb counter dominate. Host software can write the Learn Stage value to 7h to advance to the final stage at any time. Writing any value between 1h and 6h is ignored.

nTTFCfg Register (1C7h)/CVMixCap (0B6h) and CVHalfTime (0B7h) Registers

Register Type: Special

Nonvolatile Restore: CVHalfTime (0B7h) and CVMixCapRatio (0B6h) if nNVCfg1.enTTF is set.

Alternate Initial Value: CVHalfTime = 0xA00 (30 minutes) and CVMixCap = 75% x FullCapNom.

The nTTFCfg register configures parameters related to the time-to-full (TTF) calculation. If nNVCfg1.enTTF is set, CVHalfTime (0B7h) and CVMixCapRatio (0B6h) are refreshed from the nTTFCfg Register.

CVHalfTime (0B7h) is defined as the amount of time in the constant voltage portion of the charge cycle for the current to taper to half of the charging current in the constant current portion of the charge cycle. See Figure 29. CVHalfTime has an LSB of 0.0001953125 hours.

CVMixCapRatio (0B6h) is defined as the approximate state of charge where the charge transitions from the constant current portion of the charge cycle to the constant voltage portion of the charge current. See Figure 29. CVMixCapRatio has an LSB of 0.5mAh.

The Alternate Initial Value indicates that the charge cycle transitions from constant current to constant voltage when the SOC is 75% and that it then takes 30 minutes for the current to taper half of the charging current.

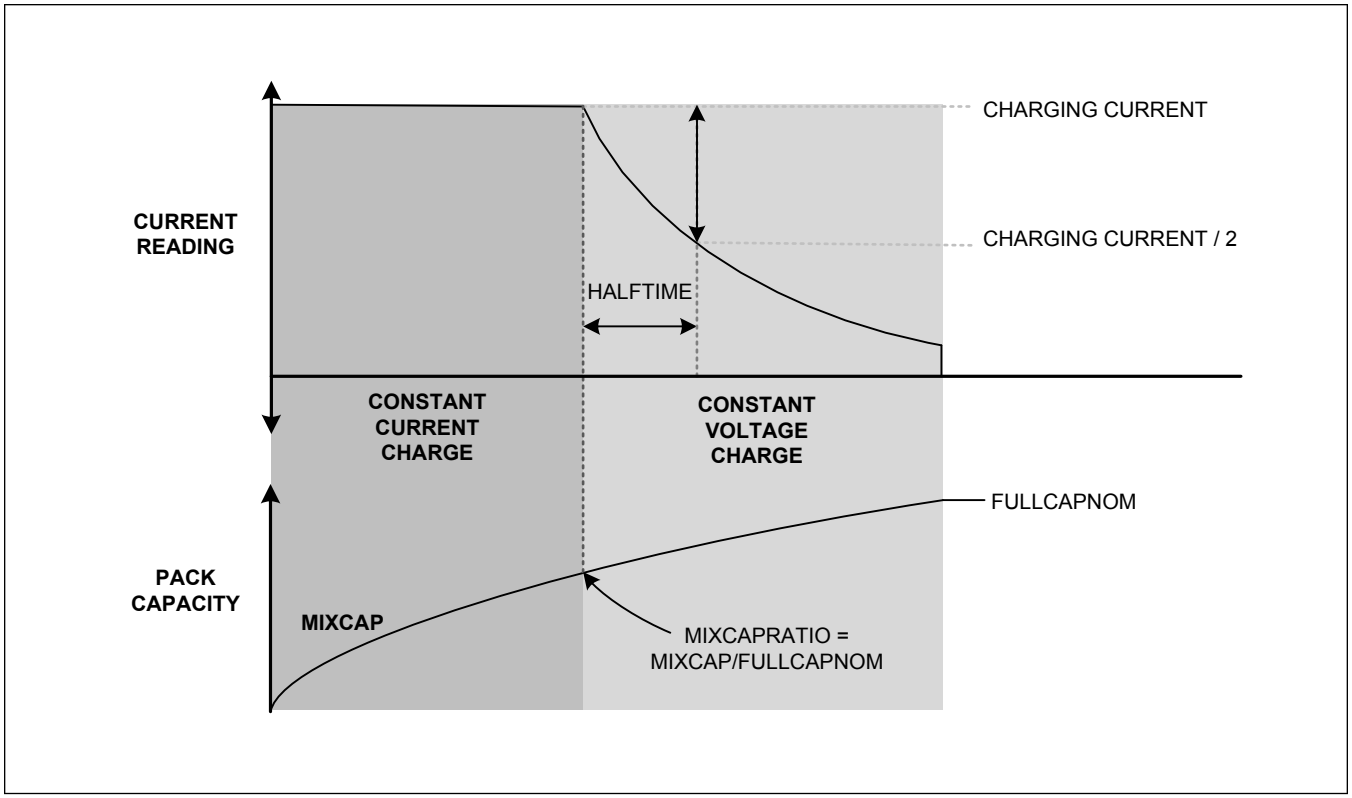


Figure 29. TTF Configuration Diagram

The nTTFCfg parameters can be tuned for best TTF performance during characterization by Maxim. Table 78 shows the register format.

Table 78. nTTFCfg Register (1C7h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
nCVHalfTime								nCVMixCapRatio							

nCVHalfTime: nCVHalfTime has an LSB of 45 seconds giving a full scale range of 0 seconds to 192 minutes.

nCVHalfTime = CVHalfTime(s)/45 seconds

nCVMixCapRatio: nCVMixCapRatio has an LSB of 1/256 giving a full scale range of 0 to 0.9961.

nCVMixCapRatio = CVMixCapRatio(%) × 256

For example, for a nCVHalftime of 37.5 minutes (2250 seconds) and a nCVMixRatio of 59%, the value for nTTFCfg = 3297h. These values are calculated as follows:

nCVHalfTime = 2250s/45 = 50dec = 32h

nCVMixCapRatio = 59% x 256 = 151dec = 97h

nConvgCfg Register (1B7h)

Register Type: Special

Factory Default Value: 2241h

Nonvolatile Restore: There is no associated restore location for this register.

The nConvgCfg register configures operation of the converge-to-empty feature. Table 79 shows the nConvgCfg register format. The *nNVCfg1.CTE* bit must be set to enable converge-to-empty functionality. If *nNVCfg1.CTE* is clear, this

register can be used as general-purpose data storage.

Table 79. nConvgCfg Register (1B7h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RepLow				VoltLowOff					MinSlopeX				RepL_per_stage		

RepL_per_stage: Adjusts the RepLow threshold setting depending on the present learn stage using the following equation. This allows the RepLow threshold to be at higher levels for earlier learn states. RepL_per_stage has an LSb of 1% giving a range of 0% to 7%.

RepLow Threshold = RepLow Field Setting + RemainingStages x RepL_per_stage

MinSlopeX: Sets the amount of slope shallowing which occurs when RepSOC falls below RepLow. MinSlopeX LSb corresponds to a ratio of 1/16 giving a full range of 0 to 15/16.

VoltLowOff: When the AvgVCell register value drops below the VoltLow threshold, RepCap begins to bend downwards by a ratio defined by the following equation. VoltLowOff has an LSb of 20mV giving a range of 0 to 620mV.

(AvgVCell - VEmpty)/VoltLowOff

RepLow: Sets the threshold below which RepCap begins to bend upwards. The RepLow field LSb is 2% giving a full scale range from 0% to 30%.

nRippleCfg Register (1B1h)

Register Type: Special

Factory Default Value: 0204h

Nonvolatile Restore: There is no associated restore location for this register.

The nRippleCfg register configures ripple measurement and ripple compensation. The recommended value for this register is 0x0204. Table 80 shows the register format.

Table 80. nRippleCfg Register (1B1h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
kDV													NR		

NR: Sets the filter magnitude for ripple observation as defined by the following equation giving a range of 1.4 seconds to 180 seconds.

$$\text{Ripple Time Range} = 1.4 \text{ seconds} \times 2^{NR}$$

kDV: Sets the corresponding amount of capacity to compensate proportional to the ripple.

SOCHold Register (0D0h)

Register Type: Special

The SOCHold register configures operation of the hold before empty feature and also the enable bit for 99% hold during charge. The default value for SOCHold is 1002h. Table 81 shows the SOCHold register format.

Table 81. SOCHold (0D0h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	99%HoldEn	EmptyVoltHold							EmptySocHold				

EmptyVoltHold: The positive voltage offset that is added to VEmpty. At VCell = VEmpty + EmptyVoltHold point, the empty detection/learning is occured. EmptyVoltHold has an LSb of 10mV giving a range of 0 to 1270mV.

EmptySocHold: It is the RepSOC at which RepSOC is held constant. After empty detection/learning occurs, RepSOC update continues as expected. EmptySocHold has an LSb of 0.5%, giving it a full range of 0 to 15.5%.

99%HoldEn: Enable bit for 99% hold feature during charging. When enabled, RepSOC holds a maximum value of 99% until Full Qualified is reached.

ModelGauge m5 Algorithm Additional Registers

The following registers contain intermediate ModelGauge m5 data which may be useful for debugging or performance analysis. The values in these registers are reset to their initial values 480ms after the IC is reset.

QResidual Register (00Ch)

Register Type: Capacity

Nonvolatile Backup: None

The QResidual register displays the calculated amount of charge in mAh that is presently inside of, but cannot be removed from the cell under present application conditions. This value is subtracted from the MixCap value to determine the capacity available to the user under present conditions (AvCap).

VFSOC Register (0FFh)

Register Type: Percentage

Nonvolatile Backup: None

The VFSOC register holds the calculated present state-of-charge of the battery according to the voltage fuel gauge.

VFOCV Register (0FBh)

Register Type: Voltage

Nonvolatile Backup: None

The VFOCV register contains the calculated open-circuit voltage of the cell as determined by the voltage fuel gauge. This value is used in other internal calculations.

QH Register (4Dh)

Register Type: Capacity

Nonvolatile Backup: None

Alternate Initial Value: 0x0000

The QH register displays the raw coulomb count generated by the device. This register is used internally as an input to the mixing algorithm. Monitoring changes in QH over time can be useful for debugging device operation.

AvCap Register (01Fh)

Register Type: Capacity

Nonvolatile Backup: None

The AvCap register holds the calculated available capacity of the cell pack based on all inputs from the ModelGauge m5 algorithm including empty compensation. The register value is an unfiltered calculation. Jumps in the reported value can be caused by changes in the application such as abrupt changes in load current or temperature. See the *Fuel-Gauge Empty Compensation* section for details.

AvSOC Register (00Eh)

Register Type: Percentage

Nonvolatile Backup: None

The AvSOC register holds the calculated available state of charge of the cell based on all inputs from the ModelGauge m5 algorithm including empty compensation. The AvSOC percentage corresponds with AvCap and FullCapNom. The AvSOC register value is an unfiltered calculation. Jumps in the reported value can be caused by changes in the application such as abrupt changes in load current or temperature. See the *Fuel-Gauge Empty Compensation* section for details.

MixSOC Register (00Dh)

Register Type: Percentage

Nonvolatile Backup: None

The MixSOC register holds the calculated present state-of-charge of the cell before any empty compensation adjustments are performed. MixSOC corresponds with MixCap and FullCapNom. See the *Fuel-Gauge Empty Compensation* section for details.

MixCap Register (02Bh)

Register Type: Capacity

Nonvolatile Backup: None

The MixCap register holds the calculated remaining capacity of the cell before any empty compensation adjustments are performed. See the *Fuel-Gauge Empty Compensation* section for details.

VFRemCap Register (04Ah)

Register Type: Capacity

Nonvolatile Backup: None

The VFRemCap register holds the remaining capacity of the cell as determined by the voltage fuel gauge before any empty compensation adjustments are performed. See the *Fuel-Gauge Empty Compensation* section for details.

FStat Register (03Dh)

Register Type: Special

Nonvolatile Backup: None

The FStat register is a read-only register that monitors the status of the ModelGauge algorithm. Do not write to this register location. Table 82 is the FStat register format.

Table 82. FStat Register (03Dh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	RelDt	EDet	X	RelDt2	X	X	X	X	X	DNR

DNR: Data Not Ready. This bit is set to 1 at cell insertion and remains set until the output registers have been updated. Afterwards, the IC clears this bit indicating the fuel gauge calculations are now up to date. This takes between 445ms and 1.845s depending on whether the IC was in a powered state prior to the cell-insertion event.

RelDt2: Long Relaxation. This bit is set to 1 whenever the ModelGauge m5 algorithm detects that the cell has been relaxed for a period of 48 to 96 minutes or longer. This bit is cleared to 0 whenever the cell is no longer in a relaxed state. See Figure 32.

EDet: Empty Detection. This bit is set to 1 when the IC detects that the cell empty point has been reached. This bit is reset to 0 when the cell voltage rises above the recovery threshold. See the *VEmpty* register for details.

RelDt: Relaxed cell detection. This bit is set to 1 whenever the ModelGauge m5 algorithm detects that the cell is in a fully relaxed state. This bit is cleared to 0 whenever a current greater than the load threshold is detected. See Figure 32.

X: Don't Care. This bit is undefined and can be logic 0 or 1.

FOTPStat Register (0BBh)

Register Type: Special

Non-Volatile Backup: None

The FOTPStat register shown in Table 83 is reserved for internal operation. It allocates 4 bits for use by the PatchID.

Table 83. FOTPStat Register (0BBh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PatchID				X	X	X	X	X	X	X	X	X	X	X	X

PatchID: PatchID. The upper 4 bits can be used to identify the PatchID version the IC uses.

Identification Registers

The following registers contain information to identify the IC type and the specific ROM ID.

DevName Register (021h)

Register Type: Special

Nonvolatile Backup: None

The DevName register holds device type and firmware revision information. This allows the host software to easily identify the type of IC being communicated to. Table 84 shows the DevName register format.

Table 84. DevName Register (021h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Revision												Device			

The DevName for the IC is 4209h, 420Ah, or 420Bh.

nROMID0 (1BCh)/nROMID1 (1BDh)/nROMID2 (1BEh)/nROMID3 (1BFh) Registers

Register Type: Special

Nonvolatile Restore: There are no associated restore locations for these registers

Each IC contains a unique 64-bit identification value that is contained in the nROMID registers. Note this is the same ID that can be read using the 1-Wire ROM ID commands. The unique ID can be reconstructed from the nROMID registers as shown in Table 85.

Table 85. nROMID Registers (1BCh to 1BFh) Format

nROMID3[15:0]	nROMID2[15:0]	nROMID1[15:0]	nROMID0[15:0]
ROM ID [63:48]	ROM ID [47:32]	ROM ID [31:16]	ROM ID [15:0]

AtRate Functionality

The AtRate function allows the host software to see the theoretical remaining time or capacity for any given load current. AtRate can be used for power management by limiting system loads depending on present conditions of the cell pack. Whenever the AtRate register is programmed to a negative value indicating a hypothetical discharge current, the AtQResidual, AtTTE, AtAvSOC, and AtAvCap registers display theoretical residual capacity, time-to-empty, state-of-charge, and available capacity respectively. Host software should wait two full task periods (703ms minimum in active mode) after writing the AtRate register before reading any of the result registers.

AtRate Register (004h)

Register Type: Current

Nonvolatile Backup: None

Host software should write the AtRate register with a negative two's-complement 16-bit value of a theoretical load current prior to reading any of the at-rate output registers.

AtQResidual Register (0DCh)

Register Type: Capacity

Nonvolatile Backup: None

The AtQResidual register displays the residual charge held by the cell at the theoretical load-current level entered into the AtRate register.

AtTTE Register (0DDh)

Register Type: Time

Nonvolatile Backup: None

The AtTTE register can be used to estimate time-to-empty for any theoretical current load entered into the AtRate register. The AtTTE register displays the estimated time-to-empty for the application by dividing AtAvCap by the AtRate register value. The AtTTE register has a maximum value of 102.3 hours. When AtTTE is larger than the maximum value, the AtTTE register saturates and contains the maximum value (FFFFh). The host can calculate time values longer that the maximum register value with the following equation:

$$AtTTE_{CALCULATED}\ (hours) = AtAvCap(mAh)/AtRate(mA)$$

AtAvSOC Register (0CEh)

Register Type: Percentage

Nonvolatile Backup: None

The AtAvSOC register holds the theoretical state of charge of the cell based on the theoretical current load of the AtRate register. The register value is stored as a percentage with a resolution of 0.0039% per LSB. If a 1% resolution state-of-charge value is desired, the host can read only the upper byte of the register instead.

AtAvCap Register (0DFh)

Register Type: Capacity

Nonvolatile Backup: None

The AtAvCap register holds the estimated remaining capacity of the cell based on the theoretical load current value of the AtRate register. The value is stored in terms of µVh and must be divided by the application sense-resistor value to determine the remaining capacity in mAh.

Alert Function

The Alert Threshold registers allow interrupts to be generated by detecting a high or low voltage, current, temperature, state-of-charge, or protection fault. Interrupts are generated on the ALRT pin open-drain output driver. An external pullup is required to generate a logic-high signal. Alerts can be triggered by any of the following conditions:

- Over/undervoltage—VAlrtTr register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/undertemperature—TAlrtTr register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/undercurrent—IAlrtTr register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/under SOC—SAlrtTr register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Protection Alert—ProtAlrt indicates which protection fault occured. Protection alerts enabled (Config.PAen = 1) and alerts enabled (Aen = 1).

To prevent false interrupts, the threshold registers should be initialized before setting the Aen bit. Alerts generated by a threshold-level violation can be configured to be cleared only by software, or cleared automatically when the threshold level is no longer violated. Prior to clearing the Status.PA, the ProtAlrt register must be written to 0000h. See the *Config* (01Dh) register description for details of the alert function configuration.

nVAlrtTh Register (18Ch)

Register Type: Special

Nonvolatile Restore: VAlrtTh (001h) if nNVCfg1.enAT is set.

Alternate Initial Value: FF00h (Disabled)

The nVAlrtTh register shown in Table 86 sets upper and lower limits that generate an ALRT pin interrupt if exceeded by any of the cell voltage readings. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 20mV resolution over the full operating range of the VCell register. At power-up, the thresholds default to their maximum settings unless they are configured to be restored from nonvolatile memory instead by setting the *nNVCfg1.enAT* bit.

Table 86. VAlrtTh (001h)/nVAlrtTh (18Ch) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VMAX								VMIN							

VMAX: Maximum voltage reading. An alert is generated if the maximum cell voltage reading exceeds this value. This field has 20mV LSb resolution.

VMIN: Minimum voltage reading. An alert is generated if the VCell register reading falls below this value. This field has 20mV LSb resolution.

nTAlrtTh Register (18Dh)

Register Type: Special

Nonvolatile Restore: TAlrtTh (002h) if nNVCfg1.enAT is set.

Alternate Initial Value: 7F80h (Disabled)

The nTAlrtTh register shown in Table 87 sets upper and lower limits that generate an ALRT pin interrupt if exceeded by any thermistor reading. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are stored in 2's-complement format with 1ºC resolution over the full operating range of the Temp register. At power-up, the thresholds default to their maximum settings unless they are configured to be restored from nonvolatile memory instead by setting the nNVCfg1.enAT bit.

Table 87. TAlrtTh (002h)/nTAlrtTh (18Dh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TMAX								TMIN							

TMAX: Maximum temperature reading. An alert is generated if any temperature channel reading exceeds this value. This field is signed 2's complement format with 1ºC LSb resolution.

TMIN: Minimum temperature reading. An alert is generated if the Temp register reading falls below this value. This field is signed 2's complement format with 1ºC LSb resolution.

nSAlrtTh Register (18Fh)

Register Type: Special

Nonvolatile Restore: SAlrtTh (003h) if nNVCfg1.enAT is set.

Alternate Initial Value: FF00h (Disabled)

The nSAlrtTh register shown in Table 88 sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the selected RepSOC, AvSOC, MixSOC, or VFSOC register values. See the *MiscCFG.SACFG* setting for details. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 1% resolution over the full operating range of the selected SOC register. At power-up, the thresholds default to their maximum settings unless they are configured to be restored from nonvolatile memory instead by setting the nNVCfg1.enAT bit.

Table 88. SAlrtTh (003h)/nSAlrtTh (18Fh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 88. SAlrtTh (003h)/nSAlrtTh (18Fh) Register Format (continued)

SMAX	SMIN

SMAX: Maximum state-of-charge reading. An alert is generated if the selected SOC register reading exceeds this value. This field has 1% LSb resolution.

SMIN: Minimum state-of-charge reading. An alert is generated if the selected SOC register reading falls below this value. This field has 1% LSb resolution.

nIAlrtTh Register (0ACh)

Register Type: Special

Nonvolatile Restore: IAlrtTh (0ACh) if nNVCfg1.enAT is set.

Alternate Initial Value: 7F80h (Disabled)

The nIAlrtTh register shown in Table 89 sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the Current register value. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 400µV resolution over the full operating range of the Current register. At power-up, the thresholds default to their maximum settings unless they are configured to be restored from nonvolatile memory instead by setting the nNVCfg1.enAT bit.

Table 89. IAlrtTh (0ACh)/nIAlrtTh (18Eh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CURRMAX								CURRMIN							

CURRMAX: Maximum Current Threshold. An alert is generated if the current register reading exceeds this value. This field is signed 2's complement with 400µV LSb resolution to match the upper byte of the Current register.

CURRMIN: Minimum Current Threshold. An alert is generated if the current register reading falls below this value. This field is signed 2's complement with 400µV LSb resolution to match the upper byte of the Current register.

Memory

The memory space of the IC consists of 32 pages of 16 registers which are 16-bits wide. Registers are addressed using an internal 9-bit range of 000h to 1FFh. Externally, registers are accessed with an 8-bit address for 2-wire communication or 16-bit address for 1-Wire communication. Registers are grouped by functional block. See the functional descriptions for details of each register's functionality. Certain memory blocks can be permanently locked to prevent accidental overwrite. See the *Locking Memory Blocks* section for details. Table 90 shows the full memory map of the IC. Note that some individual user registers are located on RESERVED memory pages. These locations can be accessed normally while the remainder of the page is considered RESERVED. Memory locations listed as RESERVED should never be written to. Data read from RESERVED locations is not defined.

Table 90. Top Level Memory Map

REGISTER PAGE	LOCK	DESCRIPTION	2-WIRE SLAVE ADDRESS	2-WIRE PROTOCOL	2-WIRE EXTERNAL ADDRESS RANGE	1-WIRE EXTERNAL ADDRESS RANGE
00h, 0Ah	—	MODELGAUGE m5 DATA BLOCK	6Ch	I²C	00h–4Fh	0000h–004Fh
01h–04h	LOCK2					
05h–09h	—	RESERVED	—	—	—	—
0Bh	LOCK2	MODELGAUGE m5 DATA BLOCK (continued)	6Ch	I²C	B0h–BFh	00B0h–00BFh
0Ch	SHA	SHA MEMORY	6Ch	I²C	C0h–CFh	00C0h–00CFh
0Dh	LOCK2	MODELGAUGE m5 DATA BLOCK (continued)	6Ch	I²C	D0h–DFh	00D0h–00DFh
0Eh–0Fh	—	RESERVED	—	—	—	—
10h–17h	—	SBS DATA BLOCK	16h	SBS	00h–7Fh	—
18h–19h	LOCK3	NONVOLATILE MEMORY	16h	I²C	80h–EFh	0180h–01EFh
1Ah–1Bh	LOCK1					
1Ch	LOCK4					
1Dh	LOCK5					
1Eh	LOCK1					
1Fh	—	NONVOLATILE HISTORY	16h	I²C	F0h–FFh	01F0h–01FFh

Table 91. Individual Registers

REGISTER ADDRESS	LOCK	DESCRIPTION	2-WIRE SLAVE ADDRESS	2-WIRE PROTOCOL	2-WIRE EXTERNAL ADDRESS RANGE	1-WIRE EXTERNAL ADDRESS RANGE
060h	—	Command Register	6Ch	I²C	60h	0060h
061h	—	CommStat Register	6Ch	I²C	61h	0061h
07Fh	—	Lock Register	6Ch	I²C	7Fh	007Fh

ModelGauge m5 Memory Space

Registers that relate to functionality of the ModelGauge m5 fuel gauge are located on pages 00h–04h and are continued on pages 0Bh and 0Dh. See the *ModelGauge m5 Algorithm* section for details of specific register operation. These locations (other than page 00h) can be permanently locked by setting LOCK2. Register locations shown in gray are reserved locations and should not be written to. See Table 92.

Table 92. ModelGauge m5 Register Memory Map

PAGE/ WORD	00_h	01_h	02_h	03_h	04_h	0A_h	0B_h	0D_h
0h	Status	FullCapRep	TTF	Reserved	AvgDieTemp	RelaxCfg	Status2	SOCHold
1h	VAlrtTh	TTE	DevName	Reserved	Reserved	LearnCfg	Power	AvgCell4
2h	TAlrtTh	QRTable00	QRTable10	QRTable20	QRTable30	Reserved	VRipple	AvgCell3
3h	SAlrtTh	FullSocThr	FullCapNom	Reserved	Reserved	Reserved	AvgPower	AvgCell2
4h	AtRate	RCell	Reserved	DieTemp	Reserved	MaxPeakPower	Reserved	AvgCell1
5h	RepCap	Reserved	Reserved	FullCap	Reserved	SusPeakPower	TTFCfg	CELL4
6h	RepSOC	AvgTA	Reserved	IAvgEmpty	Reserved	PackResistance	CVMixCap	CELL3
7h	Age	Cycles	Reserved	Reserved	Reserved	SysResistance	CVHalfTime	CELL2
8h	MaxMinVolt	DesignCap	Charging Current	Reserved	Reserved	MinSysVoltage	CGTempCo	CELL1
9h	MaxMinTemp	AvgVCell	FilterCfg	Reserved	Reserved	MPPCurrent	AgeForecast	ProtStatus
Ah	MaxMinCurr	VCell	Charging Voltage	VEmpty	VFRemCap	SPPCurrent	Reserved	Batt
Bh	Config	Temp	MixCap	Reserved	Reserved	Config2	Reserved	PCKP
Ch	QResidual	Current	Reserved	Reserved	Reserved	IAlrtTh	Reserved	AtQResidual
Dh	MixSOC	AvgCurrent	Reserved	FStat	QH	MinVolt	Reserved	AtTTE
Eh	AvSOC	IChgTerm	Reserved	Timer	QL	MinCurr	TimerH	AtAvSOC
Fh	MiscCfg	AvCap	Reserved	Reserved	Reserved	ProtAlrt	Reserved	AtAvCap

Nonvolatile Memory

Nonvolatile Memory Map

Certain ModelGauge m5 and device configuration values are stored in nonvolatile memory to prevent data loss if the IC loses power. The IC internally updates page 1Ah values over time based on actual performance of the ModelGauge m5 algorithm. The host system does not need to access this memory space during operation. Nonvolatile data from other accessible register locations is internally mirrored into the nonvolatile memory block automatically. Note that nonvolatile memory has a limited number of writes. **User accessible configuration memory is limited to 7 writes. Internal and external updates to page 1Ah as the fuel gauge algorithm learns is limited to 100 writes. Do not exceed these write limits.** See Table 99 for details on configuring the logging interval. Table 93 shows the nonvolatile memory register map.

Table 93. Nonvolatile Register Memory Map (slave address 16h)

PAGE/ WORD	18_h	19_h	1A_h[1]	1B_h	1C_h	1D_h	1E_h
0h	nXTable0	nOCVTable0	nQRTable00	nConfig	nPReserved0	nUVPrtTh	nDPLimit
1h	nXTable1	nOCVTable1	nQRTable10	nRippleCfg	nPReserved1	nTPrtTh1	nScOcvLim
2h	nXTable2	nOCVTable2	nQRTable20	nMiscCfg	nChgCfg	nTPrtTh3	nAgeFcCfg
3h	nXTable3	nOCVTable3	nQRTable30	nDesignCap	nChgCtrl	nIPrtTh1	nDesignVoltage
4h	nXTable4	nOCVTable4	nCycles	nSBSCfg	nRGain	nBALTh	Reserved
5h	nXTable5	nOCVTable5	nFullCapNom	nPackCfg	nPackResistance	nTPrtTh2	Reserved
6h	nXTable6	nOCVTable6	nRComp0	nRelaxCfg	nFullSOCThr	nProtMiscTh	nManfctrDate
7h	nXTable7	nOCVTable7	nTempCo	nConvgCfg	nTTFCfg	nProtCfg	nFirstUsed
8h	nXTable8	nOCVTable8	nBattStatus	nNVCfg0	nCGain	nJEITAC	nSerialNumber0
9h	nXTable9	nOCVTable9	nFullCapRep	nNVCfg1	nCGTempCo	nJEITAV	nSerialNumber1
Ah	nXTable10	nOCVTable10	nVoltTemp	nNVCfg2	nThermCfg	nOVPrtTh	nSerialNumber2
Bh	nXTable11	nOCVTable11	nMaxMinCurr	nHibCfg	Reserved	nStepChg	nDeviceName0
Ch	nVAlrtTh	nIChgTerm	nMaxMinVolt	nROMID0[2]	nManfctrName0	nDelayCfg	nDeviceName1
Dh	nTAlrtTh	nFilterCfg	nMaxMinTemp	nROMID1[2]	nManfctrName1	nODSCTh	nDeviceName2
Eh	nIAlrtTh	nVEmpty	nFaultLog/ nFullCapFlt	nROMID2[2]	nManfctrName2	nODSCCfg	nDeviceName3
Fh	nSAlrtTh	nLearnCfg	nTimerH	nROMID3[2]	nRSense	nProtCfg2	nDeviceName4

1. Locations 1A0h to 1AFh are updated automatically by the IC each time it learns.

2. The ROM ID is unique to each IC and cannot be changed by the user.

Shadow RAM

Nonvolatile memory is never written to or read from directly by the communication interface. Instead, data is written to or read from shadow RAM memory located at the same address. Copy and recall commands are used to transfer data between the nonvolatile memory and the shadow RAM. Figure 30 describes this relationship. Nonvolatile memory recall occurs automatically at IC power-up and software POR.

Shadow RAM and Nonvolatile Memory Relationship

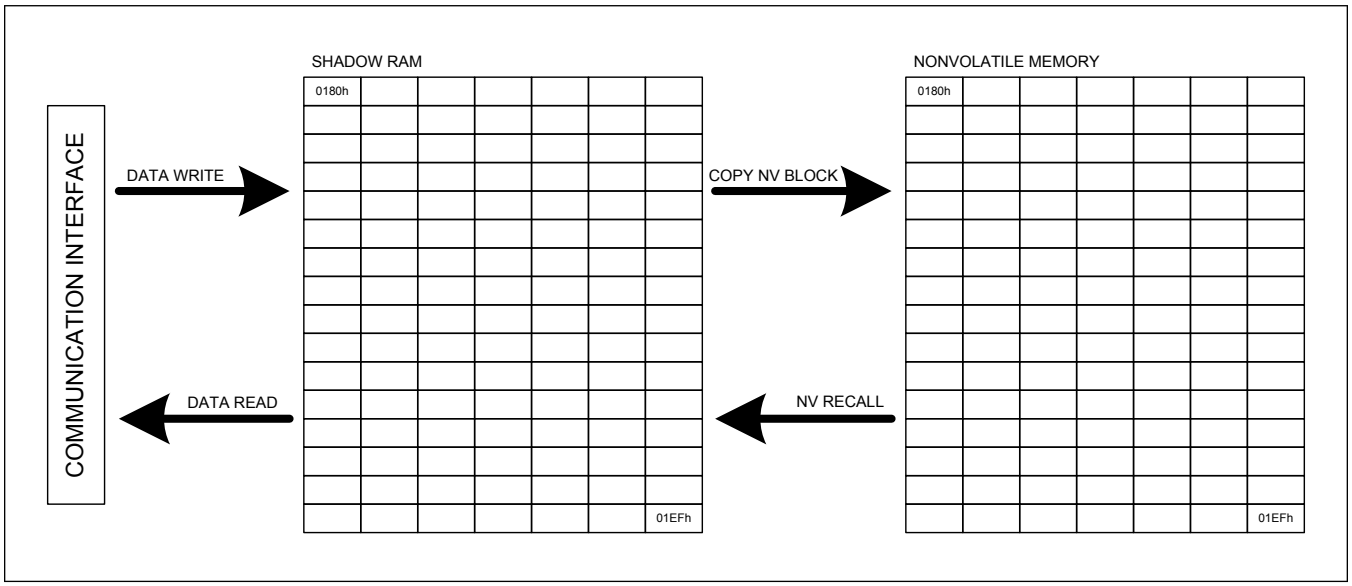


Figure 30. Shadow RAM and Nonvolatile Memory Relationship

Nonvolatile Memory Commands

The following commands are used to copy or recall data from the nonvolatile memory. All commands are written to the Command register at memory address 060h to perform the desired operation. The CommStat register can be used to track the status of the request.

COPY NV BLOCK [E904h]

This command copies the entire block from shadow RAM to nonvolatile memory addresses 180h to 1EFh excluding the unique ID locations of 1BCh to 1BFh. After issuing this command, the host must wait t_{BLOCK} for the operation to complete. The configuration memory can be copied a maximum of seven times. Note that the supply voltage must be above V_{NVM} for the operation to complete successfully.

NV RECALL [E001h]

This command recalls the entire block from nonvolatile memory to Shadow RAM addresses 180h to 1EFh. This is a low-power operation that takes up to t_{RECALL} to complete. Note that the supply voltage must be above V_{NVM} for the operation to complete successfully.

HISTORY RECALL [E2XXh]

This command copies history data into page 1Fh of the memory. After issuing this command, the host must wait t_{RECALL} for the operation to complete before reading page 1Fh. Table 94 shows the history information that can be recalled. See the *SHA-256*, Battery Life Logging, and *Determining Number of Remaining Updates* sections for details on how to decode this information.

Table 94. History Recall Command Functions

COMMAND	FUNCTION
0xE29D	Recall indicator flags to determine remaining SHA-256 secret updates or clears
0xE29B	Recall indicator flags to determine remaining configuration memory writes
0xE29C	Recall indicator flags to determine remaining Battery Life Logging updates
0xE29C, 0xE29D	Recall indicator flags to determine Battery Life Logging update errors
0xE22E to 0xE291	Recall Battery Life Logging information

Nonvolatile Block Programming

The host must program all nonvolatile memory locations at the same time by using the Copy NV Block command. After clearing the write protection bits, the host writes all desired nonvolatile memory Shadow RAM locations to their desired values, then sends the Copy NV Block command, and then waits t_{BLOCK} for the copy to complete. The CommStat.NVError bit should be read to determine if the copy command executed successfully. Afterwards, the host should send the power-on-reset sequence to reset the IC and have the new nonvolatile settings take effect. Note that the configuration memory is limited to n_{BLOCK} total write attempts. The recommended full sequence is as follows:

1. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
2. Write desired memory locations to new values.
3. Write 0x0000 to the CommStat register (0x61) one more time to clear CommStat.NVError bit.
4. Write 0xE904 to the Command register 0x060 to initiate a block copy.
5. Wait t_{BLOCK} for the copy to complete.
6. Check the CommStat.NVError bit. If set, repeat the process. If clear, continue.
7. Write 0x000F to the Command register 0x060 to send the full reset command to the IC.
8. Wait 10ms for the IC to reset. Write protection resets after the full reset command.
9. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
10. Write 0x8000 to the Config2 register 0x0AB to reset firmware.
11. Wait for the POR_CMD bit (bit 15) of the Config2 register to be cleared to indicate that the POR sequence is complete.
12. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

Determining Number of Remaining Updates

The configuration memory can only be updated seven times by the user (first update occurs during the manufacturing test). The number of remaining updates can be calculated using the following procedure:

1. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
2. Write 0xE29B to the Command register (060h).
3. Wait t_{RECALL}.
4. Read memory address 1FDh.
5. Decode address 1FDh data as shown in Table 95. Each block write has redundant indicator flags for reliability. Logically OR the upper and lower bytes together then count the number of 1s to determine how many updates have already been used. The first update occurs in the manufacturing test prior to shipping to the user.
6. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

Table 95. Number of Remaining Config Memory Updates

ADDRESS 1FDH DATA	LOGICAL OR OF UPPER AND LOWER BYTES	NUMBER OF UPDATES USED	NUMBER OF UPDATES REMAINING
0000000x00000001b or 000000010000000xb	00000001b	1	7
000000xx0000001xb or 0000001x000000xxb	00000011b	2	6
00000xxx000001xxb or 000001xx00000xxxb	00000111b	3	5
0000xxxx00001xxxb or 00001xxx0000xxxxb	00001111b	4	4
000xxxxx0001xxxxb or 0001xxxx000xxxxxb	00011111b	5	3
00xxxxxx001xxxxxb or 001xxxxx00xxxxxxb	00111111b	6	2
0xxxxxxx01xxxxxxb or 01xxxxxx0xxxxxxb	01111111b	7	1
xxxxxxxx1xxxxxxxb or 1xxxxxxxxxxxxxxxb	11111111b	8	0

Enabling and Freeing Nonvolatile vs. Defaults

There are seven nonvolatile memory words labeled nUser that are dedicated to general-purpose user data storage. Most other nonvolatile memory locations can also be used as general-purpose storage if their normal function is disabled. The nNVCfg0, nNVCfg1, and nNVCfg2 registers control which nonvolatile memory functions are enabled and disabled. Table 97 shows how to free up the specific registers for user data storage. Table 98 shows which nNVCfg bits control different IC functions and the effects when the bit is set or cleared. See the *nNVCfg* register descriptions for complete details. Do not convert a nonvolatile register to general-purpose memory space if that register's function is used by the application.

Table 96 is a summary of how many bytes can be made available for user memory and the functional trade-off to free up those bytes.

Table 96. Total Bytes Freeable for User Memory

BYTES FREEABLE	DESCRIPTION
164	Maximum freeable when protector is disabled and EZ Model is used.
132	When using protector and EZ Model.
84	When using protector and custom model.
66	When using protector, custom model, and half of the miscellaneous configuration options.
48	When using protector, custom model, and all of the miscellaneous configuration options.
40	When using protector, custom model, all of the miscellaneous configuration options, and alerts.
28	When using protector, custom model, all of the miscellaneous configuration options, alerts, and backup enabled.

Table 96. Total Bytes Freeable for User Memory (continued)

BYTES FREEABLE	DESCRIPTION
28	Always free when SBS mode is not enabled.

Table 97. Making Nonvolatile Memory Available for User Data

	RELATED FEATURE	FREE BY	BYTES	REGISTERS	ADDRESS	COMMENTS
MAJOR FEATURE CHOICES	SBS NVM	Disable SBS and DS features nNVCfg0.enSBS = 0 nNVCfg1.enDS = 0	13 words 26 bytes	nManfctrName[0:2] nManfctrDate nFirstUsed nSerialNumber[0:2] nDeviceName[0:4]	1CCh–CEh, 1E6h–1EFh	Generally freeable.
	Time-to-Full Configurability	nNVCfg1.enTTF = 0	1 word 2 bytes	nTTFCfg	1C7h	Free if default nTTFCfg is acceptable.
	Dynamic Power	nNVCfg0.enDP = 0	1 word 2 bytes	nDPLimit	1E0h	Free if feature is not used.
	Age Forecasting	nNVCfg0.enAF = 0	1 word 2 bytes	nAgeFcCfg	1E2h	Free if feature is not used. Has additional implications with nVoltTemp.
	$LiFePO_4$	nNVCfg1.enSC = 0	1 word 2 bytes	nScOcvLim	1E1h	Free if feature is not used.
	JEITA Charge Voltage/ Current vs. Temp	nNVCfg0.enJ = 0 nNVCfg0.enJP = 0	2 words 4 bytes	nJEITAC nStepChg	1D8h, 1DBh	Free if feature is not used. Note that nJEITAV and nOVPrtTh are still required for protector functionality.
MODELLING/ CHARACTER-IZATION CONFIGURATION OPTIONS	Design Cap + FullCapRep	nNVCfg0.enDC = 0	1 word 2 bytes	nDesignCap (else nFullCapRep)	1B3h	Freeable when original full-capacity is not required to be remembered as FullCapRep ages.
	Relaxation Configuration	nNVCfg0.enRCfg = 0	6 words 12 bytes	nRelaxCfg	1B6h	Normally freeable. Defaults work for most applications.
	Miscellaneous Configuration	nNVCfg0.enMC = 0		nMiscCfg	1B2h	
	Converge-to-Empty Non-Default Configuration	nNVCfg1.enCTE = 0		nConvgCfg	1B7h	
	Full Detection % Threshold	nNVCfg1.enFTh = 0		nFullSOCTh	1C6h	
	Filter Configuration	nNVCfg0.enFC = 0		nFilterCfg	19Dh	
	nLearnCfg	nNVCfg0.en = 0	1 word 2 bytes	nLearnCfg	19Fh	Freeable depending on modelling/characterization.
	Empty Voltage	nNVCfg0.enVE = 0	1 word 2 bytes	nVEmpty	19Eh	Free if targeting the fuel gauge to default 3.3V empty voltage.
	Charge Termination	nNVCfg0.enICT = 0	1 word 2 bytes	nIChgTerm	19Ch	With custom models/ characterization, this is not freeable.

Table 97. Making Nonvolatile Memory Available for User Data (continued)

	RELATED FEATURE	FREE BY	BYTES	REGISTERS	ADDRESS	COMMENTS
	SOC Table	Use m5 EZ model by setting nNVCfg.enOCV = 0 nNVCfg.enX = 0	12 words 24 bytes	nXTable[0:11]	180h–18Bh	
	OCV Table		12 words 24 bytes	nCVTable[0:11]	190h–19Bh	
OTHER	Alert Startup Configuration	nNVCfg1.enAT = 0	4 words 8 bytes	nVAlrtTh nTAlrtTh nIAlrtTh nSAlrtTh	18Ch–18Fh	
	Protector	nNVCfg1.enProt = 0 nNVCfg1.enJP = 0	15 words 30 bytes	nUVPrtTh, nTPrtTh1 nTPrtTh3, nIPrtTh1 nTPrtTh2 nProtMisTh nProtCfg, nJEITAV nOVPrtTh, nDelayCfg nODSCTh, nODSCCfg (below if JEITA also off) nJEITAC, nStepChg	1D0h–1DFh	Most applications of the MAX17320 use the protector. However, if the protector is entirely disabled, these 32 bytes become free NVM. The FET drivers and protection do not work in this configuration.

Table 98. Nonvolatile Memory Configuration Options

ADDRESS	REGISTER NAME	FACTORY DEFAULT	CONTROL BIT(S)	FUNCTION WHEN CONTROL BIT IS SET	FUNCTION WHEN CONTROL BIT(S) CLEARED
180h–18Bh	nXTable0 through nXTable11	All 0x0000	nNVCfg0.enX	180h–18Bh Hold Custom Cell Model Information	Becomes Free[1], IC Uses Default EZ Cell Model
18Ch	nVAlrtTh	0x0000	nNVCfg1.enAT	VAlrtTh, TAlrtTh, IAlrtTh, SAlrtTh initialize from nVAlrtTh, nTAlrtTh, nIAlrtTh, nSAlrtTh	Becomes Free[1], VAlrtTh, TAlrtTh, IAlrtTh, SAlrtTh → Disabled Threshold Values
18Dh	nTAlrtTh	0x0000			
18Eh	nIAlrtTh	0x0000			
18Fh	nSAlrtTh	0x0000			
190h–19Bh	nOCVTable0 through nOCVTable11	All 0x0000	nNVCfg0.enOCV	190h–19Bh Hold Custom Cell Model Information	Becomes Free[1], IC Uses Default EZ Cell Model
19Ch	nIChgTerm	0x0000	nNVCfg0.enICT	nIChgTerm→ IChgTerm	Becomes Free[1], IChgTerm = FullCapRep/3
19Dh	nFilterCfg	0x0000	nNVCfg0.enFCfg	nFilterCfg→ FilterCfg	Becomes Free[1], FilterCfg = 0x0EA4
19Eh	nVEmpty	0x0000	nNVCfg0.enVE	nVEmpty→ VEmpty	Becomes Free[1], VEmpty = 0xA561
19Fh	nLearnCfg	0x0000	nNVCfg0.enLCfg	nLearnCfg→ LearnCfg	Becomes Free[1], LearnCfg = 0x2687

Table 98. Nonvolatile Memory Configuration Options (continued)

ADDRESS	REGISTER NAME	FACTORY DEFAULT	CONTROL BIT(S)	FUNCTION WHEN CONTROL BIT IS SET	FUNCTION WHEN CONTROL BIT(S) CLEARED
1A0h	nQRTable00	0x1050	N/A	Always QRTable Information nQRTable00→ QRTable00 nQRTable10→ QRTable10 nQRTable20→ QRTable20 nQRTable30→ QRTable30	
1A1h	nQRTable10	0x8002			
1A2h	nQRTable20	0x078C			
1A3h	nQRTable30	0x0880			
1A4h	nCycles	0x0000		Always nCycles→ Cycles	
1A5h	nFullCapNom	0x0D48		Always nFullCapNom→ FullCapNom	
1A6h	nRComp0	0x08CC		Always nRComp0→ RComp0	
1A7h	nTempCo	0x223E		Always nTempCo→ TempCo	
1A8h	nBattStatus	0x0000	nNVCfg1.enProt nProtCfg.PFen	Logs/Saves Permanent Failure Status	Becomes Free[1]
1A9h	nFullCapRep	0x0D48	nNVCfg2.enFC	nFullCapRep→ FullCapRep	Becomes Free[1] nFullCapNom→ FullCapRep
1AAh	nVoltTemp	0x0000	nNVCfg2.enVT (nNVCfg0.enAF = 0)	AvgVCell→ nVoltTemp and AvgTA→ nVoltTemp at each backup event	Becomes Free[1], Voltage, Temperature Logging Disabled
			nNVCfg0.enAF (nNVCfg2.enVT = 0)	nVoltTemp stores Age Forecasting Information	Becomes Free[1], Age Forecasting Disabled
1ABh	nMaxMinCurr	0x0000	nNVCfg2.enMMC	MaxMinCurr→ nMaxMinCurr at each backup event	Becomes Free[1]
1ACh	nMaxMinVolt	0x0000	nNVCfg2.enMMV	MaxMinVolt→ nMaxMinVolt at each backup event	Becomes Free[1],
1ADh	nMaxMinTemp	0x0000	nNVCfg2.enMMT	MaxMinTemp→ nMaxMinTemp at each backup event	Becomes Free[1],
1AEh	nFaultLog/ nFullCapFlt	0x0000	nNVCfg0.enAF nNVCfg2.enFL	nFullCapFlt stores Age Forecasting backup or stores FaultLog information	Becomes Free[1], Age Forecasting and Fault Logging Disabled
1AFh	nTimerH	0x0000	nNVCfg2.enT	TimerH→ nTimerH at each backup event	Becomes Free[1],
1B0h	nConfig	0x2290	N/A	nConfig→ Config nConfig→ Config2	Never Free[1]
1B1h	nRippleCfg	0x0204	N/A	Always nRippleCfg→ RippleCfg	
1B2h	nMiscCfg	0x0000	nNVCfg0.enMC	nMiscCfg→ MiscCfg	Becomes Free[1], MiscCfg = 0x3870
1B3h	nDesignCap	0x0000	nNVCfg0.enDC	nDesignCap→ DesignCap	Become Free[1], FullCapRep→ DesignCap
1B4h	nSBSCfg	0x0008	nNVCfg0.enSBS	SBS Functions Enabled	Never Free[1]
1B5h	nPackCfg	0x0004	N/A	Always nPackCfg→ PackCfg	
1B6h	nRelaxCfg	0x083B	nNVCfg0.enRCfg	nRelaxCfg→ RelaxCfg	Becomes Free[1], RelaxCfg = 0x2039,
1B7h	nConvgCfg	0x2241	nNVCfg1.enCTE	Converge-to-Empty Enabled	Becomes Free[1], Converge-to-Empty Disabled

Table 98. Nonvolatile Memory Configuration Options (continued)

ADDRESS	REGISTER NAME	FACTORY DEFAULT	CONTROL BIT(S)	FUNCTION WHEN CONTROL BIT IS SET	FUNCTION WHEN CONTROL BIT(S) CLEARED
1B8h	nNVCfg0	0x0A00	N/A	Always Required Nonvolatile Memory Control Registers	
1B9h	nNVCfg1	0x0182			
1BAh	nNVCfg2	0xBE0A			
1BBh	nHibCfg	0x0909	nHibCfg Always Applies, Not Optional		
1BCh	nROMID0	Varies	N/A	Always the Unique 64-bit ID	
1BDh	nROMID1	Varies			
1BEh	nROMID2	Varies			
1BFh	nROMID3	Varies			
1C0h	nPReserved0	0x0000	N/A	**Do Not Modify** without Special Guidance from Maxim	
1C1h	nPReserved1	0x0000			
1C2h	nChgCfg	0x2061		Always Required for Charge Control	
1C3h	nChgCtrl	0x00E1			
1C4h	nRGain	0x0000	nNVCfg0.enDP	Used for Dynamic Power	Becomes Free[1], Dynamic Power Disabled
1C5h	nPackResistance	0x0000			
1C6h	nFullSOCThr	0x0000	nNVCfg1.enFTh	nFullSOCThr→ FullSOCThr	Becomes Free[1], FullSOCThr = 0x5005
1C7h	nTTFCfg	0x0000	nNVCfg1.enTTF	nTTFCfg Configures Time-to-Full Calculation	Becomes Free[1], Time-to-Full Default Configuration
1C8h	nCGain	0x4000	N/A	Trim for Calibrating Current-Sense Gain	
1C9h	nCGTempCo/ nTCurve	0x0000	nNVCfg1.enMtl (nNVCfg2.enMet = 1)	Metal Current Sense TempCo Configurable nTCurve→ CGTempCo	Becomes Free[1], Metal Current Sense TempCo Enabled, CGTempCo = 0x20C8
			nNVCfg2.enMet = 0 *(default)*	Thermistor Curvature Controlled by nTCurve	Becomes Free[1], Thermistor Curvature Disabled
1CAh	nThermCfg	0x71BE	N/A	Configuration for Translating Thermistor to ºC	
1CBh	Reserved	0x0000	N/A	Never Free[1]	
1CCh	nManfctrName0	0x0000	nNVCfg0.enSBS	nManfctrName[2:0]→ sManfctrName	Becomes Free[1]
1CDh	nManfctrName1	0x0000			
1CEh	nManfctrName2	0x0000			
1CFh	nRSense	0x01F4	N/A	Sense Resistor Value—Helps Host Translate Currents and Capacities	
1D0h	nUVPrtTh	0x508C	nNVCfg1.enProt	Configures Protection Thresholds	Becomes Free[1] Protector Disabled
1D1h	nTPrtTh1	0x3700			
1D2h	nTPrtTh3	0x5528			
1D3h	nIPrtTh1	0x4BB5			
1D4h	nBalTh	0x0000			
1D5h	nTPrtTh2	0x2D0A			
1D6h	nProtMiscTh	0x7A58			
1D7h	nProtCfg	0x0900			

Table 98. Nonvolatile Memory Configuration Options (continued)

ADDRESS	REGISTER NAME	FACTORY DEFAULT	CONTROL BIT(S)	FUNCTION WHEN CONTROL BIT IS SET	FUNCTION WHEN CONTROL BIT(S) CLEARED
1D8h	nJEITAC	0x644B			
1D9h	nJEITAV	0x0059			
1DAh	nOVPrtTh	0xB754			
1DBh	nStepChg	0xC884			
1DCh	nDelayCfg	0xAB3D			
1DDh	nODSCTh	0x0EAF			
1DEh	nODSCCfg	0x4355			
1DFh	nProtCfg2	0xA065	nNVCfg1. {enProtChkSm and enProt}	Holds CheckSum Value of 1B0h-1BBh, 1C0h-1C3h, 1D0h-1DEh for Validating NVM at Startup	Never Free[1]
1E0h	nDPLimit	0x0000	nNVCfg0.enDP	Configures Dynamic Power	Becomes Free[1] Dynamic Power Disabled
1E1h	nScOcvLim	0x0000	nNVCfg1.enSC	Used for $LiFePO_4$ Gauging	Becomes Free[1] $LiFePO_4$ Disabled
1E2h	nAgeFcCfg	0x0000	nNVCfg0.enAF	Configures Age Forecast	Becomes Free[1]
1E3h	nDesignVoltage	0xA5B9	nNVCfg0.enSBS	nDesignVoltage→ sDesignVolt	Becomes Free[1]
1E4h	Reserved	0x0000	N/A	Never Free[1]	
1E5h	Reserved	0x0000	N/A	Never Free[1]	
1E6h	nManfctrDate	0x0000	nNVCfg0.enSBS	nManfctrDate→ sManfctrDate	Becomes Free[1]
1E7h	nFirstUsed	0x0000		nFirstUsed→ sFirstUsed	Becomes Free[1]
1E8h	nSerialNumber0	0x0000		nSerialNumber[2:0]→ sSerialNumber	Becomes Free[1]
1E9h	nSerialNumber1	0x0000			
1EAh	nSerialNumber2	0x0000			
1EBh	nDeviceName0	0x0000		nDeviceName[4:0]→ sDeviceName	Becomes Free[1]
1ECh	nDeviceName1	0x0000			
1EDh	nDeviceName2	0x0000			
1EEh	nDeviceName3	0x0000			
1EFh	nDeviceName4	0x0000			

Note 1: "Free" indicates the address is unused and available as general user nonvolatile memory.

100 Record Life Logging

Addresses 1A0h–1AFh support 100 burn entries of learned battery characteristics and other life logging if LOCK1 is unlocked. The save interval is managed automatically using a Fibonacci-like algorithm which provides the following benefits:

1. **Lifespan autopsy/debug data** to support analysis of any aged or returned battery
    1. **Battery Characteristic Learning/Adaptation**. FullCap (nFullCapRep, nFullCapNom), empty-compensation (nQRTable00-30), resistance (nRComp0 and nTempCo)
    2. **Permanent Failure Information** (nBattStatus)
    3. **Battery Charge/Discharge Fractional Cycle Counter** (nCycles)
    4. **23.9 year Timer** (nTimerH)
    5. **Log-Interval Max/Min Voltage/Current/Temperature** (nMaxMinCurr, nMaxMinVolt, nMaxMinTemp)
    6. **Voltage/Temperature** at logging moment (nVoltTemp)
    7. **Faults** from any moment during the logging period.
2. **Intelligently managed save-intervals**
    1. **Frequent When New**. When the battery is new, the updates occur more frequently, since early information obtained, such as full-capacity, is more critical for overall performance.
    2. **Slower With Age.** As the battery matures the update interval slows down, since change observations progress slower.
    3. **Faster Updates Following Power-Loss**. This limits the loss of information associated with power-loss. This is limited to seven reset accelerations. The reset counter is also recorded (see the *nCycles* register). Most battery applications can proceed for longer than one year without interruption in power.
    4. **Limitation on Slowest Interval.** Beyond a certain cycle life, the update interval remains constant.

Configure this behavior according to the expected battery lifespan using the FibMax and FibScl parameters in *nNVCfg2* as shown in Table 99:

Table 99. Fibonacci Configuration Settings

		FIBONACCI SCALAR—NNVCFG2.FIBSCL			
Setting		**00**	**01**	**10**	**11**
1st and 2nd Interval		0.25	0.5	1	2
Battery Cycles Record Limit	FibMax = 0	193	386	**772**	1544
	FibMax = 1	**310.5**	**621**	**1242**	2484
	FibMax = 2	**496.5**	**993**	**1986**	3972
	FibMax = 3	**795.5**	**1591**	3182	6364
	FibMax = 4	**1273.25**	2546.5	5093	10186
	FibMax = 5	2038.75	4077.5	8155	16310
	FibMax = 6	3262	6524	13048	26096
	FibMax = 7	5220	10440	20880	41760

The **bold** settings in Table 99 and Table 100 are the generally recommended choices, depending on preference for update interval, slowest update rates, and lifespan.

Table 100 shows the slowest update intervals associated with each configuration.

Table 100. Longest Update Interval (in battery cycles)

		FIBONACCI SCALAR—NNVCFG2.FIBSCL			
Setting		00	01	10	11
1st and 2nd Interval		0.25	0.5	1	2
Slowest Update Interval	FibMax = 0	2	4	**8**	16
	FibMax = 1	**3.25**	**6.5**	**13**	26
	FibMax = 2	**5.25**	**10.5**	**21**	42
	FibMax = 3	**8.5**	**17**	34	68
	FibMax = 4	**13.75**	27.5	55	110
	FibMax = 5	22.25	44.5	89	178
	FibMax = 6	36	72	144	288
	FibMax = 7	58.25	116.5	233	466

Table 101 illustrates the saving schedule with the most preferred configurations.

Table 101. Saving Schedule Example With the Most Preferred Configurations

EX.	TOTAL CYCLE LIFE	FIBMAX	FIBSCL	SLOWEST UPDATE	1ST	2ND	3RD	4TH	5TH	6TH	7TH	8TH	9TH	10TH	11TH
1	**310.5**	1	0	3.25	0.25	0.25	0.5	0.75	1.25	2	3.25	3.25	3.25	.	.
2	**386**	0	1	4	0.5	0.5	1	1.5	2.5	4	4	4	.	.	.
3	**496.5**	2	0	5.25	0.25	0.25	0.5	0.75	1.25	2	3.25	5.25	5.25	5.25	.
4	**621**	1	1	6.5	0.5	0.5	1	1.5	2.5	4	6.5	6.5	6.5	.	.
5	**772**	0	2	8	1	1	2	3	5	8	8	8	.	.	.
6	**795.5**	3	0	8.5	0.25	0.25	0.5	0.75	1.25	2	3.25	5.25	8.5	8.5	.
7	**993**	2	1	10.5	0.5	0.5	1	1.5	2.5	4	6.5	10.5	10.5	10.5	.,
8	**1242**	1	2	13	1	1	2	3	5	8	13	13	13	.	.
9	**1273.25**	4	0	13.75	0.25	0.25	0.5	0.75	1.25	2	3.25	5.25	8.5	13.75	13.75

As an example for all subsequent startups for the configuration of Example 9 from Table 101, see the following:

1st startup [0.25, 0.25, 0.5, 0.75, 1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

2nd startup [0.25, 0.5, 0.75, 1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

3rd startup [0.5, 0.75, 1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

4th startup [0.75, 1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

5th startup [1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

6th startup [2, 3.25, 5.25, 8.5, 13.75, ...]

7th startup [3.25, 5.25, 8.5, 13.75, ...]

8th startup [5.25, 8.5, 13.75, ...]

Memory Locks and Write Protection

ModelGauge m5 RAM Registers and all nonvolatile memory locations can be write protected or permanently locked to prevent accidental overwriting or data loss in the application. Write protecting or locking a memory block only prevents future writes to the locations. Reading locked locations is still allowed. The IC has write protection enabled by default and must be disabled (as described in *CommStat Register*) before any registers can be written. **Note that locking a memory location is permanent so carefully choose all desired locks before sending the NV LOCK command.**

The SHA secret is stored in separate secure non-readable memory. There is a different command for locking the SHA secret and its state is not displayed in the Lock register. See the *SHA-256 Authentication* section for details. Once a lock bit is set, it can never be cleared. Table 90 shows which lock bits correspond to which memory blocks of the IC.

CommStat Register (061h)

Register Type: Special

Nonvolatile Backup: None

The CommStat register tracks the progress and error state of any command sent to the Command register. It also provides the write protection control and status of each page of registers. Table 102 shows the register format.

Table 102. CommStat Register (061h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	DISOff	CHGOff	WP5	WP4	WP3	WP2	WP1	NVError	NVBusy	WPGlobal

X: Don't Care. This bit is undefined and can be logic 0 or 1.

Write Protection: To prevent the host from accidentally writing any registers of the IC, write protection is enabled by default. Any time the host wants to write a register, the global write protection must be disabled as well as the write protection for the specific register page. To prevent accidental unlocking of the write protection, the CommStat register must be written with the desired value two times in a row without accessing any other registers to set or clear any of the write protection bits. All bits can be set or cleared in the same write sequence. For example, writing 0x0000 to CommStat twice in a row clears the WPGlobal and all WP1-WP5 at the same time.

WPGlobal: Write Protection Global Enable. Set to 1 to write protect all register pages. Clear to 0 to allow individual write protect bits (WP1–WP5) to be disabled.

WP1–WP5: Write Protection Enable Bits. Set any bit to 1 to write protect the pages specified below. Clear any bit to 0 to allow pages to be writable. To update any of these bits, the WPGlobal bit must be 0.

WP1: Write protects register pages 1Ah, 1Bh, 1Eh

WP2: Write protects register pages 01h, 02h, 03h, 04h, 0Bh, 0Dh

WP3: Write protects register pages 18h, 19h

WP4: Write protects register pages 1Ch

WP5: Write protects register pages 1Dh

DISOff: Set this bit to 1 to forcefully turn off DIS FET ignoring all other conditions if nProtCfg.CmOvrdEn is enabled. DIS FET remains off as long as this bit stays to 1. Clear to 0 for normal operation. Write Protection must be disabled before writing to the DISOff bit.

CHGOff: Set this bit to 1 to forcefully turn off CHG FET ignoring all other conditions if nProtCfg.CmOvrdEn is enabled. CHG FET remains off as long as this bit stays set to 1. Clear to 0 for normal operation. Write Protection must be disabled before writing to the CHGOff bit.

NVBusy: This read only bit tracks if nonvolatile memory is busy or idle. NVBusy defaults to 0 after reset indicating nonvolatile memory is idle. This bit sets after a nonvolatile related command is sent to the command register, and clears automatically after the operation completes.

NVError: This bit indicates the results of the previous SHA-256 or nonvolatile memory related command sent to the command register. This bit sets if there was an error executing the command or if the Full Reset command is executed. Once set, the bit must be cleared by system software in order to detect the next error. Write Protection must be disabled before the NVError bit can be cleared by the host.

NV LOCK [6AXXh]

This command permanently locks a block or blocks of memory. To set a lock, send 6AXXh to the Command register where the lower 5 bits of the command determine which locks are set. Table 103 shows a detailed format of the NV LOCK command. Set each individual LOCK bit to 1 to lock the corresponding register block. Set the LOCK bit to 0 to do nothing at this time. For example, writing 6A02h to the Command register sets LOCK2. Writing 6A1Fh sets all five locks. Writing 6A00h sets no locks.

Table 103. Format of LOCK Command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	1	0	0	0	0	LOCK 5	LOCK 4	LOCK 3	LOCK 2	LOCK 1

LOCK1: Locks register pages 1Ah, 1Bh, 1Eh (Locking disables History Life Logging)

LOCK2: Locks register pages 01h, 02h, 03h, 04h, 0Bh, 0Dh

LOCK3: Locks register pages 18h, 19h

LOCK4: Locks register pages 1Ch

LOCK5: Locks register pages 1Dh

Locking Memory Blocks

Prior to sending the lock command, the CommStat.NVError bit should be cleared, and after the command is sent, the CommStat.NVError bit should be read to determine if the lock command executed successfully. Note that locking memory blocks is a permanent operation. The recommended full sequence is:

1. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
2. Write 0x0000 to the CommStat register (0x61) one more time to clear CommStat.NVError bit.
3. Write 0x6AXX to the Command register 0x060 to lock desired blocks.
4. Wait t_{UPDATE} for the copy to complete.
5. Check the CommStat.NVError bit. If set, repeat the process.
6. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

Reading Lock State

The Lock register at address 07Fh reports the state of each lock. See Table 104 for the format of the Lock register. If a LOCK bit is set, the corresponding memory block is locked. If the LOCK bit is cleared, the corresponding memory block is unlocked. Note that the SHA-256 Secret lock state cannot be read through this register.

Table 104. Format of Lock Register (07Fh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	LOCK 5	LOCK 4	LOCK 3	LOCK 2	LOCK 1

X: Don't Care

1: LOCK is set

0: LOCK is clear

SHA-256 Authentication Procedures

The IC supports authentication which is performed using a FIPS 180-4 compliant SHA-256 one-way hash algorithm on a 512-bit message block. The message block consists of a 160-bit secret, a 160-bit challenge, and 192 bits of constant data. Optionally, the 64-bit ROM ID replaces 64 of the 192 bits of constant data used in the hash operation. Contact Maxim for details of the message block organization.

The host and the IC both calculate the result based on the mutually known secret. The result of the hash operation is known as the message authentication code (MAC) or message digest. The MAC is returned by the IC for comparison to the host's MAC. Note that the secret is never transmitted on the bus and thus cannot be captured by observing bus traffic. Each authentication attempt is initiated by the host system by writing a 160-bit random challenge into the SHA memory address space 0C0h to 0C9h. The host then issues the compute MAC or compute MAC with ROM ID command. The MAC is computed per FIPS 180-4 and stored in address space 0C0h to 0CFh overwriting the challenge value.

The IC introduces the new MAC key derivation function (MKDF), a 2-stage authentication scheme that utilizes an intermediate secret for an added layer of security.

Note that the results of the authentication attempt are determined by host verification. Operation of the IC is not affected by authentication success or failure.

Authentication Procedure

Figure 31 shows how a host system verifies the authenticity of a connected battery. The host first generates a random 160-bit challenge value and writes the challenge to IC memory space 0C0h to 0C9h. The host then sends the Compute MAC with ROM ID (3500h) or Compute MAC without ROM ID (3600h) to the Command register 060h and waits t_{SHA} for the computation to complete. Finally, the host reads the MAC from memory space 0C0h to 0CFh to verify the result. This procedure requires the secret to be maintained on the host side as well as in the battery. The host must perform the same calculations in parallel to verify the battery is authentic.

Procedure to Verify a Battery

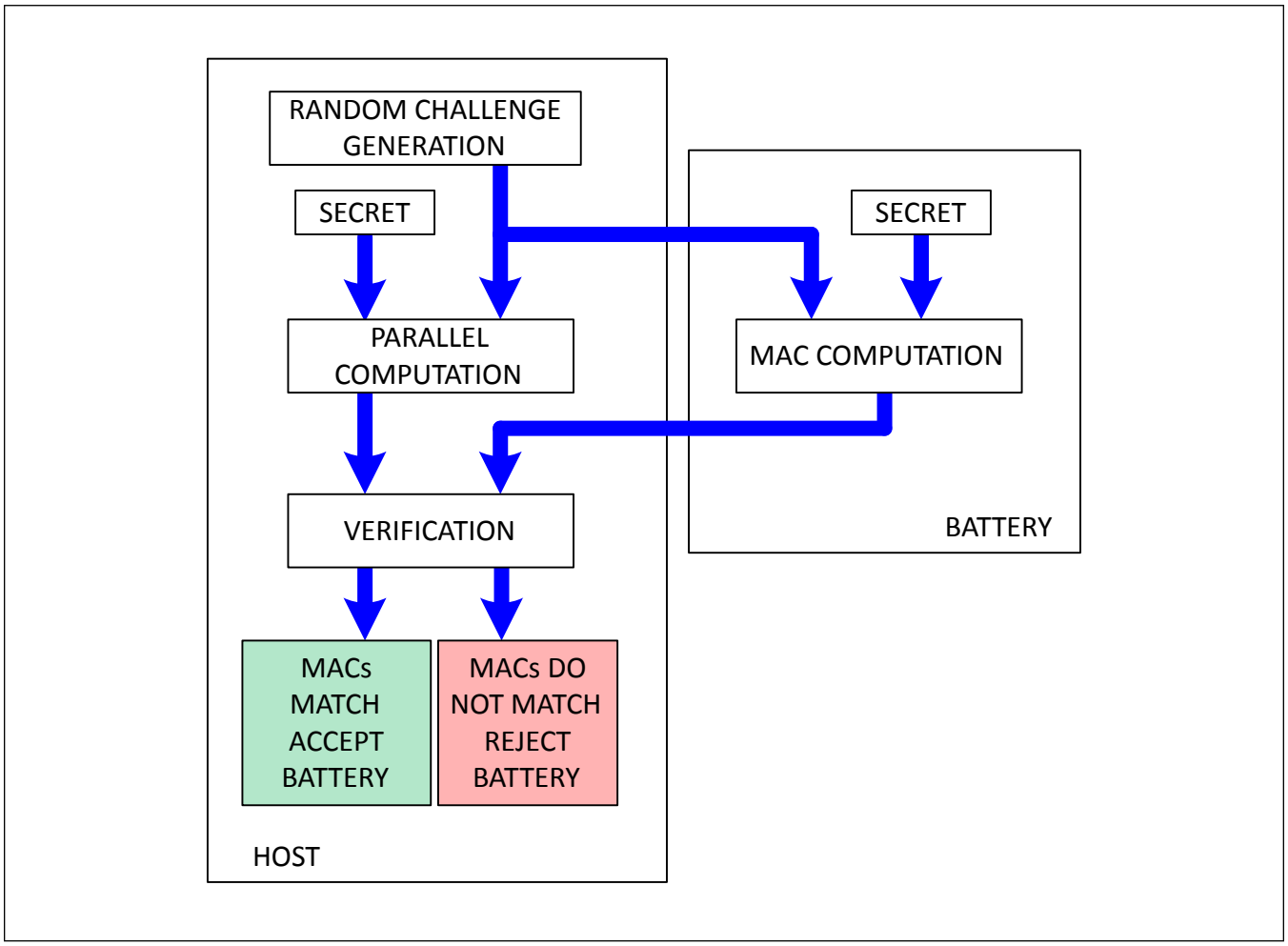


Figure 31. Procedure to Verify a Battery

Alternate Authentication Procedure

Figure 32 shows an alternative method of battery authentication which does not require the host to know the secret. In this method, each host device knows a challenge and MAC pair that matches the secret stored in an authentic battery, but each host device uses a different pair. This eliminates the need for special hardware on the host side to protect the secret from hardware intrusion. A battery could be cloned for a single host device, but creating a clone battery that works with any host would not be possible without knowing the secret.

The authentication process for this method is less complex. The host simply writes the challenge to IC memory space 0C0h to 0C9h. The host then sends the Compute MAC without ROM ID (3600h) to the Command register 060h. Note that Compute MAC with ROM ID Command is not valid for this authentication method. The host then waits t_{SHA} for computation to complete and reads the MAC from memory space 0C0h to 0CFh to verify the result.

Battery Authentication without a Host Side Secret

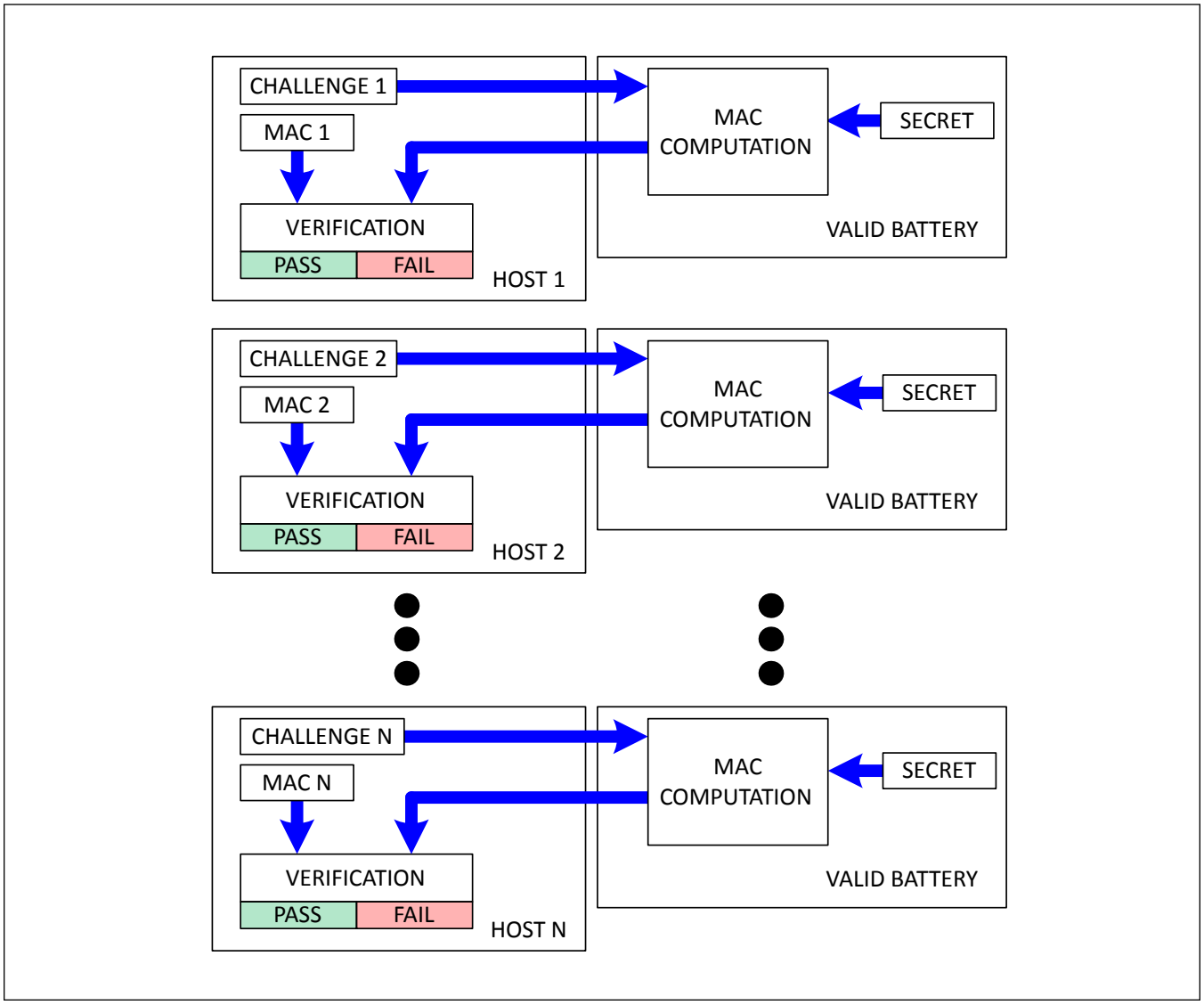


Figure 32. Battery Authentication without a Host Side Secret

Secret Management

The secret value must be programmed to a known value prior to performing authentication in the application. The secret cannot be written directly. Instead, the user must generate a new internal secret by performing a SHA computation with the old internal secret and a seed value sent as a challenge. To prevent any one entity from knowing the complete secret value, the process can be repeated multiple times by sending additional challenge seeds and performing additional computations.

Note that secret memory can only be changed a maximum of n_{SECRET} times including erase operations, and nonvolatile memory updates are not guaranteed. See the n_{SECRET} write limit in the *Electrical Characteristics* table. Any secret update operation that fails does not change the secret value stored in the IC, but consumes one of the available limited updates. Be careful not to use up all secret memory during the generation process. Maxim strongly recommends permanently locking the secret after it has been generated.

Single-Step Secret Generation

The single-step secret generation procedure should be used in production environments where the challenge seed value can be kept confidential, for example, when there are no OEM manufacturing steps or situations where an outside individual or organization would need to know the challenge seed. Use the following sequence to program the IC. Since the secret cannot be read from the IC, a parallel computation must be performed externally in order to calculate the stored secret. Figure 33 shows an example single step secret generation operation. Note that new units have their secret value already cleared to all 0s.

1. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
2. Clear the CommStat.NVError bit.
3. Write a challenge seed value to the SHA memory space 0C0h to 0C9h.
4. Write Compute Next Secret with ROM ID 3300h or Compute Next Secret without ROM ID 3000h to the Command register 060h.
5. Wait t_{SHA} + t_{UPDATE} for the computation to complete and the new secret to be stored.
6. If CommStat.NVError is set, return to step 1, otherwise, continue.
7. Verify the secret has been generated correctly with a test challenge at this time. If verification fails, return to step 1. See the *Determining Number of Remaining Updates* section to verify that enough nonvolatile memory writes remain in order to repeat the process.
8. Write Lock Secret 6000h to the Command register 060h. **Note this operation cannot be reversed.**
9. Wait t_{UPDATE} for secret to lock permanently.
10. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

Single-Step Secret Generation Example

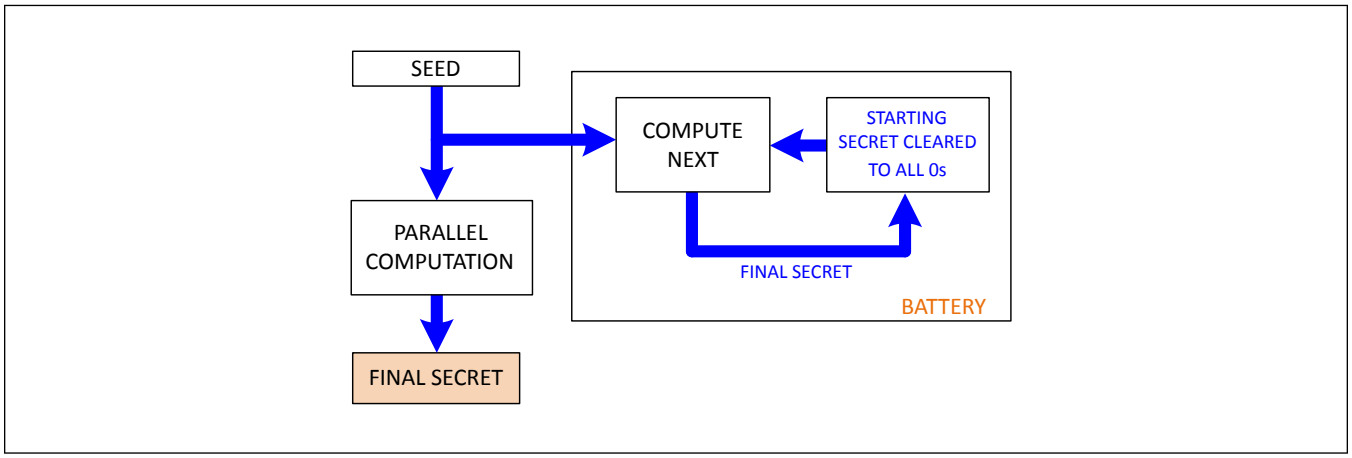


Figure 33. Single-Step Secret Generation Example

Multistep Secret Generation Procedure

The multistep secret generation procedure should be used in environments where an outside individual or organization would need to know the challenge seed such as OEM manufacturing. The multistep procedure is more complicated but allows a secret to be stored inside the IC without providing any information to an OEM manufacturer that could jeopardize secret integrity. Figure 34 shows an example where three OEM manufacturers are each provided with a seed value for a Compute Next operation. The final secret value stored inside the IC are known only to the top level manager who knows all seed values and has performed the computation separately. Use the following procedures when generating a multi-step secret. Note that the secret can only be updated or cleared n_{SECRET} times total. New units have their secret value already cleared to all 0s.

All OEMs:

1. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
2. Clear the CommStat.NVError bit.
3. Write the challenge seed value to the SHA memory space 0C0h to 0C9h.
4. Write Compute Next Secret with ROM ID 3300h or Compute Next Secret without ROM ID 3000h to the Command register 060h.
5. Wait t_{SHA} + t_{UPDATE} for computation to complete and new secret to be stored.
6. If CommStat.NVError is set, return to step 1, otherwise, continue.
7. Verify the secret has been generated correctly with a test challenge at this time. If verification fails, return to step 1. See the *Determining Number of Remaining Updates* section to verify that enough nonvolatile memory writes remain in order to repeat the process.
8. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

Last OEM:

1. Follow the procedure above for the final secret update, but skip step 8.
2. Write Lock Secret 6000h to the Command register 060h. **Note this operation cannot be reversed.**
3. Wait t_{UPDATE} for secret to lock permanently.
4. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

Top Level:

1. Generate all seed values to provide to OEMs.
2. Perform SHA calculations separately to determine what the final secret is after all manufacturing steps.
3. Keep final secret value secure.

Multistep Secret Generation Example

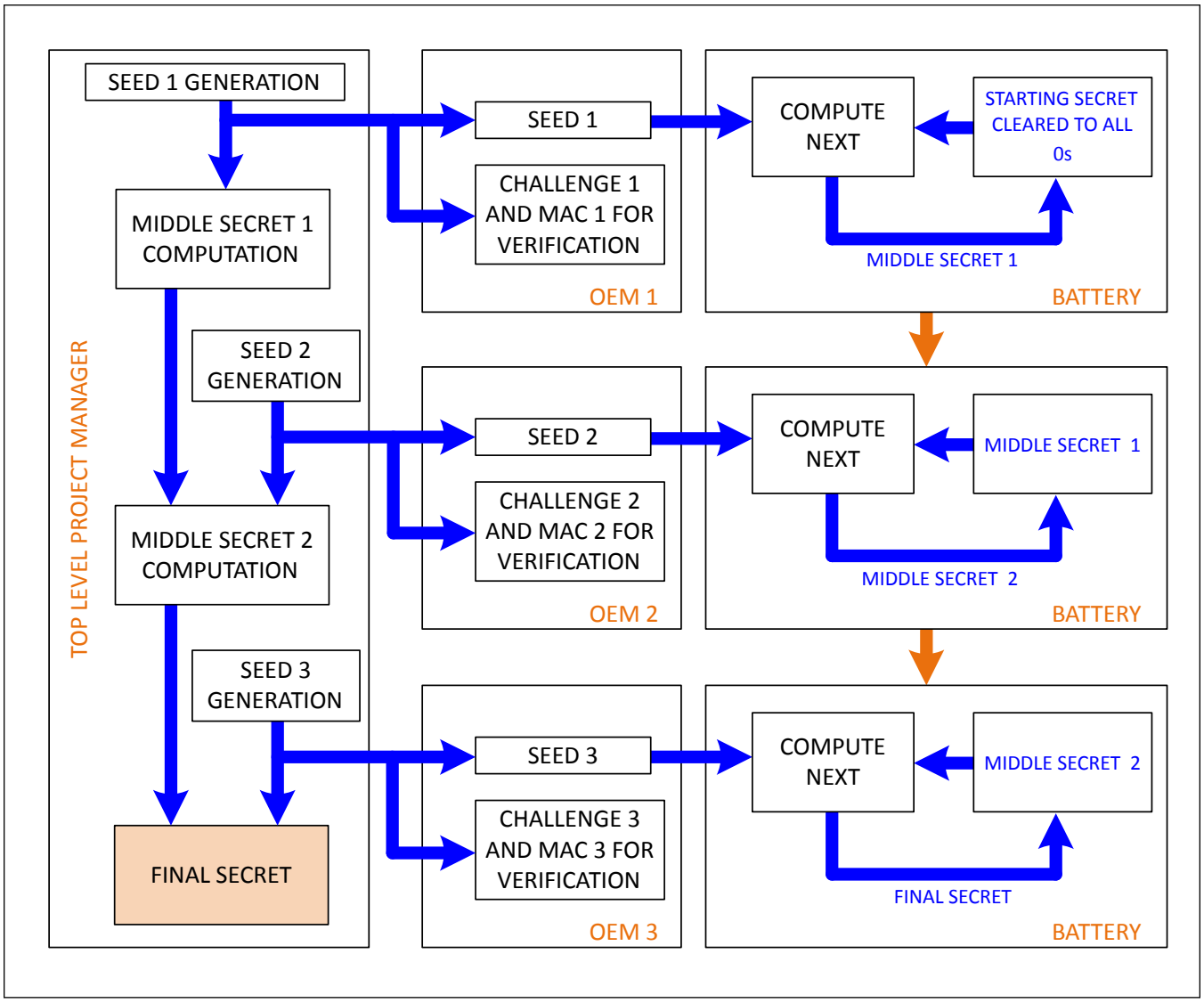


Figure 34. Multistep Secret Generation Example

2-Stage MKDF Authentication Scheme

The IC introduces the new 2-stage MKDF authentication scheme that utilizes an intermediate secret for an added layer of security. Figure 35 illustrates how to create a unique intermediate secret that can be stored in the host at the factory. Figure 36 outlines the procedure to complete the 2-stage authentication.

The following procedure implements the MKDF authentication scheme:

1. Write Copy Intermediate Secret from NVM command 3800h to the Command register 060h.
2. Write the unique challenge seed value to the SHA memory space 0C0h to 0C9h to be used to compute the next intermediate secret.
3. Write Compute Next Intermediate Secret with ROM ID 3900h or Compute Next Intermediate Secret without ROM ID 3A00h to the Command register 060h.
4. Wait t_{SHA} for computation to complete.
5. Write the challenge seed value to the SHA memory space 0C0h to 0C9h to be used to compute MAC using the intermediate secret.
6. Write Compute MAC From Intermediate Secret with ROM ID 3D00h or Compute MAC From Intermediate Secret without ROM ID 3C00h to the Command register 060h.
7. Wait t_{SHA} for computation to complete.
8. Read the MAC from SHA memory space 0C0h to 0CFh to verify the result.

Because the intermediate secret is stored in the same RAM location used for SHA calculation, executing some commands overwrites the intermediate secret. The functional impact is summarized as follows:

- Compute MAC and Compute Next Secret commands overwrites the intermediate secret.
- Copy intermediate secret from NVM overwrites the intermediate secret (as expected).
- Compute MAC from intermediate secret also overwrites the intermediate secret. If an intermediate secret is used for multiple MAC calculations, the intermediate secret needs to be reconstructed after each MAC computation.

Create a Unique Intermediate Secret

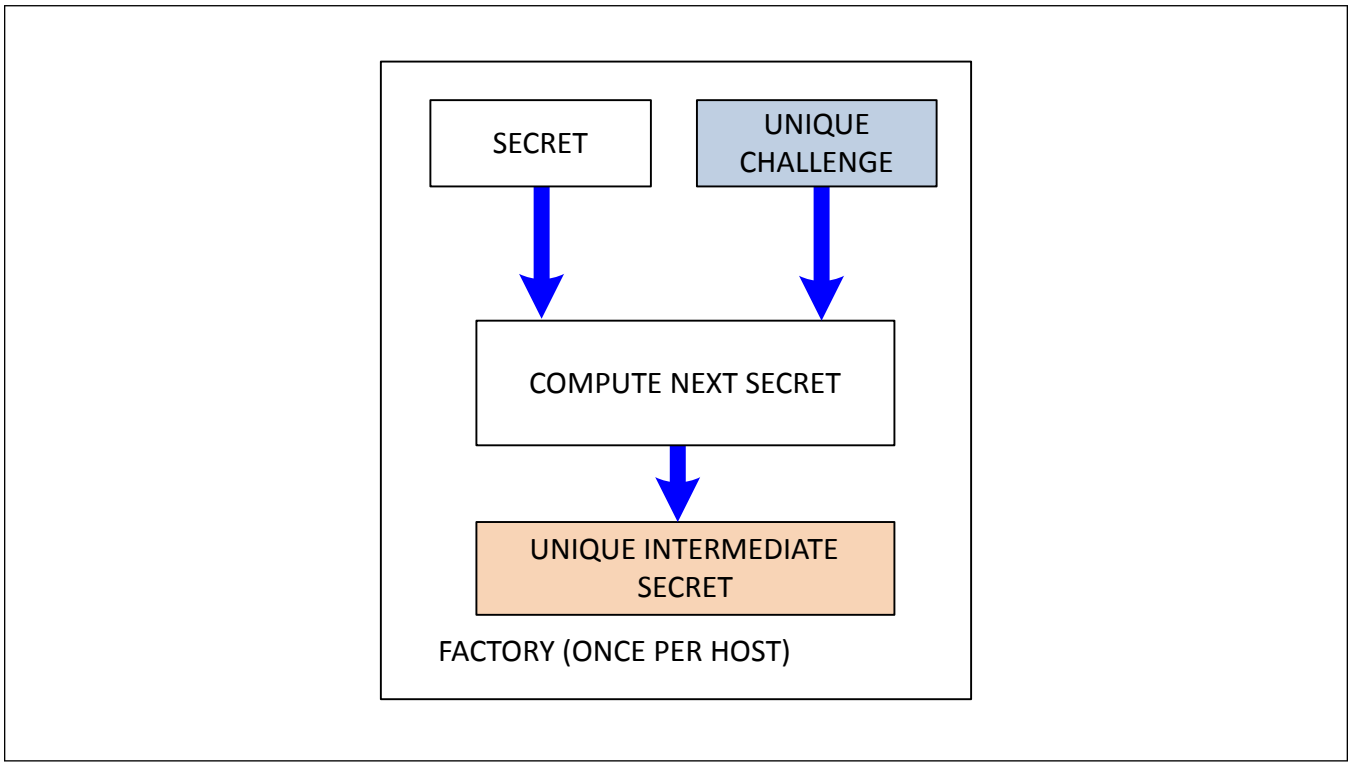


Figure 35. Create a Unique Intermediate Secret

Procedure for 2-Stage MKDF Authentication

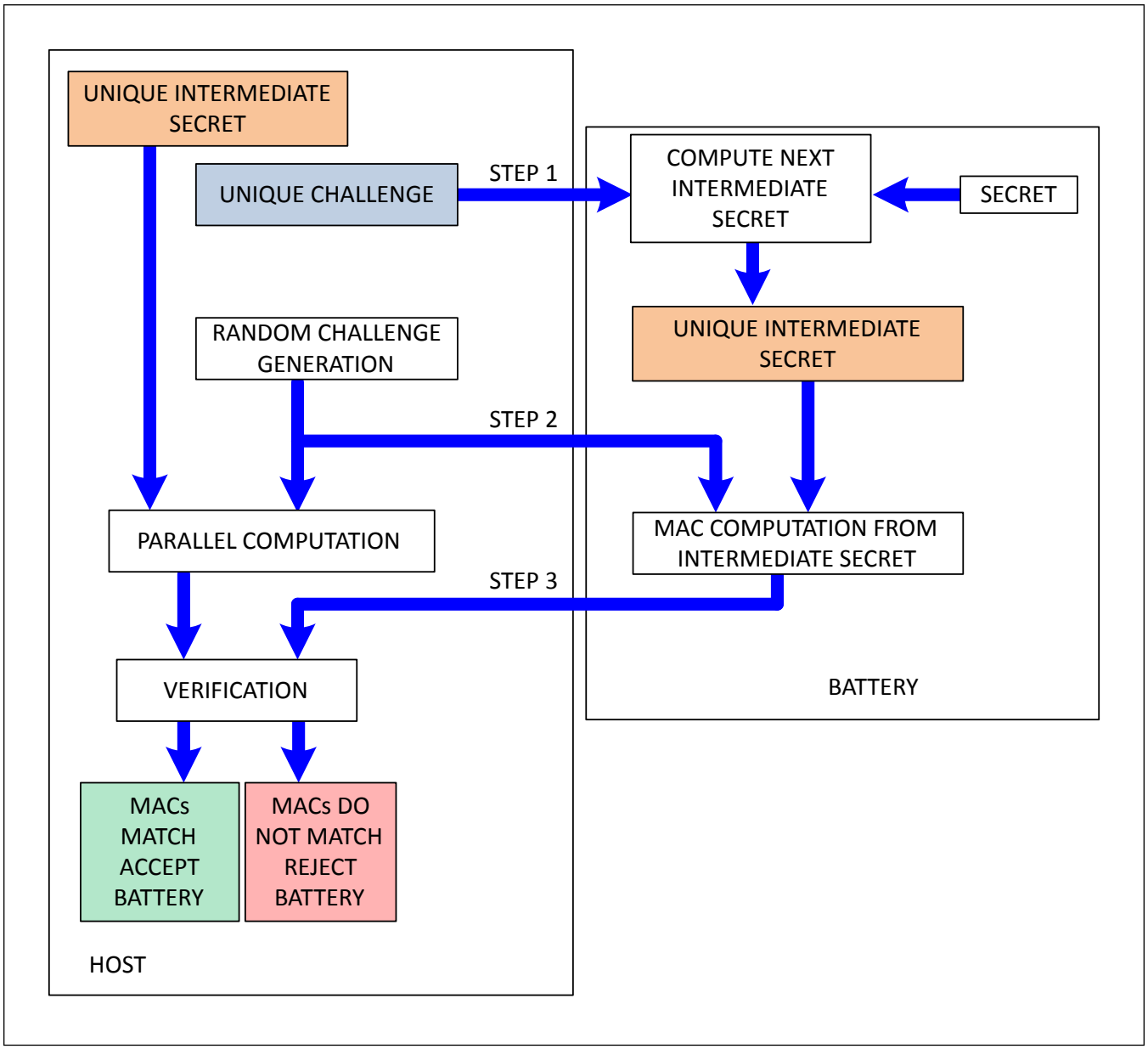


Figure 36. Procedure for 2-Stage MKDF Authentication

Determining Number of Remaining Updates

The internal secret can only be updated or cleared n_{SECRET} times total. The number of remaining updates can be calculated using the following procedure:

1. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
2. Write 0xE29D to the Command register (060h).
3. Wait t_{RECALL}.
4. Read memory address 1FDh.
5. Decode address 1FDh data as shown in Table 105. Each secret update has redundant indicator flags for reliability. Logically OR the upper and lower bytes together then count the number of 1s to determine how many updates have already been used. The first update occurs in the manufacturing test to clear the secret memory prior to shipping to the user.
6. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

Table 105. Number of Remaining Secret Updates

ADDRESS 0E6H DATA	LOGICAL OR OF UPPER AND LOWER BYTES	NUMBER OF UPDATES USED	NUMBER OF UPDATES REMAINING
0000000x00000001b or 000000010000000xb	00000001b	1	5
000000xx0000001xb or 0000001x000000xxb	00000011b	2	4
00000xxx000001xxb or 000001xx00000xxxb	00000111b	3	3
0000xxxx00001xxxb or 00001xxx0000xxxxb	00001111b	4	2
000xxxxx0001xxxxb or 0001xxxx000xxxxxb	00011111b	5	1
00xxxxxx001xxxxxb or 001xxxxx00xxxxxxb	00111111b	6	0

Authentication Commands

All SHA authentication commands are written to memory address 060h to perform the desired operation. Writing the Challenge or reading the MAC is handled by accessing the SHA memory space on page 0Ch through direct write and read operations. Note that write protection must be disabled before issuing any of the SHA-256 commands.

COMPUTE MAC WITHOUT ROM ID [3600h]

The challenge value must be written to the SHA memory space prior to performing a Compute MAC. This command initiates a SHA-256 computation without including the ROM ID in the message block. Instead, the ROM ID portion of the message block is replaced with a value of all 1s. Since the ROM ID is not used, this command allows the use of a master secret and MAC response independent of the ROM ID. The IC computes the MAC in t_{SHA} after receiving the last bit of this command. After the MAC computation is complete, the host can read the MAC from the SHA memory space.

COMPUTE MAC WITH ROM ID [3500h]

The challenge value must be written to the SHA memory space prior to performing a Compute MAC. This command is structured the same as the compute MAC without ROM ID, except that the ROM ID is included in the message block. With the unique ROM ID included in the MAC computation, the MAC is unique to each unit. After the MAC computation

is complete, the host can read the MAC from the SHA memory space.

COMPUTE NEXT SECRET WITHOUT ROM ID [3000h]

This command initiates a SHA-256 computation and uses the resulting MAC as the next or new secret. The hash operation is performed with the current 160-bit secret and the new 160-bit challenge. Logical 1s are loaded in place of the ROM ID. The last 160 bits of the MAC are used as the new secret value. The host must allow t_{SHA} after issuing this command for the SHA calculation to complete, then wait t_{UPDATE} for the new secret value to be stored in nonvolatile memory. During this operation, the SHA memory space is not updated. Note that the old secret value must be known prior to executing this command in order to calculate what the new secret value is.

COMPUTE NEXT SECRET WITH ROM ID [3300h]

This command initiates a SHA-256 computation and uses the resulting MAC as the next or new secret. The hash operation is performed with the current 160-bit secret, the 64-bit ROM ID, and the new 160-bit challenge. The last 160 bits of the output MAC are used as the new secret value. The host must allow t_{SHA} after issuing this command for the SHA calculation to complete, then wait t_{UPDATE} for the new secret value to be stored in nonvolatile memory. During this operation, the SHA memory space is not updated. Note that the old secret value must be known prior to executing this command in order to calculate what the new secret value is.

CLEAR SECRET [5A00h]

This command sets the 160-bit secret to all 0s. The host must wait t_{UPDATE} for the IC to write the new secret value to nonvolatile memory. This command uses up one of the secret write cycles.

LOCK SECRET [6000h]

This command write protects the secret to prevent accidental or malicious overwrite of the secret value. The secret value stored in nonvolatile memory becomes permanent. The host must wait t_{UPDATE} for the lock operation to complete.

The SHA-256 Lock state is not shown in the Lock register. Lock state can be verified by reading nonvolatile memory history using the following sequence:

1. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
2. Send 0xE29B to the Command register (060h).
3. Wait for t_{RECALL}.
4. Read memory address 1FCh.
5. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

If address 1FCh is 0x0000, then the secret is not locked. If address 1FCh is anything other than 0x0000, then the secret is permanently locked.

COPY INTERMEDIATE SECRET FROM NVM [3800]

This command copies the secret from NVM and places it in RAM to allow the secret to be used by the other commands.

COMPUTE NEXT INTERMEDIATE SECRET WITH ROMID [3900]

This command is similar to COMPUTE NEXT SECRET WITH ROMID except the secret used in the computation comes from the previously executed COPY INTERMEDIATE SECRET FROM NVM or COMPUTE NEXT INTERMEDIATE SECRET WITH/WITHOUT ROMID and the next secret is placed in RAM so it can be used in subsequent commands.

COMPUTE NEXT INTERMEDIATE SECRET WITHOUT ROMID [3A00]

This command is similar to COMPUTE NEXT SECRET WITHOUT ROMID except the secret used in the computation comes from the previously executed COPY INTERMEDIATE SECRET FROM NVM or COMPUTE NEXT INTERMEDIATE SECRET WITH/WITHOUT ROMID and the next secret is placed in RAM so it can be used in subsequent commands.

COMPUTE MAC FROM INTERMEDIATE SECRET WITHOUT ROMID [3C00]

This command is the same as COMPUTE MAC WITHOUT ROMID except the secret used in the computation comes from the previously executed COPY INTERMEDIATE SECRET FROM NVM or COMPUTE NEXT INTERMEDIATE SECRET WITH/WITHOUT ROMID.

COMPUTE MAC FROM INTERMEDIATE SECRET WITH ROMID [3D00]

This command is the same as COMPUTE MAC WITH ROMID except the secret used in the computation comes from the previously executed COPY INTERMEDIATE SECRET FROM NVM or COMPUTE NEXT INTERMEDIATE SECRET WITH/WITHOUT ROMID.

Smart Battery Compliant Operation

The IC is compliant to the Smart Battery Specification v1.1 when nNVCfg0.enSBS = 1. Enabling SBS operation does not interfere with normal operation of the IC. SBS formatted registers are accessed at slave address 16h, the memory addresses 100h to 17Fh using SBS protocols. SBS functionality can be configured using the nSBSCfg and nDesignVoltage registers.

SBS Compliant Memory Space

The IC contains an SBS v1.1 Compliant memory space on pages 10h to 17h that can be accessed using the Read Word, Write Word, and Read Block commands at 2-wire slave address 16h. Table 106 lists the SBS compliant registers. Refer to the SBS 1.1 Specification for details of registers at addresses 100h to 12Fh. Registers marked with Note 3 in the table are shared between SBS and normal IC functions and are always readable regardless of IC settings. Their format is described in the *Analog Measurements* section of the data sheet. All other registers on pages 13h to 17h are described in this section. Greyed locations are reserved and should not be written to.

Table 106. SBS Register Space Memory Map

PAGE/ WORD	10_h	11_h	12_h	13_h	14_h	15_h	16_h	17_h
0h	sManfct Access	sFullCap	sManfctr Name[1]	—	—	—	—	sMinVolt
1h	sRemCap Alarm	sRunTTE	sDevice Name[1]	—	—	sProtection Status	—	AvgPowerL
2h	sRemTime Alarm	sAvgTTE	sDev Chemistry[1]	—	—	PFStatus	—	—
3h	sBattery Mode	sAvgTTF	sManfct Data[2]	[s]AvgTemp4[3]	—	—	—	sMinCurr
4h	sAtRate	sCharging Current	—	[s]AvgTemp3[3]	—	—	—	—
5h	sAtTTF	sCharging Voltage	—	[s]AvgTemp2[3]	—	—	—	—
6h	sAtTTE	sBattery Status	—	[s]AvgTemp1[3]	—	—	—	—
7h	sAtRateOK	sCycles	—	[s]Temp4[3]	—	—	sAvCap	—
8h	sTemperature	sDesignCap	—	[s]Temp3[3]	—	—	sMixCap	—
9h	sPackVoltage	sDesignVolt	—	[s]Temp2[3]	—	MaxPeak Power[3]	—	—
Ah	sCurrent	sSpecInfo	—	[s]Temp1[3]	—	SusPeak Power[3]	—	—
Bh	sAvgCurrent	sManfctDate	—	—	—	Pack Resistance[3]	—	—
Ch	sMaxError	sSerial Number[2]	—	sCell4	sAvgCell4	Sys Resistance[3]	—	—
Dh	sRelSOC	—	—	sCell3	sAvgCell3	MinSys Voltage[3]	—	—
Eh	sAbsSOC	—	—	sCell2	sAvgCell2	MPP Current[3]	—	—

Table 106. SBS Register Space Memory Map (continued)

PAGE/ WORD	10_h	11_h	12_h	13_h	14_h	15_h	16_h	17_h
Fh	sRemCap	—	—	sCell1	sAvgCell1	SPP Current[3]	—	—

1. Location is read as ASCII data using the Read Block command.
2. Location is read as Hexadecimal data using the Read Block command.
3. Location is shared between SBS and normal IC functions and is always readable regardless of IC settings.

sManfctAccess Register (100h)

Register Type: Special

Nonvolatile Backup: None

The sManfctAccess register reports a value of 0x0000.

sRemCapAlarm/sRemTimeAlarm Registers (101h/102h)

Register Type: Capacity/Time

Nonvolatile Restore: None

sRemCapAlarm: sRemCapAlarm defaults to DesignCap/10 at startup.

sRemTimeAlarm: sRemTimeAlarm defaults to 10min at startup.

sBatteryMode Register (103h)

Register Type: Special

Nonvolatile Backup: None

Table 107 shows the sBatteryMode register format.

Table 107. sBatteryMode Register (103h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CapMd	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Only the CAPACITY_MODE bit is supported from the SBS spec for this register.

CapMd: CAPACITY_MODE from SBS. If CapMd = 1, the current and capacity registers report with an LSB of 10mW/ 10mWh instead of 1mA/1mAh. If CapMd = 0, the capacity registers report with an LSB of 1mAh.

At-Rate Functionality

sAtRate Register (104h)

Register Type: Current

Nonvolatile Backup: None

Host software should write the sAtRate register with a negative two's-complement 16-bit value of a theoretical load current prior to reading any of the at-rate output registers. AtRate calculations are performed using sAtRate (0x104) if enSBS = 1, or AtRate(0x004) if enSBS = 0.

sAtTTF Register (105h)

Register Type: Time

Nonvolatile Backup: None

The sAtTTF register can be used to estimate time to full for any theoretical current load entered into the sAtRate register. AtRate calculations are performed using either sAtRate (0x104) if enSBS = 1, or AtRate(0x004) if enSBS = 0.

sAtTTE Register (106h)

Register Type: Time

Nonvolatile Backup: None

The sAtTTE register can be used to estimate time-to-empty for any theoretical current load entered into the sAtRate register. The AtTTE register displays the estimated time-to-empty for the application by dividing AtAvCap by the sAtRate register value. sAtTTE is translated from AtTTE for conversion into minutes. AtRate calculations are performed using either sAtRate (0x104) if enSBS = 1, or AtRate(0x004) if enSBS = 0.

sAtRateOK Register (107h)

Register Type: Special

Nonvolatile Restore: None

From SBS specifications for AtRateOK:

Description:

Returns a Boolean value that indicates whether or not the battery can deliver the previously written AtRate value of additional energy for 10 seconds (Boolean). If the AtRate value is zero or positive, the AtRateOK function always returns true. Result can depend on the setting of the CAPACITY_MODE bit.

Purpose:
The AtRateOK function is part of a two-function call set used by power management systems to determine if the battery can safely supply enough energy for an additional load. It is used immediately after the SMBus host sets the AtRate value. See the *AtRate* register for additional usage information.

sTemperature Register (108h)

Register Type: Temperature

Nonvolatile Restore: None

Temperature is translated from the AvgTA register.

sPackVoltage Register (109h)

Register Type: Voltage

Nonvolatile Restore: None

sPackVoltage is translated from the PCKP Register.

Note: The sPackVoltage.MSbit (D15) can be set when sPackVoltage exceeds 0x3FFFh. Apply a mask of 0x7FFF to the sPackVoltage reading.

sChargingCurrent Register (114h)

Register Type: Current

Nonvolatile Restore: None

As for the SBS, this register returns the smart battery's desired charging rate in milliampere.

sBatteryStatus Register (116h)

Register Type: Special

Nonvolatile Backup: None

Table 108. BatteryStatus Register (116h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OChg	TChg	X	OTmp	TDis	X	RCA	RTA	Init	Dis	Full	Empty	0	0	0	0

X: Don't Care.

OChg: Over_Charged_Alarm. Set when: Fully charged (0x47), or OverChargeTemp (0x4B), or

OverChargeCurrent(0x4A), or ChargeSuspension (0x44). Cleared for other modes.

TChg: Terminate_Charge_Alarm: Set when: FullyCharged (0x47), or OverChargeTemp (0x4B), or OverChargeCurrent (0x4A), or ChargeSuspension (0x44), or BatteryFailure (0x4C), or Permanent Failure (0x89). Cleared for other modes.

OTmp: Over_Temp_Alarm. Set when: OverChargeTemp (0x4B) or OverDischargeTemp (0x8B). Cleared for other modes.

TDis: Terminate_Discharge_Alarm. Set when: Min_Cel < V_TBD or OverDischargeCurrent (0x1A or 0x8D), or RSOC < SALRT_Th1.Min, or OverDischargeTemp (0x8B). Cleared if Min_Cell > V_TBD, and RSOC > SOC_TBD, and not (0x1A or 0x8D).

RCA: RemCapAlarm. Set if sRemCap < RemCapAlarm. Cleared otherwise.

RTA: RemainingTimeAlarm. Set if AverageTimeToEmpty < RemTimeAlarm, cleared otherwise.

Init: Initialized. Always 1.

Dis: Discharging. Set if sCurrent ≤ 0mA and cleared if sCurrent > 0.

Full: Fully_Charged. Set if (RepSOC > 0x6380 (99.5%)). Cleared when RepSOC < nSBSCfg.FullReleasThr. nSBSCfg.FullReleasThr can be configured between 85% and 99%.

Empty: Fully_Discharged. Set if RepSOC < 1%. Cleared when RepSOC ≥ 19%.

sSpecInfo Register (11Ah)

Register Type: Special

Nonvolatile Backup: None

Table 109. SpecInfo Register (11Ah) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	1	1 (PEC)	0	0	0	1

PEC: PEC indicates whether the pack is configured to support SMBus PEC correction. PEC is always enabled on the MAX17320 in SBS Mode.

sManfctrDate Register (11Bh)

Register Type: Special

Nonvolatile Backup: None

Table 110. sManfctrDate Register (11Bh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Year							Month				Day				

sManfctrDate indicates the manufacturer's date, according to the value stored in MTP, nManfctrDate.

sSerialNumber Register (11Ch to 11Eh)

Register Type: Special

Nonvolatile Restore: None

SerialNumber indicates the 16-bit serial number as stored in nSerialNumber MTP. SerialNumber2 and SerialNumber3 provide extended data for the serial number as stored in nSerialNumber2 and nSerialNumber3. By using 6 bytes total, a serial number can provide a very unique ID for 281 trillion devices. A 4-byte serial number can support 4.3 billion devices. Some of the bits can be fixed to indicate platform or other information.

sManfctrName Register (120h)

Register Type: Special

Nonvolatile Restore: nManfctrName

A block SMBus/I^2C read of 0x20 on the I^2C slave 0x16 (SBS) reports RAM address 0x120 sequenced with 0x146 to

0x14A, for a total of 6 words of data. The first byte indicates the byte length and the following bytes are ASCII characters representing the brand name of the pack. This data is taken from nManfctrName in NVM, except that the byte count is set by firmware instead of saved in NVM.

sDeviceName Register (121h)

Register Type: Special

Nonvolatile Restore: nDeviceName

A block SMBus/I2C read of 0x21 on the I2C slave 0x16 (SBS) reports RAM address 0x121 sequenced with 0x140 to 0x143, for a total of 5 words of data. The first byte indicates the byte length and the following bytes are ASCII characters representing the device name. This data is taken from nDeviceName in NVM, except that the byte count is set by firmware instead of saved in NVM.

sDevChemistry Register (122h)

Register Type: Special

Nonvolatile Restore: None

A block SMBus/I2C read of 0x22 on the I2C slave 0x16 (SBS) reports RAM address 0x122 sequenced with 0x156 to 0x158, for a total of 4 words of data. The first byte indicates the byte length and the following bytes are ASCII characters representing the device chemistry. For the IC, this string is always “LION,” which is standard for all SBS packs.

sManfctData Registers (123h to 12Fh)

Register Type: Various

Nonvolatile Restore: None

The bytes of this read-block command are defined as follows:

BYTE 0 : NCELLS (DevName 4209h only)

BYTE 0 : NCELLS + 2 (DevName 420Ah or newer)

BYTE 1 : STATUS LSB

BYTE 2 : STATUS MSB

BYTE 3 : HCONFIG LSB

BYTE 4 : HCONFIG MSB

BYTE 5 : HCONFIG2 LSB

BYTE 6 : HCONFIG2 MSB

BYTE 7 : QL LSB

BYTE 8 : QL MSB

BYTE 9 : QH LSB

BYTE 10 : QH MSB

sProtectionStatus Register (151h)

Register Type: Special

Non-Volatile Backup: None

The sProtectionStatus is a copy of the *ProtStatus* Register.

PFStatus Register (152h)

Register Type: Special

Non-Volatile Backup: None

The sProtectionStatus is a copy of the *nBattStatus* Register.

sDesignVolt Register (119h)

Register Type: Voltage

Nonvolatile Restore: None

sDesignVolt is represented for the total pack voltage (DevName 420Ah or newer) and is calculated as nDesignVolt.DesignVolt x (nPackCfg.NCells + 2). sChargingVoltage and sMinSysVoltage are also scaled with nPackCfg.NCells. sDesignVolt is represented as per cell on DevName 4209h.

sFirstUsed Register (136h)

This register contains a mirror of the value stored in nonvolatile memory address 1D7h.

sCell1-4 Registers (13Fh-13Ch)

This register contains the same cell voltages information displayed in Cell1-4 (0D8h-0D5h) respectively with SBS compliant formatting. 1 LSb = 1mV giving a full scale range of 0.0V to 65.535V.

sAvgCell1-4 Registers (14Fh-14Ch)

This register contains the same average cell voltage information displayed in AvgCell1-4 (0D4h-0D1h) with SBS compliant formatting. 1 LSb = 1mV giving a full scale range of 0.0V to 65.535V.

sAvCap Register (167h)

This register contains the same information as the AvCap (01Fh) register. It is formatted for SBS compliance where 1 LSb = 1.0mAh giving a full scale range of 0.0mAh to 65535mAh.

sMixCap Register (168h)

This register contains the same information as the MixCap (00Fh) register. It is formatted for SBS compliance where 1 LSb = 1.0mAh giving a full scale range of 0.0mAh to 65535mAh.

sManfctInfo Register (170h)

The sManfctInfo register is accessed using the SBS protocol read block command. This register function is not supported in the IC.

nDesignVoltage Register (1E3h)

Register Type: Special

Factory Default Value: A5B9h

Nonvolatile Restore: There is no associated restore location for this register

Table 111. nDesignVoltage Register (1E3h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Vminsys								Vdesign							

Vminsys: (unsigned byte) = 'Minimum system voltage' specification for the design. Generates MinSysVoltage value.

Vdesign: (unsigned byte) = 'Design voltage' specification for the design.

Each byte has an LSb = 20mV (resolution) giving a full scale range = 0V to 5.12V.

These values are used in SBS calculations only when enSBS = 1.

nSBSCfg Register (1B4h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nSBSCfg register manages settings for SBS mode operation of the IC. Table 112 shows the register format.

Table 112. nSBSCfg Register (1B4h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CapMd	X	SBS_FullReleaseThr				X	X	X	X	SBS_RSenseSel		WPen	MECfg		X

X: Don't Care. This bit is undefined and can be logic 0 or 1.

SBS_FullReleaseThr: SBS Full Release Threshold. (DevName 420Ah or newer) sBatteryStatus.Full bit is cleared when SOC<SBS_FullReleaseThr. Configurable between 85% and 99% with a 1% LSB

SBS_FullReleaseThr Value = 85% + SBS_FullReleaseThr

SBS_RSenseSel: RSense Selction. (DevName 420Ah or newer) SBS module can support 1.25mOhm, 2.5mOhm, 5mOhm and 10mOhm (Previously only 2.5mOhm sense resistor was supported with DevName 4209h). All the SBS registers for capacity and current are scaled based on RSenseSel.

RsenseSel settings shown in Table 113.

Table 113. RSense Selection Settings

RSenseSel	RSENSE VALUE (mΩ)
0	1.25
1 (Default)	2.5
2	5
3	10

MECfg: Configures sMaxError register output when operating in SBS mode.

00: Always report 0% error

01: Always report 1% error

10: Report actual experienced error

11: Always report 3% error

CapMd: Selects the sBatteryMode.CapMd bit default setting when operating in SBS mode. CapMd resets to 0 every time a pack removal occurs as detected by floating communication lines.

WPen: Write Protection Enable. Set WPen to 0 for SBS mode.

Nonvolatile SBS Register Backup

When SBS mode operation is enabled by setting nNVCfg0.enSBS = 1, data from several nonvolatile memory locations is translated into SBS memory space. Table 114 lists these translations. Note that when performing an SBS Read Block command, the IC automatically generates the size data byte by counting the number of sequential non-zero data bytes stored in the corresponding nonvolatile memory locations. The nonvolatile memory only needs to store the actual data to be read by an SBS Read Block command. If SBS mode of operation is disabled, these locations become available for general-purpose nonvolatile data storage.

Table 114. SBS to Nonvolatile Memory Mapping

NONVOLATILE MEMORY ADDRESS	NONVOLATILE MEMORY REGISTER NAME	SBS MEMORY ADDRESS	S REGISTER NAME
1D6h	nManfctrDate	1Bh	sManfctrDate
1D7h	nFirstUsed	36h	sFirstUsed
1CCh–1CEh	nManfctrName[2:0]	20h (Read Block Command)	sManfctrName
1D8h–1DAh	nSerialNumber[2:0]	1Ch (Read Block Command)	sSerialNumber

Table 114. SBS to Nonvolatile Memory Mapping (continued)

NONVOLATILE MEMORY ADDRESS	NONVOLATILE MEMORY REGISTER NAME	SBS MEMORY ADDRESS	S REGISTER NAME
1DBh–1DFh	nDeviceName[4:0]	21h (Read Block Command)	sDeviceName

nCGain and Sense Resistor Relationship

To meet SBS compliance, current and capacity registers in the SBS memory space must have an LSb bit weight of 1.0mA and 1.0mAh. The current gain must be adjusted based on the application sense resistor value to set the proper bit weight. Table 115 shows the proper nCGain value to use for the most common sense resistor values. This is the default register value only. It does not include any offset trim or custom gain adjustment. Note that changing the nCGain register affects the gain reported by the standard ModelGauge m5 current and capacity registers.

Table 115. nCGain Register Settings to Meet SBS Compliance

SENSE RESISTOR VALUE (Ω)	NCGAIN REGISTER VALUE	CORRESPONDING CGAIN REGISTER VALUE
0.0025	4000h	0400h
0.005	2000h	0200h
0.010	1000h	0100h

Device Reset

There are two different levels of reset for the IC. A full reset restores the IC to its power-up state the same as if power had been cycled. A fuel-gauge reset resets only the fuel gauge operation without resetting IC hardware. This is useful for testing different configurations without writing nonvolatile memory. Use the following sequences to reset the IC.

FULL RESET

1. Write 0x0000 to CommStat register (0x61) two times in a row to unlock write protection.
2. Write 0x000F to the Command register 0x060 to send the full reset command to the IC.
3. Wait 10ms for the IC to reset. Write protection resets after the full reset command.
4. Write 0x0000 to CommStat register (0x61) two times in a row to unlock write protection.
5. Write 0x8000 to Config2 register 0x0AB to reset IC fuel gauge operation. This command does not disturb the state of the protection FETs.
6. Wait for POR_CMD bit (bit 15) of the Config2 register to be cleared to indicate that the POR sequence is complete.
7. Write 0x00F9 to CommStat register (0x61) two times in a row to lock write protection.

FUEL-GAUGE RESET

1. Write 0x0000 to CommStat register (0x61) two times in a row to unlock write protection.
2. Write 0x8000 to Config2 register 0x0AB to reset IC fuel gauge operation. This command does not disturb the state of the protection FETs.
3. Wait for POR_CMD bit (bit 15) of the Config2 register to be cleared to indicate that the POR sequence is complete.
4. Write 0x00F9 to CommStat register (0x61) two times in a row to lock write protection.

Reset Commands

There are two commands that can be used to reset either the entire IC or just the operation of the fuel gauge. Note that the reset fuel gauge command is written to Config2 instead of the Command register.

HARDWARE RESET [000Fh to address 060h]

Send the hardware reset command to the Command register to recall all nonvolatile memory into shadow RAM and reset all hardware-based operations of the IC. This command should always be followed by the reset fuel gauge command to fully reset operation of the IC.

FUEL GAUGE RESET [8000h to address 0ABh]

The fuel gauge reset command resets operation of the IC without restoring nonvolatile memory values into shadow RAM. This command allows different configurations to be tested without using one of the limited number of nonvolatile memory writes. This command does not disturb the state of the protection FETs.

Communication

This section covers communication protocols and summarizes all special commands used by the IC. The IC communicates over a 2-wire interface using either I^2C or SBS protocols depending on the memory address selected by the host. The IC communicates using the Maxim 1-Wire interface.

2-Wire Bus System

The 2-wire version of the IC uses a 2-wire bus system to communicate by both standard I^2C protocol or by SBS smart battery protocol. The slave address used by the host to access the IC determines which protocol is used and which memory locations are available to read or write. The following sections apply to both protocols. See the *I^2C* and *SBS Bus System* descriptions for specific protocol details.

Hardware Configuration

The 2-wire bus system supports operation as a slave-only device in a single or multi-slave and single or multi-master system. Up to 128 slave devices can share the bus using 7-bit slave addresses. The 2-wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the IC and a master device at speeds up to 400kHz. The ICs SDA pin operates bidirectionally. When the IC receives data, SDA operates as an input. When the IC returns data, SDA operates as an open-drain output with the host system providing a resistive pullup. See Figure 37. The IC always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal as well as the START and STOP bits, which begin and end each transaction.

2-Wire Bus Interface Circuitry

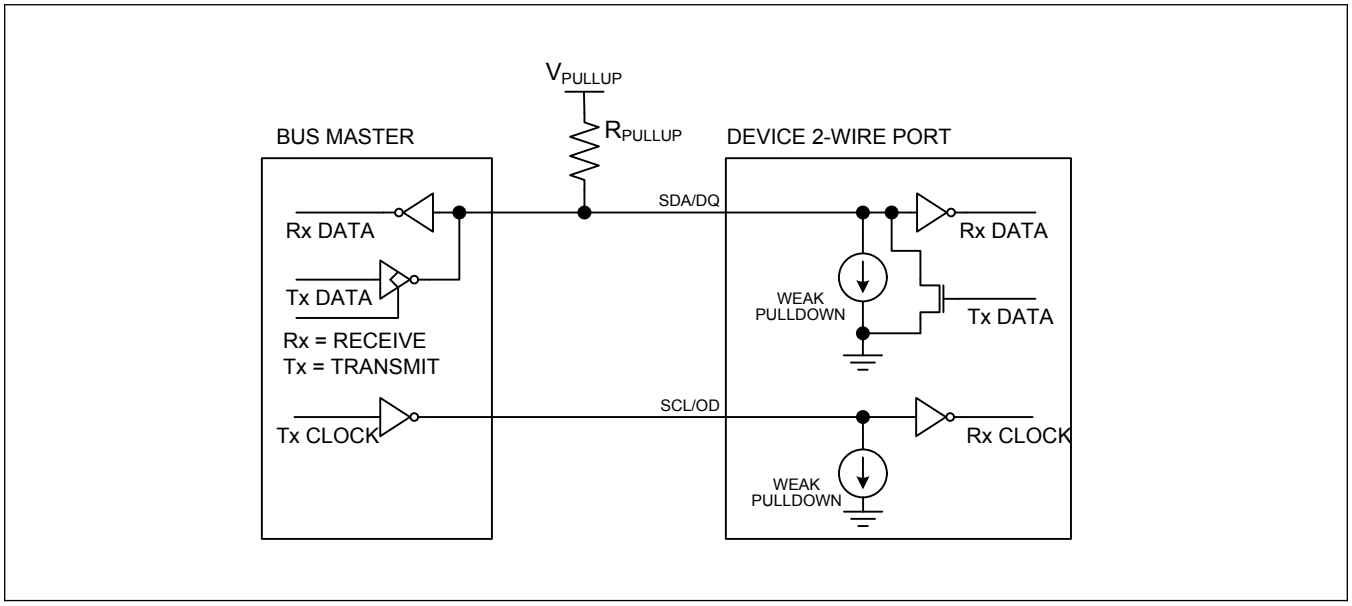


Figure 37. 2-Wire Bus Interface Circuitry

I/O Signaling

The following individual signals are used to build byte level 2-Wire communication sequences.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low to high and then high to low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition by a low-to-high transition on SDA while SCL is high. A Repeated START condition can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multi-master systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits

Each byte of a data transfer is acknowledged with an acknowledge bit (ACK) or a negative acknowledge bit (NACK). Both the master and the IC slave generate acknowledge bits. To generate an ACK bit, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a NACK bit, the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication. If a transaction is aborted mid-byte, the master should send additional clock pulses to force the slave IC to free the bus prior to restarting

communication.

Data Order

With 2-wire communication, a byte of data consists of 8 bits ordered most significant bit (MSb) first. The least significant bit (LSb) of each byte is followed by an ACK bit. IC registers composed of multibyte values are ordered least significant byte (LSB) first.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a Slave Address and the read/write (R/W) bit. When the bus is idle, the IC continuously monitors for a START condition followed by its slave address. When the IC receives a slave address that matches its Slave Address, it responds with an ACK bit during the clock period following the R/W bit. The IC supports the slave addresses shown in Table 116.

Table 116. 2-Wire Slave Addresses

SLAVE ADDRESS	PROTOCOL	ADDRESS BYTE RANGE	INTERNAL MEMORY RANGE ACCESSED
6Ch	I²C	00h-FFh	000h-0FFh
16h	SMBUS	00h-7Fh	100h-17Fh
	I²C	80h-FFh	180h-1FFh

Read/Write Bit

The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction, with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction, with the following bytes being read from the slave by the master.

Bus Timing

The IC is compatible with any bus timing up to 400kHz. See the *Electrical Characteristics* table for timing details. No special configuration is required to operate at any speed. Figure 38 shows an example of standard 2-wire bus timing.

2-Wire Bus Timing Diagram

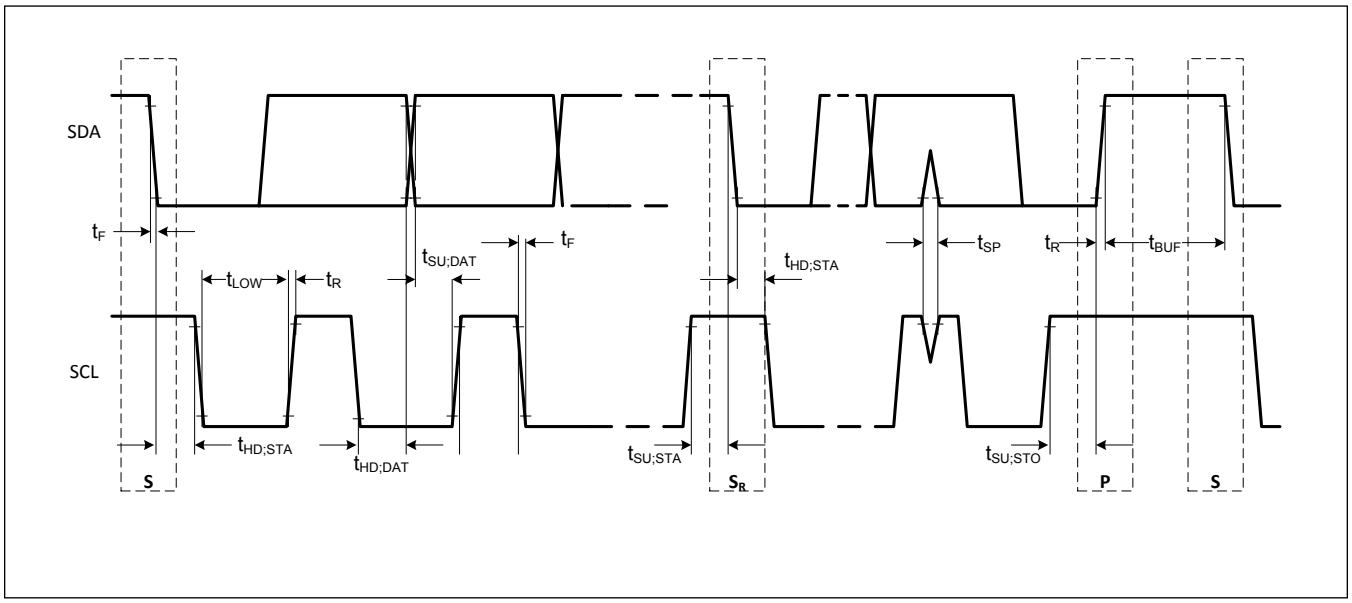


Figure 38. 2-Wire Bus Timing Diagram

I²C Protocols

The following 2-wire communication protocols must be used by the bus master to access IC memory locations 000h to 1FFh. Addresses 000h to 0FFh and 180h to 1FFh can be read continuously. Addresses 100h to 17Fh must be read one word at a time. These protocols follow the standard I²C specification for communication.

I²C Write Data Protocol

The Write Data protocol is used to transmit data to the IC at memory addresses from 000h to 1FFh. Addresses 000h to 0FFh and 180h and 1FFh can be written as a block. Addesses 100h to 17Fh must be written one word at a time. The memory address is sent by the bus master as a single byte value immediately after the slave address, followed by an ACK from the IC. The LSB of the data to be stored is written immediately after the memory address byte, followed by an ACK from the IC. The MSB of the data to be stored is written next, followed by an ACK from the IC. Because the address is automatically incremented after the least significant bit (LSb) of the MSB of each word received by the IC, the LSB of the data at the next memory address can be written immediately after the acknowledgment of the MSB of data at the previous address. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit. If the bus master continues an auto-incremented write transaction beyond address 0FFh or 1FFh, the IC ignores the data. Data is also ignored on writes to read-only addresses but not reserved addresses. Do not write to reserved address locations. See Figure 39 for an example Write Data communication sequence.

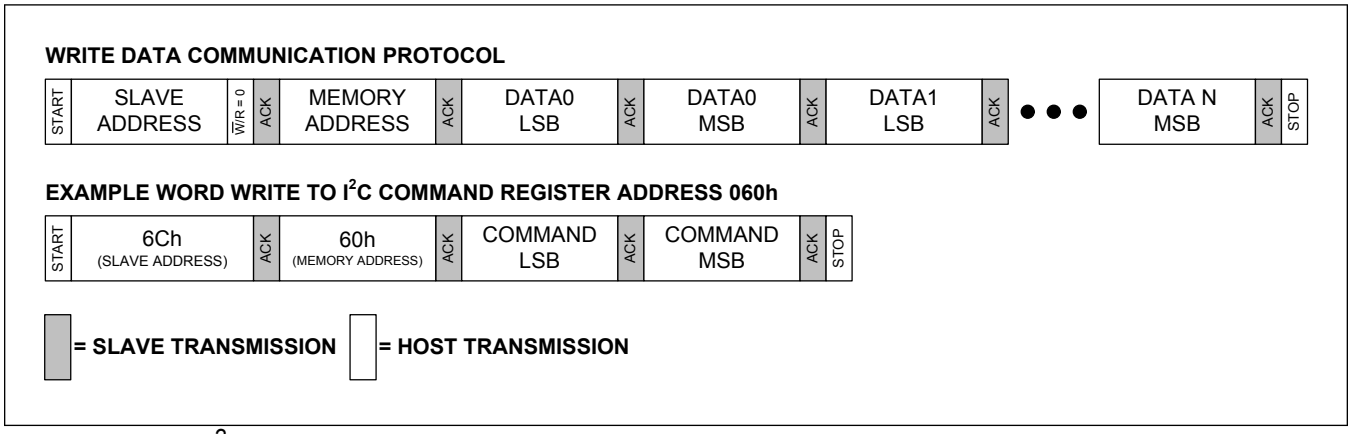


Figure 39. Example I²C Write Data Communication Sequence

I²C Read Data Protocol

The Read Data protocol is used to transmit data from IC memory locations 000h to 1FFh . Addresses 000h to 0FFh and 180h to 1FFh can be read as a block. Addresses 100h to 17Fh must be read as individual words. The memory address is sent by the bus master as a single byte value immediately after the slave address. Immediately following the memory address, the bus master issues a REPEATED START followed by the slave address. The IC ACKs the address and begin transmitting data. A word of data is read as two separate bytes that the master must ACK. The LSB is read first, followed by an ACK from the master. The MSB is read next, followed by an ACK from the master. Because the address is automatically incremented after the least significant bit (LSb) of the MSB of each word transmitted by the IC, the LSB of the data at the next memory address can be read immediately after the acknowledgment of the MSB of data at the previous address. The master indicates the end of a read transaction by sending a NACK followed by a STOP. If the bus master continues an auto-incremented read transaction beyond memory address 0FFh or 1FFh, the IC transmits all 1s until a NACK or STOP is received. Data from reserved address locations is undefined. See Figure 40 for an example Read Data communication sequence.

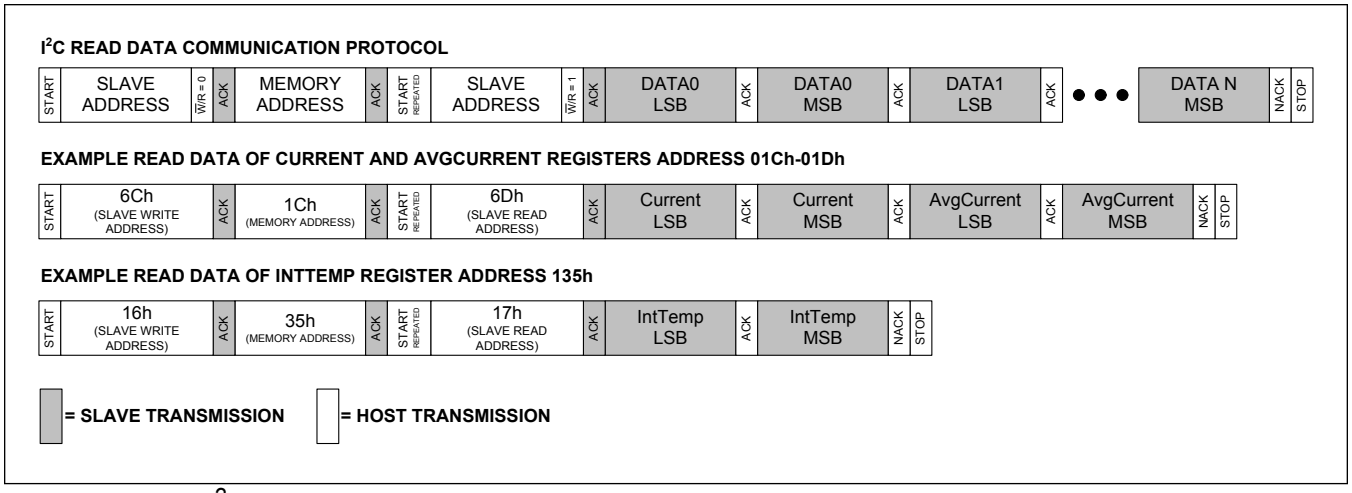


Figure 40. Example I²C Read Data Communication Sequence

SBS Protocols

The following 2-wire communication protocols must be used by the bus master to access IC memory locations 100h to 17Fh. These protocols follow the smart battery specification for communication.

SBS Write Word Protocol

The Write Word protocol is used to transmit data to IC memory addresses between 100h and 17Fh that do not require the Write Block protocol. The memory address is sent by the bus master as a single byte LSB value immediately after the slave address, the MSb of the address is omitted. The LSB of the data to be stored is written immediately after the memory address byte is acknowledged, followed by the MSB. A PEC byte can follow the data word, but the data word is written without checking the validity of the PEC. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit. Data is ignored on writes to read-only addresses but not reserved addresses. Do not write to reserved address locations. The Write Word protocol should not be used to write to addresses supported by the Write Block protocol, use Write Block at these locations instead. See Figure 41 for an example Write Word communication sequence.

Example SBS Write Word Communication Sequence

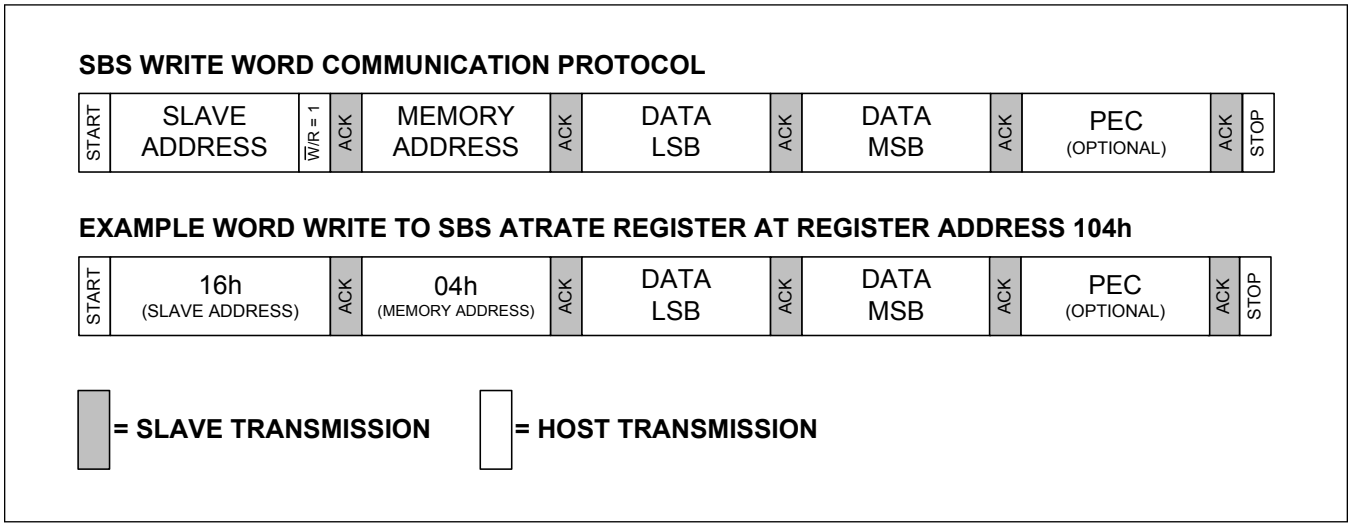


Figure 41. Example SBS Write Word Communication Sequence

SBS Read Word Protocol

The Read Word protocol is used to read data from the IC at memory addresses between 100h and 17Fh. The memory address is sent by the bus master as a single byte LSB value immediately after the slave address, the MSb of the address is ignored. The LSB of the data is read immediately after the memory address byte is acknowledged, followed by the MSB. A PEC byte follows the data word. The master indicates the end of a write transaction by sending a STOP or Repeated START after not acknowledging the last received byte. Data from reserved address locations is undefined. The Read Word protocol should not be used to read from addresses supported by the Read Block protocol, use Read Block at these locations instead. See Figure 42 for an example Read Word communication sequence.

Example SBS Read Word Communication Sequence

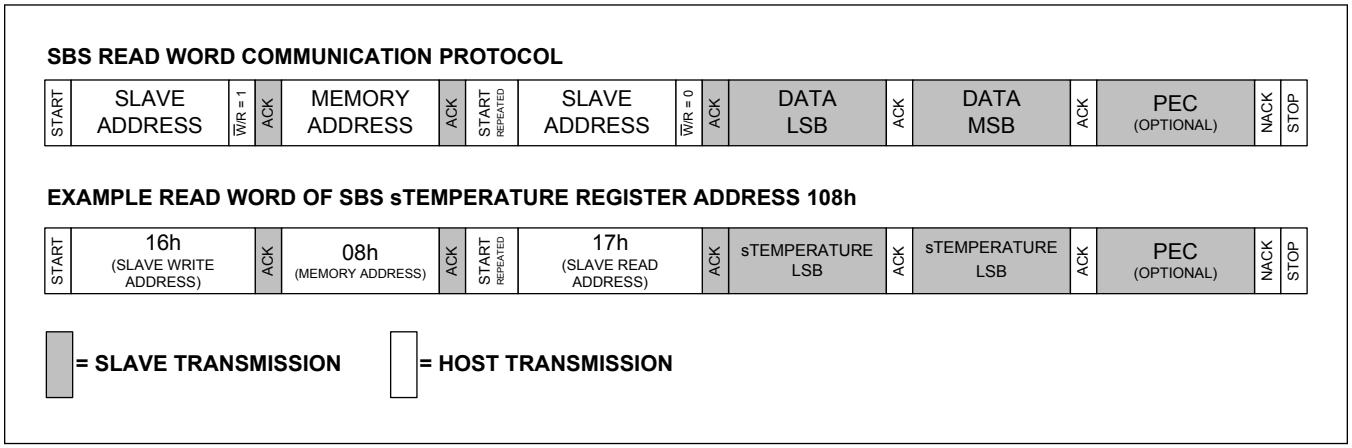


Figure 42. Example SBS Read Word Communication Sequence

SBS Write Block Protocol

The SBS Write Block protocol is not supported by the IC. Use the Write Data command sequence to the corresponding nonvolatile memory locations to update Write/Read Block register locations. See Table 106.

SBS Read Block Protocol

The Read Block protocol is similar to the Read Word protocol except the master reads multiple words of data at once. A data size byte is transmitted by the IC immediately after the memory address byte and before the first byte of data to be read. The Read Block protocol is only supported at the register locations shown in Table 117. PEC error checking is provided by the Read Block protocol if nNVCfg0.enSBS = 1. Figure 43 shows an example Read Block communication sequence.

Example SBS Read Block Communication Sequence

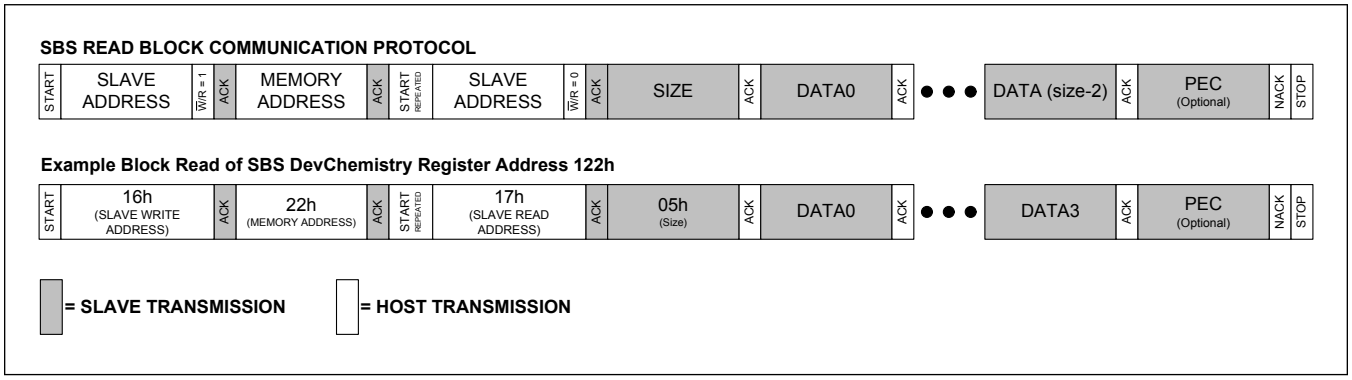


Figure 43. Example SBS Read Block Communication Sequence

Valid SBS Read Block Registers

Table 117. Valid SBS Read Block Registers

ADDRESS	REGISTER	SIZE BYTE MAX VALUE	FORMAT
0120h	sManfctName	0Ah	ASCII String
0121h	sDeviceName	0Ch	ASCII String
0122h	sDevChemistry	05h	ASCII String
0123h	sManfctData	1Ah	Hexadecimal
011Ch	sSerialNumber	08h	Hexadecimal
0170h	sManfctInfo	18h	Hexadecimal

Packet Error Checking

SBS read functions support packet error checking (PEC) if nNVCfg0.enSBS is enabled. The host system is responsible for verifying the CRC value it receives and taking action as a result. SBS write functions accept a PEC byte but complete the write function regardless of the value of the PEC.

The CRC can be generated by the host using a circuit consisting of a shift register and XOR gates as shown in Figure 44, or it can be generated in software using the polynomial $X^8 + X^2 + X^1 + 1$. Refer to the *Smart Battery Data Specification* for more information.

PEC CRC Generation Block Diagram

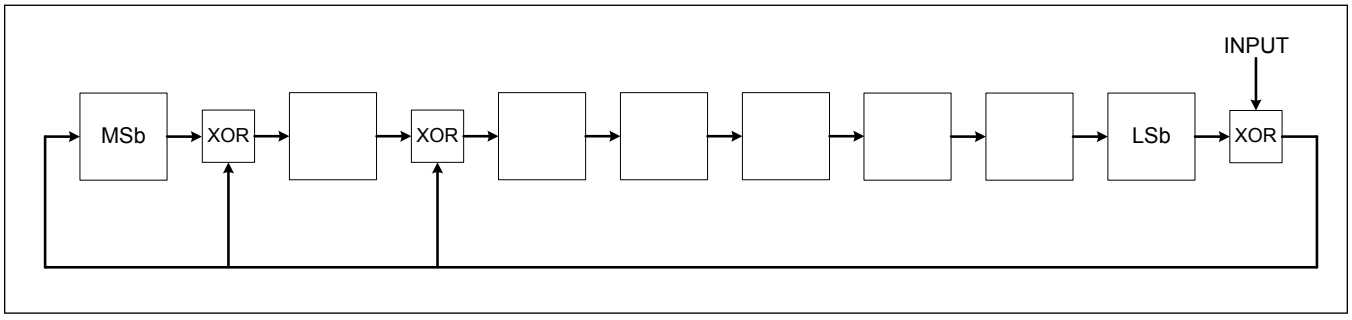


Figure 44. PEC CRC Generation Block Diagram

1-Wire Bus System

The 1-Wire version of the IC communicates to a host through a Maxim 1-Wire interface. The 1-Wire bus is a system that has a single bus master and one or more slaves. A multi-drop bus is a 1-Wire bus with multiple slaves, while a single-drop bus has only one slave device. In all instances, this IC is a slave device. The bus master is typically a microprocessor in the host system. The discussion of this bus system consists of five topics: 64-bit net address, CRC generation, hardware configuration, transaction sequence, and 1-Wire signaling.

Hardware Configuration

Because the 1-Wire bus has only a single line, it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus with open-drain or tri-state output drivers. The IC uses an open-drain output driver as part of the bidirectional interface circuitry shown in Figure 45. If a bidirectional pin is not available on the bus master, separate output and input pins can be connected together. Communication speed is controlled by the OD/SCL pin. Connect OD/SCL to PACK- to enable communication at standard speed. Connect OD/SCL to the REG3 pin to enable communication at overdrive speed.

The 1-Wire bus must have a pullup resistor on the host side of the bus. A value between 2kΩ and 5kΩ is recommended for most applications. The idle state for the 1-Wire bus is logic high. If, for any reason, a bus transaction must be suspended, the bus must be left in the idle state to properly resume the transaction later. Note that if the bus is left low for more than t_{LOW0}, slave devices on the bus begin to interpret the low period as a reset pulse, effectively terminating the transaction.

1-Wire Bus Interface Circuitry

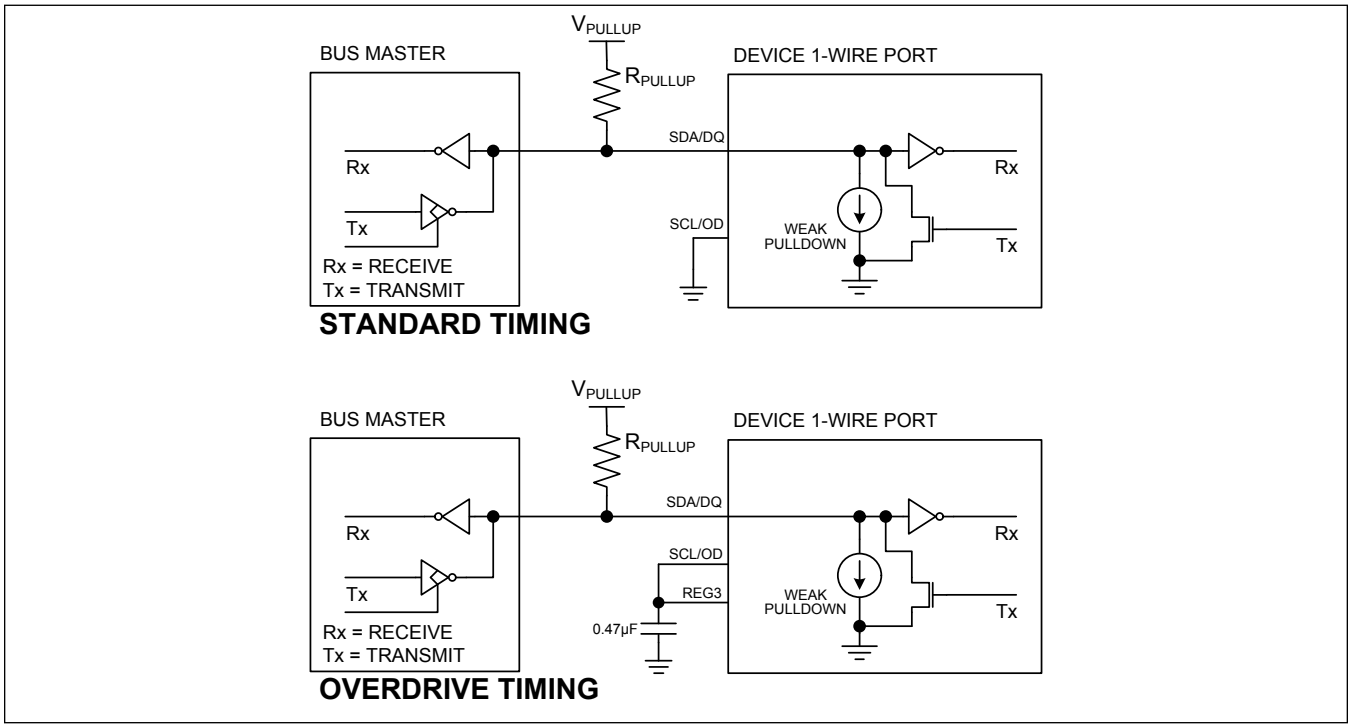


Figure 45. 1-Wire Bus Interface Circuitry

64-Bit Net Address (ROM ID)

The 1-Wire net address is 64 bits in length. The term net address is synonymous with the ROM ID or ROM code terms used in other 1-Wire documentation. The value of the net address is stored in nonvolatile memory and cannot be changed. In a 1-Wire standard net address, the first 8 bits of the net address are the 1-Wire family code. This value is the

same for all ICs of the same type. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. Table 118 details the Net Address data format. The 64-bit net address and the 1-Wire I/O circuitry built into the device enable the 1-Wire version of the IC to communicate through the 1-Wire protocol detailed in this data sheet.

Table 118. 1-Wire Net Address Format

MSb: 8-Bit CRC	48-Bit Serial Number	LSb: 8-Bit Family Code (26h)

I/O Signaling

The 1-Wire bus requires strict signaling protocols to ensure data integrity. The four protocols used by the IC are as follows: the initialization sequence (reset pulse followed by presence pulse), write 0, write 1, and read data. The bus master initiates all signaling except for the presence pulse.

Reset Time Slot

The initialization sequence required to begin any communication with the IC is shown in Figure 46. The bus master transmits (Tx) a reset pulse for t_{RSTL}. The bus master then releases the line and goes into Receive mode (Rx). The 1-Wire bus line is then pulled high by the pullup resistor. After detecting the rising edge on the DQ pin, the IC waits for t_{PDH} and then transmits the presence pulse for t_{PDL}. A presence pulse following a reset pulse indicates that the IC is ready to accept a net address command.

1-Wire Initialization Sequence

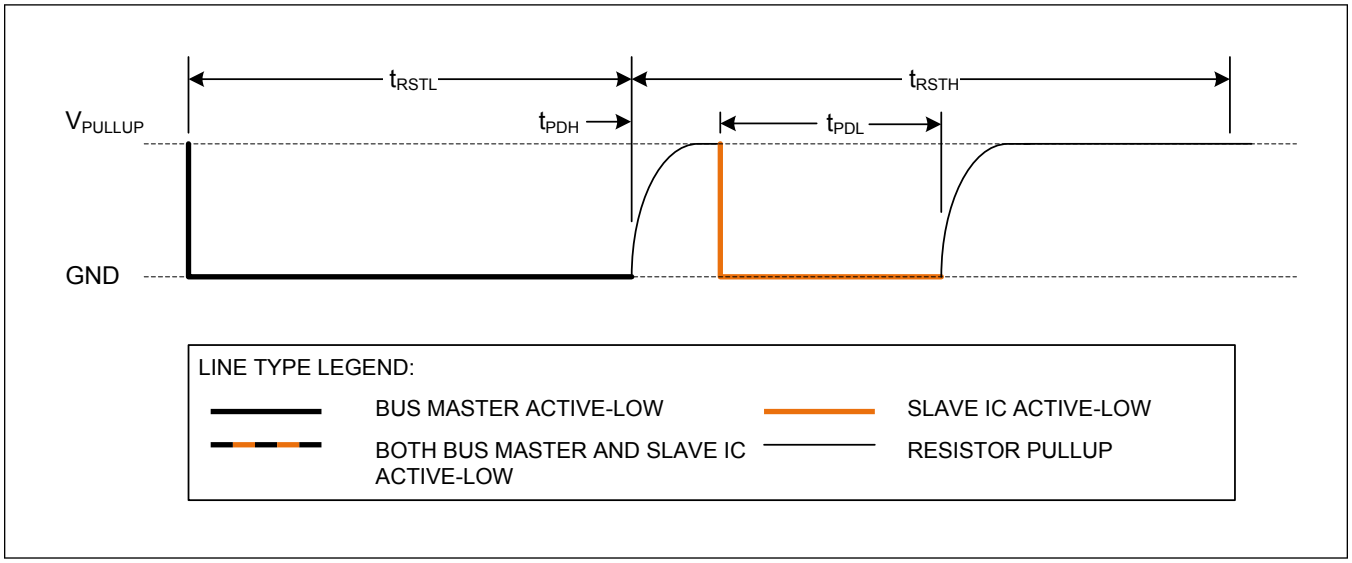


Figure 46. 1-Wire Initialization Sequence

Write Time Slots

A write time slot is initiated when the bus master pulls the 1-Wire bus from a logic-high (inactive) level to a logic-low level. There are two types of write time slots: Write 1 and Write 0. All write time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles. The IC samples the 1-Wire bus line between t_{LOW1_MAX} and t_{LOW0_MIN} after the line falls. If the line is high when sampled, a write 1 occurs. If the line is low when sampled, a Write 0 occurs. The sample window is illustrated in Figure 47. For the bus master to generate a Write 1 time slot, the bus line must be pulled low and then released, allowing the line to be pulled high less than t_{RDV} after the start of the write time slot. For the host to generate a Write 0 time slot, the bus line must be pulled low and held low for the duration of the write time slot.

Read Time Slots

A read-time slot is initiated when the bus master pulls the 1-Wire bus line from a logic-high level to a logic-low level. The bus master must keep the bus line low for at least 1µs and then release it to allow the IC to present valid data. The bus master can then sample the data t_{RDV} from the start of the read-time slot. By the end of the read-time slot, the IC releases the bus line and allows it to be pulled high by the external pullup resistor. All read-time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles. See Figure 47 and the timing specifications in the *Electrical Characteristics* table for more information.

1-Wire Write and Read Time Slots

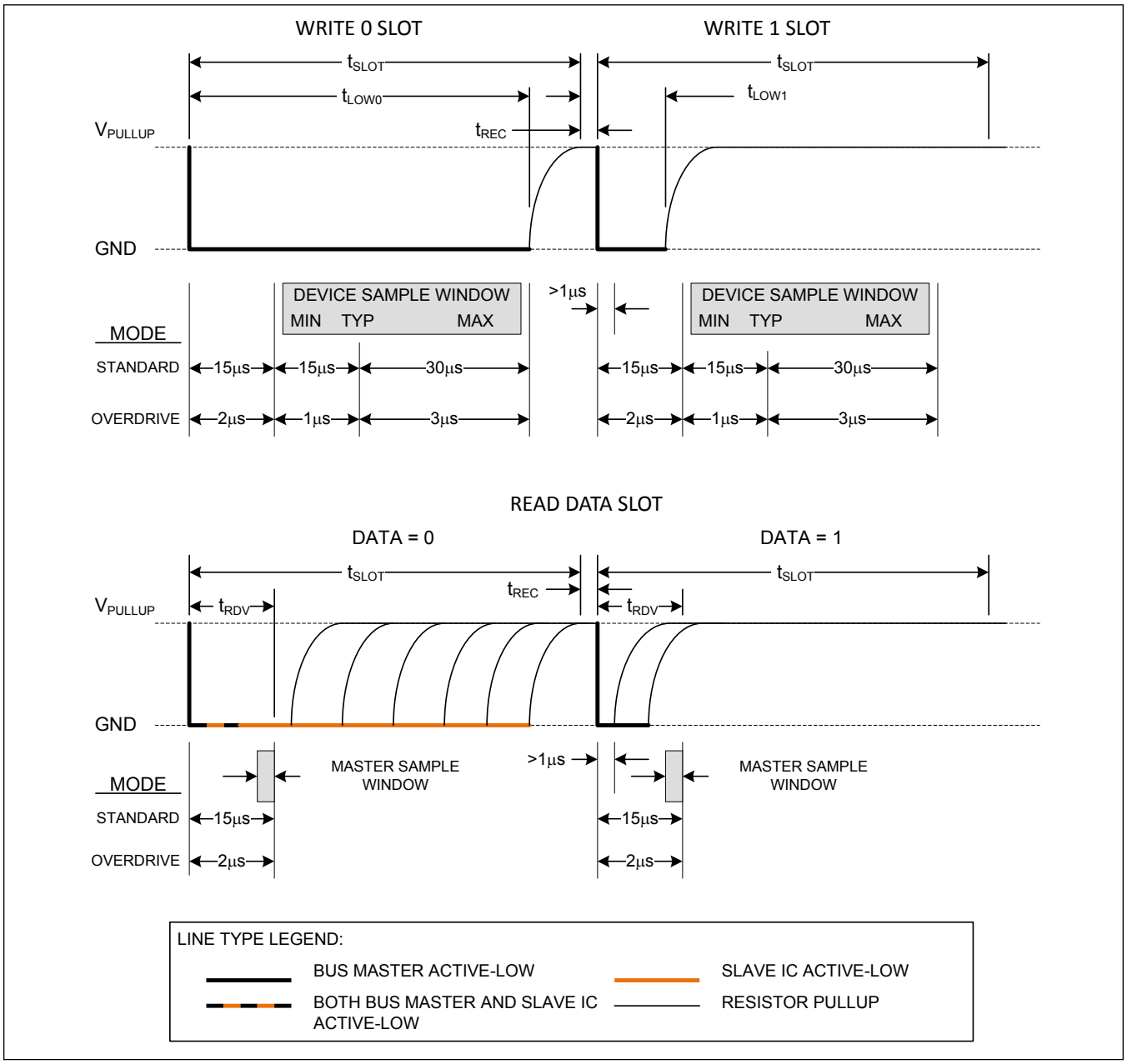


Figure 47. 1-Wire Write and Read Time Slots

Transaction Sequence

The protocol for accessing the IC through the 1-Wire port is as follows:

- Initialization
- Net Address Command
- Function Command(s)
- Data Transfer (not all commands have data transfer)

Net Address Commands

Once the bus master has detected the presence of one or more slaves, it can issue one of the net address commands described in the following sections. The name of each net address command (ROM command) is followed by the 8-bit op code for that command in square brackets.

Read Net Address [33h]

This command allows the bus master to read the ICs 1-Wire net address. This command can only be used if there is a single slave on the bus. If more than one slave is present, a data collision occurs when all slaves try to transmit at the same time (open-drain produces a wired-AND result).

Match Net Address [55h]

This command allows the bus master to specifically address one IC on the 1-Wire bus. Only the addressed IC responds to any subsequent function command. All other slave devices ignore the function command and wait for a reset pulse. This command can be used with one or more slave devices on the bus.

Skip Net Address [CCh]

This command saves time when there is only one IC on the bus by allowing the bus master to issue a function command without specifying the address of the slave. If more than one slave device is present on the bus, a subsequent function command can cause a data collision when all slaves transmit data at the same time.

Search Net Address [F0h]

This command allows the bus master to use a process of elimination to identify the 1-Wire net addresses of all slave devices on the bus. The search process involves the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit location of the net address. After one complete pass through all 64 bits, the bus master knows the address of one device. The remaining devices can then be identified on additional iterations of the process. Refer to Chapter 5 of the *Book of iButton® Standards* for a comprehensive discussion of a net address search, including an actual example (www.maximintegrated.com/iButtonBook).

iButton is a registered trademark of Maxim Integrated Products, Inc.

1-Wire Functions

After successfully completing one of the net address commands, the bus master can access the features of the IC with either a Read Data or Write Data function command described in the following sections. Any other IC operation such as a Compute MAC operation is accomplished by writing to the COMMAND register. See the *Nonvolatile Memory Commands* section for details.

Read Data [69h, LL, HH]

This command reads data from the IC starting at memory address HHLL. Any memory address from 0000h to 01FFh is a valid starting address. The LSb of the data in address HHLL is available to be read immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is received, the LSb of the data at address HHLL + 1 is available to be read immediately after the MSb of the data at address HHLL. If the bus master continues to read beyond address 01FFh, data is undefined. Addresses labeled “Reserved” in the memory map contain undefined data values. The Read Data command can be terminated by the bus master with a reset pulse at any bit boundary. Reads from nonvolatile memory addresses return the data in the shadow RAM. A Recall Data command is required to transfer data from nonvolatile memory to the shadow RAM. See the *Nonvolatile Memory Commands* section for details. See Figure 48 for an example Read Data communication sequence.

Write Data [6Ch, LL, HH]

This command writes data to the IC starting at memory address HHLL. Any memory address from 0000h to 01FFh is a valid starting address. The LSb of the data to be stored at address HHLL can be written immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is written, the LSb to be stored at address HHLL + 1 can be written immediately after the MSb to be stored at address HHLL. If the bus master continues to write beyond address 01FFh, the data is ignored by the IC. Writes to read-only addresses and locked memory blocks are ignored. Do not write to RESERVED address locations. Incomplete bytes are not written. Writes to unlocked nonvolatile memory addresses modify the shadow RAM. A Copy NV Block command is required to transfer data from the shadow RAM to nonvolatile memory. See the *Nonvolatile Memory Commands* section for details. See Figure 48 for an example Write Data communication sequence.

Example 1-Wire Communication Sequences

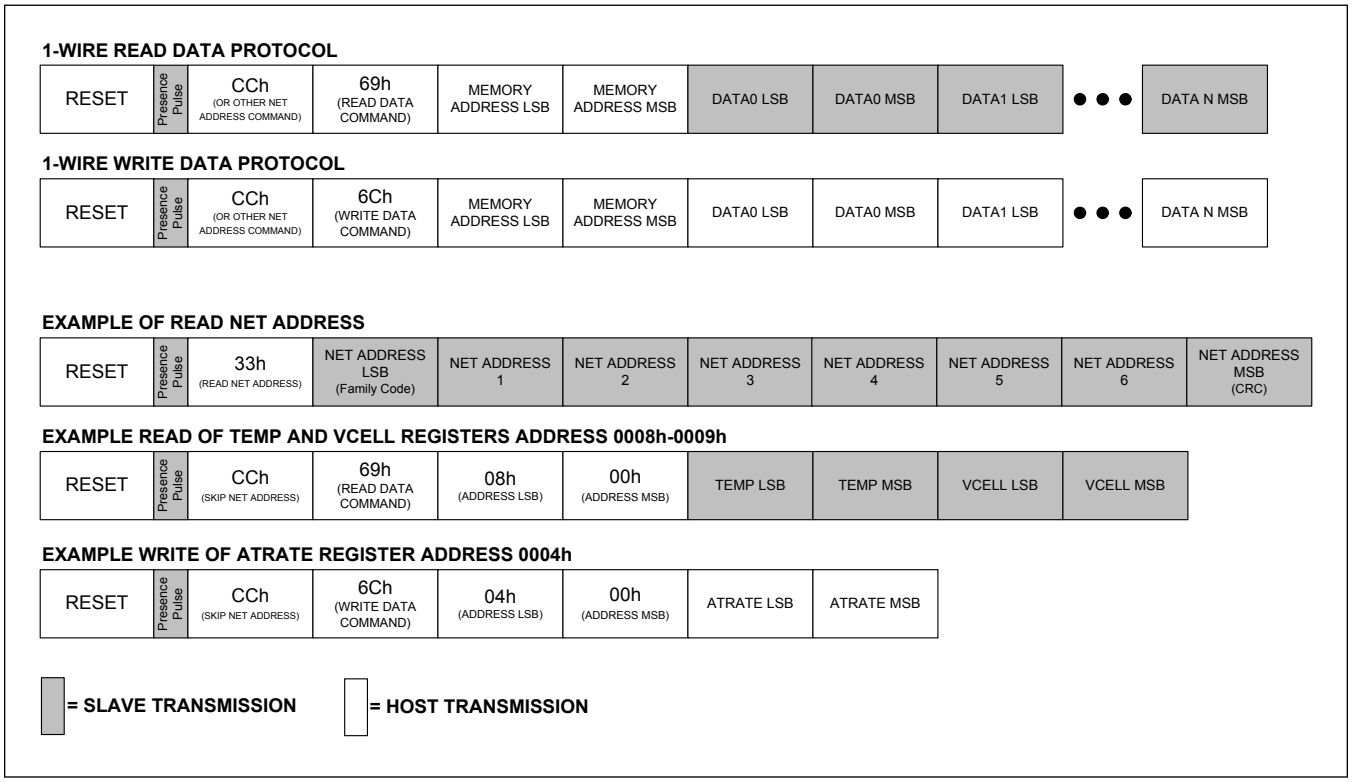


Figure 48. Example 1-Wire Communication Sequences

Summary of Commands

Any operation other than writing or reading a memory location is executed by writing the appropriate command to the Command or Config2 registers. Table 119 lists all function commands understood by the IC. For both 1-Wire and 2-Wire communication, the function command must be written to the Command (060h) or Config2 (0ABh) registers. Device commands are described in detail in the *Authentication*, *Nonvolatile Memory*, *Reset*, and *Power Up* sections of the data sheet.

Table 119. All Function Commands

COMMAND	TYPE	REGISTER	HEX	DESCRIPTION
Compute MAC *Without* ROM ID	SHA	060h	3600h	Computes hash operation of the message block with logical 1s in place of the ROM ID.

Table 119. All Function Commands (continued)

COMMAND	TYPE	REGISTER	HEX	DESCRIPTION
Compute MAC *With* ROM ID	SHA	060h	3500h	Computes hash operation of the message block including the ROM ID.
Compute Next Secret *Without* ROM ID	SHA	060h	3000h	Computes hash operation of the message block with logical 1s in place of the ROM ID. The result is then stored as the new Secret.
Compute Next Secret *With* ROM ID	SHA	060h	3300h	Computes hash operation of the message block including the ROM ID. The result is then stored as the new Secret.
Clear Secret	SHA	060h	5A00h	Resets the SHA-256 Secret to a value of all 0s.
Lock Secret	SHA	060h	6000h	Permanently locks the SHA-256 Secret.
Copy NV Block	Memory	060h	E904h	Copies all shadow RAM locations to nonvolatile memory at the same time.
NV Recall	Memory	060h	E001h	Recalls all nonvolatile memory to RAM.
History Recall	Memory	060h	E2XXh	Recalls a page of nonvolatile memory history into RAM page 1Eh.
NV Lock	Memory	060h	6AXXh	Permanently locks an area of memory. See the *Memory Locks* section for details.
Hardware Reset	Reset	060h	000Fh	Recalls nonvolatile memory into RAM and resets the IC hardware. Fuel gauge operation is not reset.
Fuel Gauge Reset	Reset	0ABh	8000h	Restarts the fuel gauge operation without affecting nonvolatile shadow RAM settings.

16-Reading ADC FIFO Feature

The IC supports an ADC FIFO feature, which allows a user-triggered acquisition cycle of 16-samples of AvgVCell and AvgCurrent, sampled every 2.8s, for a total acquisition time of 45s. AvgCurrent and AvgVCell filtering is configurable (see *nFilterCfg*) with a default filter time-constant of 5.625s (AvgCurrent) and 45s (AvgVCell). Set FilterCfg = 0x0E83 for faster filtering to better match the FIFO update rate (2.8s for AvgCurrent and 11.25s for AvgVCell).

Set Config2.ADCFIFOen = 1 and disable nonvolatile nConfig.ADCFIFOen = 0 to trigger a single acquisition cycle. On completion of acquisition, this bit self-resets to 0. Enable nonvolatile nConfig.ADCFIFOen = 1 to keep the ADC FIFO in a continuous loop without termination. Since the ADC FIFO uses the same register-space as SBS, it is incompatible with SBS. Set nNVCfg0.enSBS = 0 to prevent collision between these incompatible features.

The FIFO is useful for measuring system shutdown consumption during production testing. Use the following sequence to measure the system consumption during system shutdown:

1. Ensure nNVCfg0.enSBS = 0 (generally just once during initial NVM configuration).
2. Host enables the ADC FIFO (write Config2.ADCFIFOEn = 1) and sets FilterCfg = 0E83h.
3. Host shuts everything down (except pack and the IC).
4. Host remains shut down for at least 6 seconds (ideally closer to 45s for more readings).
5. Host boots up and inspects the FIFO (slave 16h registers 00h to 1Fh) to understand the system consumption during system shutdown.

NOTE: I^2C addresses on slave 16h from 00h to 7Fh must be read one word at a time.

The FIFO can be used in other applications to acquire voltage and current data with less frequent polling or system wakeup by setting nonvolatile nConfig.ADCFIFOen = 1.

The memory map is shown in Table 120.

Table 120. I^2C Slave Address = 0x16 (SBS Memory Area)

INDEX	PAGE = 0	PAGE = 1	PAGE = 2	PAGE = 4
0	CurrentBuf0	VoltBuf0	CurrentMax0	VoltMax0
1	CurrentBuf1	VoltBuf1	CurrentMin0	VoltMin0
2	CurrentBuf2	VoltBuf2	CurrentMax1	VoltMax1

Table 120. I²C Slave Address = 0x16 (SBS Memory Area) (continued)

INDEX	PAGE = 0	PAGE = 1	PAGE = 2	PAGE = 4
3	CurrentBuf3	VoltBuf3	CurrentMin1	VoltMin1
4	CurrentBuf4	VoltBuf4	CurrentMax2	VoltMax2
5	CurrentBuf5	VoltBuf5	CurrentMin2	VoltMin2
6	CurrentBuf6	VoltBuf6	CurrentMax3	VoltMax3
7	CurrentBuf7	VoltBuf7	CurrentMin3	VoltMin3
8	CurrentBuf8	VoltBuf8	CurrentMax4	VoltMax4
9	CurrentBuf9	VoltBuf9	CurrentMin4	VoltMin4
A	CurrentBufA	VoltBufA	—	—
B	CurrentBufB	VoltBufB	—	—
C	CurrentBufC	VoltBufC	—	—
D	CurrentBufD	VoltBufD	—	—
E	CurrentBufE	VoltBufE	—	—
F	CurrentBufF	VoltBufF	ADCIndex	—

Appendix A: Reading History Data Pseudo-Code Example

The following pseudo-code can be used as a reference for reading history data from the IC. The code first reads all flag information, tests all flag information, then reads all valid history data into a two-dimensional array. Afterwards, the HistoryLength variable indicates the depth of the history array data. Note before starting this sequence, the Write Protection should be disabled by writing 0x0000 to the CommStat register (0x61) two times in a row. At the conclusion of the pseudo-code, the Write Protection should be enabled by writing 0x00F9 to the CommStat register (0x61) two times in a row.

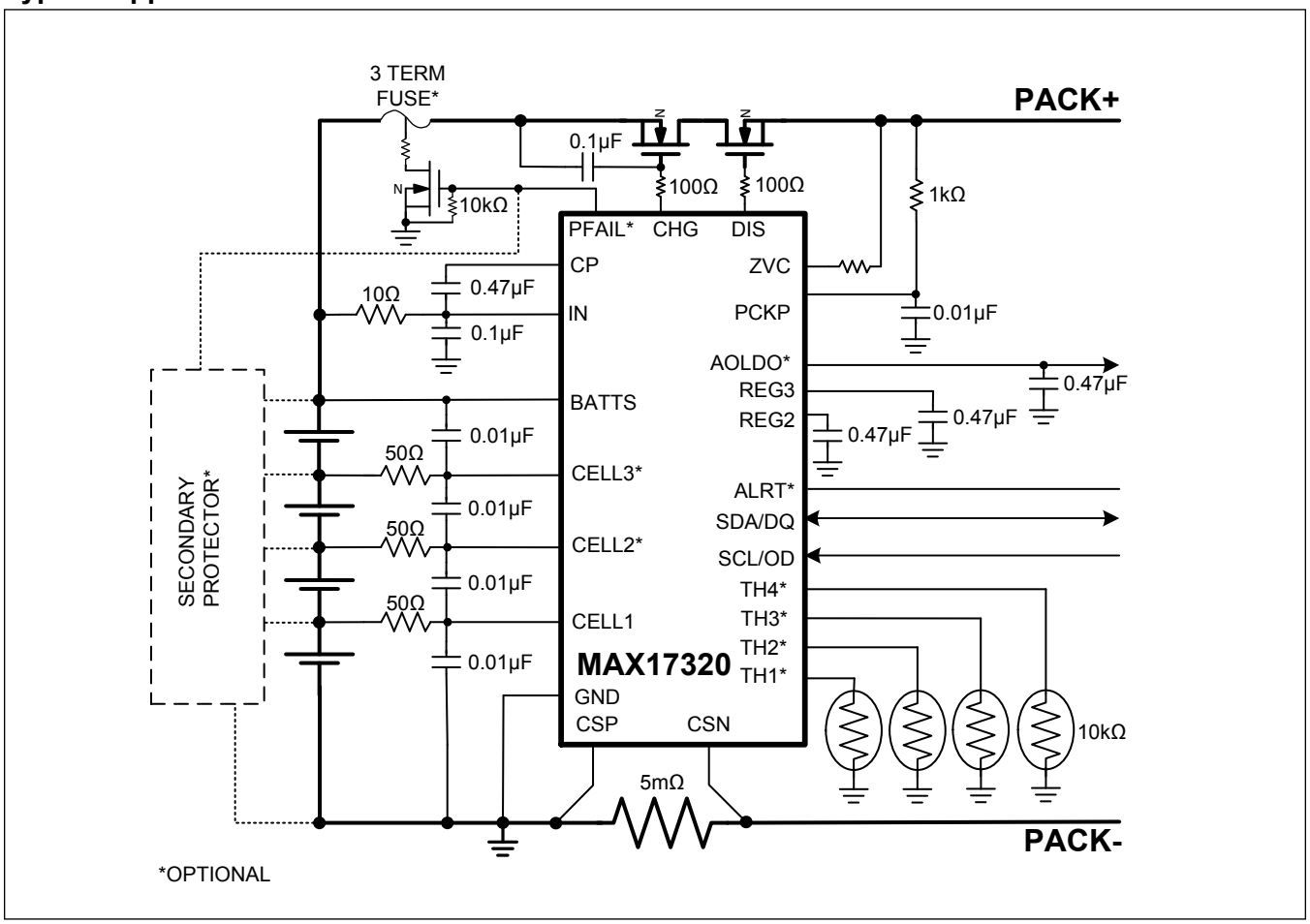
```
Int WriteFlags[26];
Int ValidFlags[26];
Boolean PageGood[100];
Int HistoryData[100][16];
Int HistoryLength;
Int word, position, flag1, flag2, flag3, flag4;
//Read all flag information from the IC
WriteCommand(0xE29C);
Wait(tRECALL);
WriteFlags[0] = ReadData(0x1F2);
WriteFlags[1] = ReadData(0x1F3);
WriteFlags[2] = ReadData(0x1F4);
WriteFlags[3] = ReadData(0x1F5);
WriteFlags[4] = ReadData(0x1F6);
WriteFlags[5] = ReadData(0x1F7);
WriteFlags[6] = ReadData(0x1F8);
WriteFlags[7] = ReadData(0x1F9);
WriteFlags[8] = ReadData(0x1FA);
WriteFlags[9] = ReadData(0x1FB);
WriteFlags[10] = ReadData(0x1FC);
```

```
WriteFlags[11] = ReadData(0x1FD);
WriteFlags[12] = ReadData(0x1FE);
ValidFlags[0] = ReadData(0x1FF);
WriteCommand(0xE29D);
Wait(tRECALL);
ValidFlags[1] = ReadData(0x1F0);
ValidFlags[2] = ReadData(0x1F1);
ValidFlags[3] = ReadData(0x1F2);
ValidFlags[4] = ReadData(0x1F3);
ValidFlags[5] = ReadData(0x1F4);
ValidFlags[6] = ReadData(0x1F5);
ValidFlags[7] = ReadData(0x1F6);
ValidFlags[8] = ReadData(0x1F7);
ValidFlags[9] = ReadData(0x1F8);
ValidFlags[10] = ReadData(0x1F9);
ValidFlags[11] = ReadData(0x1FA);
ValidFlags[12] = ReadData(0x1FB);
//Determine which history pages contain valid data
For loop = 0 to 99
{
    word = (int)( loop / 8 );
    position = loop % 8 ;  //remainder
    flag1 = (WriteFlags[word] >> position) & 0x0001;
    flag2 = (WriteFlags[word] >> (position+8)) & 0x0001;
    flag3 = (ValidFlags[word] >> position) & 0x0001;
    flag4 = (ValidFlags[word] >> (position+8)) & 0x0001;
    if (flag1 || flag2) && (flag3 || flag4)
        PageGood[loop] = True;
    else
        PageGood[loop] = False;
}
//Read all the history data from the IC
HistoryLength = 0;
For loop = 0 to 99
{
    if(PageGood[loop]) == TRUE
    {
        SendCommand(0xE22E + loop);
        Wait(tRECALL);
        HistoryData[HistoryLength][0] = ReadData(0x1F0);
        ...
```

```
        HistoryData[HistoryLength][15] = ReadData(0x1FF);
        HistoryLength++;
    }
}
```

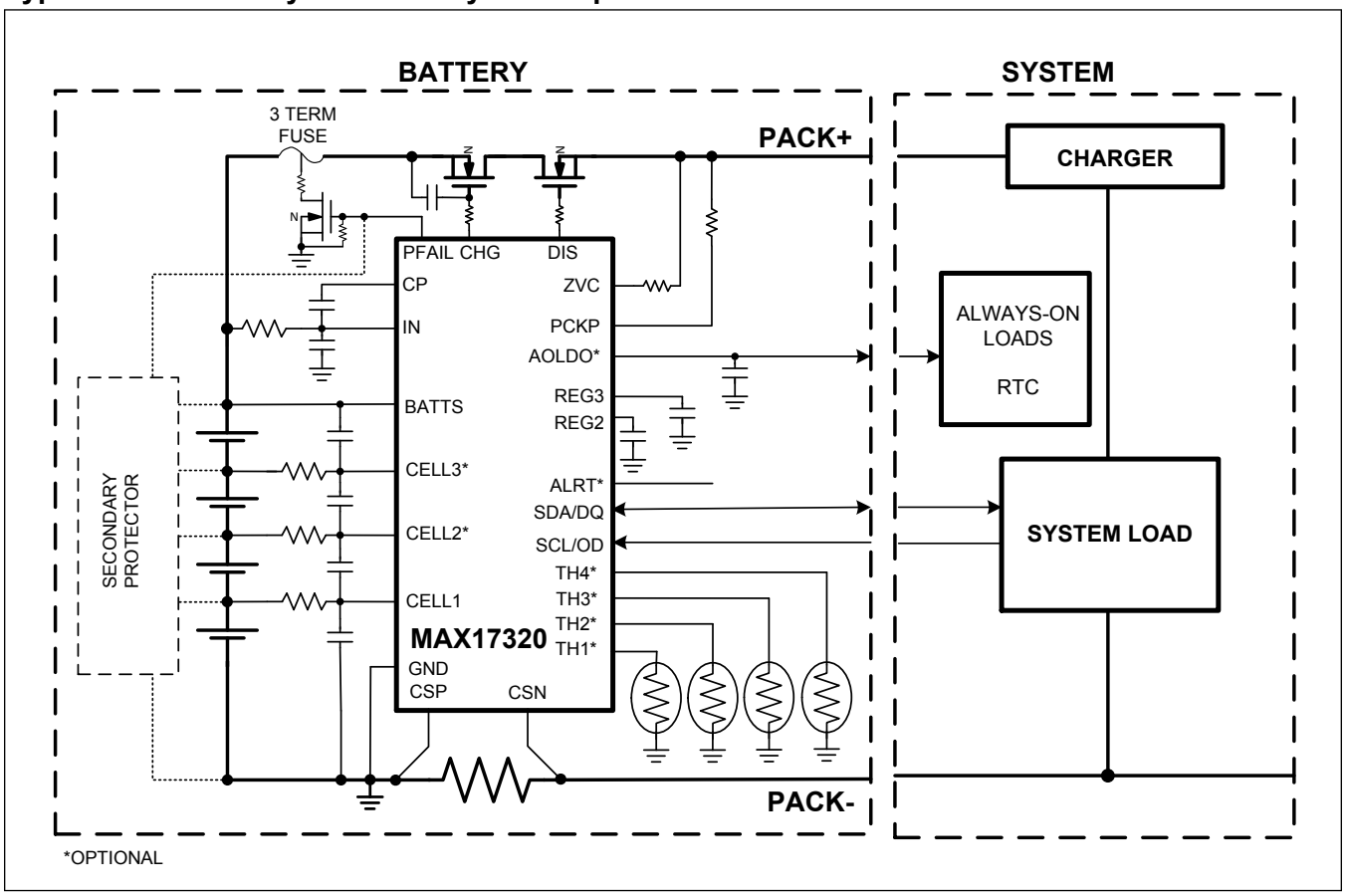
Typical Application Circuits

Typical Application Schematic



Typical Application Circuits (continued)

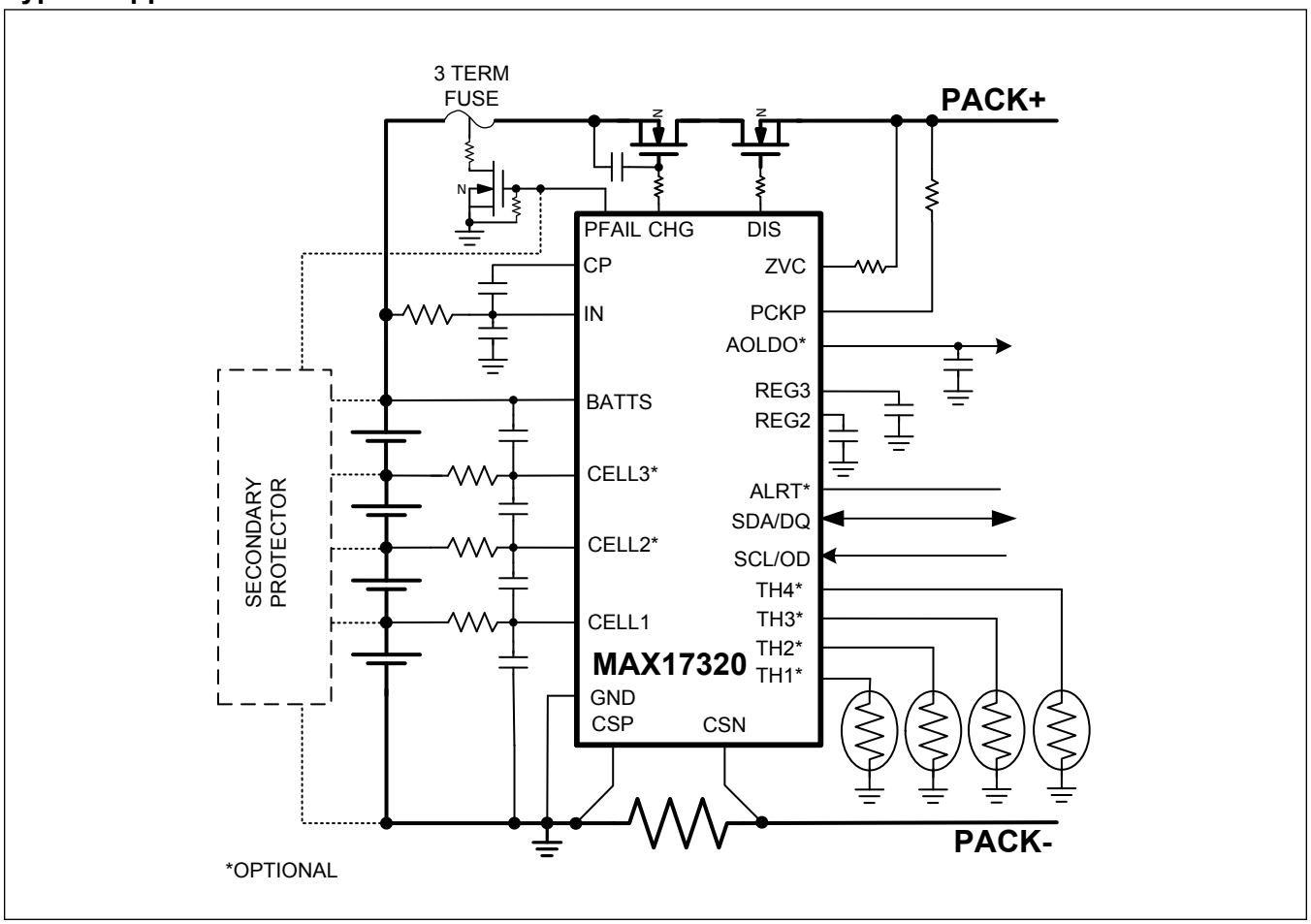
Typical 2S-4S Battery Pack and System Implementation



The IC measures voltage of the cells and balances the charge using internal FETs and the balancing resistors. It also measures current using a sense resistor that is accumulated to give a coulomb count and measures temperature using an on-chip sensor or up to 4 external thermistors, since the cells are likely to be located far away from the IC. The protector control drives a pair of high-side N-channel FETs. The IC also opens a three-terminal fuse for harsh faults that necessitate the battery to be permanently disabled for safety reasons. To power small loads like real-time clocks or housekeeping microcontrollers that need to be always on, the IC provides a regulated output that stays alive even when the protection FETs are opened. This output powers down only when the cells are severely depleted and, therefore, prevents any further drain for safety reasons.

Typical Application Circuits (continued)

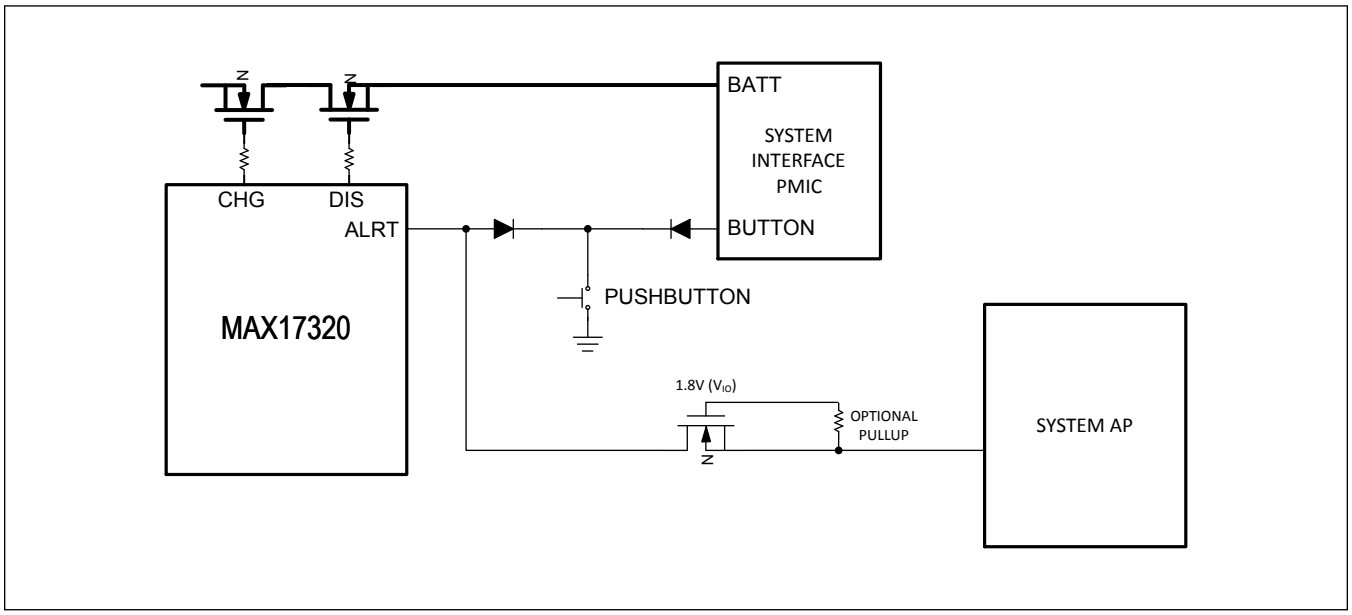
Typical Application with a Fuse



The IC can permanently open a three-terminal fuse with the PFAIL pin when a permanent failure is detected. A secondary protector can also be included to open the three-terminal fuse.

Typical Application Circuits (continued)

Pushbutton Schematic



The IC and the system can share a pushbutton to wake up the system and the IC. The diode on the system interface PMIC blocks the pulldown when there is no supply. This prevents the wakeup for the IC when the system interface PMIC loses power in ship mode. The diode on the ALRT pin prevents the alert pulldown from triggering a button action on the PMIC. This prevents accidental shutdown in the event of an uncleared alert for > 10 seconds. The FET between the IC and the System AP blocks the System AP pulldown from triggering the wakeup when the AP does not have power. The FET acts as a level shifter and passes the pulldown alert signal in both directions when the 1.8V voltage is present.

Ordering Information

PART NUMBER	SHA-256	INTERFACE	PIN-PACKAGE
MAX17320X10+		1-Wire	30 WLP
MAX17320X10+T		1-Wire	30 WLP
MAX17320X12+	Included	1-Wire	30 WLP
MAX17320X12+T	Included	1-Wire	30 WLP
MAX17320X20+		I^2C	30 WLP
MAX17320X20+T		I^2C	30 WLP
MAX17320X22+	Included	I^2C	30 WLP
MAX17320X22+T	Included	I^2C	30 WLP
MAX17320G10+		1-Wire	24 TQFN
MAX17320G10+T		1-Wire	24 TQFN
MAX17320G12+	Included	1-Wire	24 TQFN
MAX17320G12+T	Included	1-Wire	24 TQFN
MAX17320G20+		I^2C	24 TQFN
MAX17320G20+T		I^2C	24 TQFN
MAX17320G22+	Included	I^2C	24 TQFN
MAX17320G22+T	Included	I^2C	24 TQFN
MAX17320G22+009	Included	I^2C	24 TQFN
MAX17320G22+T09	Included	I^2C	24 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/20	Initial release	—
1	4/20	Updated the *General Description* section, *Benefits and Features* section, *Absolute Maximum Ratings* section, *Functional Diagrams* section, *Detailed Description* section, *Protector* section, and *Permanent Failure* section, Table 8, *nUVPrtTh Register (1D0h), nBattStatus Register (1A8h), ProtAlrt Register (0AFh)*, Table 56, *nConfig Register (1B0h)*, Table 103, and *Ordering Information* table; added *Typical Operating Characteristics, Battery Internal Self-Discharge Detection (ISD)* section, *Configuring ISD* section, *Internal Self-Discharge Detection with Cell Balancing* section, *Wake-Up/Shutdown* section, and *Battery Internal Self-Discharge Detection Registers*	1, 18, 26–29, 33–34, 37, 47–48, 50, 64, 73, 75–76, 79, 86–87, 90, 92, 98, 106, 146, 178
2	5/20	Updated the title, *General Description*, and *Battery Internal Self-Discharge Detection (ISD)* section	1, 47
3	5/20	Updated the *Ordering Information* table	178
4	6/20	Updated the *Simplified Block* Diagram, *Typical Application* Schematic, and *Ordering Information* table	1, 170, 178
5	6/20	Updated the *Ordering Information* table	178
6	8/20	Updated Table 51, the *nChgCfg (1C2h) Prequal Configuration* description, *nFullSOCThr Register (1C6h)* description, Table 94, and *Ordering Information* table	95, 100, 105, 129, 178
7	8/20	Updated the *Pin Description* table. Guidance of unused THx pins changed to connect to GND or leave disconnected. Previous guidance to connect unused THx pins to REG3 resulted in all thermistor readings very low.	32
8	9/23	Added *nPReserved0 Register (1C0h), nProtMiscTh2 (1CBh)*. Updated *DevName Register (021h), nConfig Register (1B0h), nNVCfg0 Register (1B8h), nPackCfg Register (1B5h), nSBSCfg Register (1B4h), nBalTh Register (1D4h), nProtCfg Register (1D7h), sManfctAccess Regsiter (100h), sBatteryStatus Register (116h), sDesignVolt Register (119h), sProtectionStatus (151h), PFStatus (152h), sManfctData Registers (123h to 12Fh)*. Updated *Protector* section, *I²C Write Data Protocol* section, *I²C Read Data Protocol* section, *Pin Description, nChgCfg (1C2h) Prequal Configuration* section, *Block* Diagram. Updated *Cell Balancing Circuit* Diagram, *Battery Life Logging* section, *100 Record Life Logging* section, *Memory* section, *NV LOCK [6AXXh]* section	31–33, 35, 36, 64–68, 72, 78, 80, 88, 100,106, 108, 119, 123–137, 150, 152, 154–155, 160–161
9	7/24	Updated *nProtMiscTh2 Register (1CBh), nDelayCfg Register (1DCh), HProtCfg2 Register (0F1h), nNVCfg0 Register (1B8h)*, Figure 34, Table 97, *sPackVoltage Register (109h), sDesignVolt Register (119h),* and *Ordering Information* table	86, 93, 109, 133, 143, 151, 154, 177
10	9/24	Updated *nPReserved0 Register (1C0h)*, restored *Register Description* and *Memory* sections	78–140
11	1/25	Updated *FOTPStat Register (0BBh)*	122

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