19-5071; 12/09

DS2502-E48
48-Bit Node Address Chip

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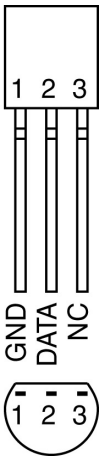
FEATURES

- Factory programmed 48-bit node address chip with 768 bits user-programmable OTP-EPROM communicates with the economy of one signal plus ground
- Provides valid MAC-48/EUI-48 Ethernet address
- Unique, factory lasered and tested 64-bit registration number assures absolute traceability because no two parts are alike
- Built-in multidrop controller ensures compatibility with other 1-Wire® products
- Device is an "add-only" memory where additional data can be programmed into EPROM without disturbing existing data
- Reduces control, address, data, power and programming signals to a single pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbps
- Presence detector acknowledges when reader first applies voltage
- Low cost TO-92 or TSOC surface mount packages
- Reads over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C; programs at 11.5V to 12.0V from -40°C to + 50°C

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

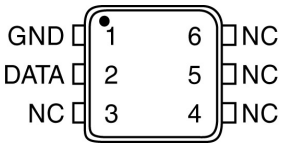
PIN CONFIGURATION

TO-92



BOTTOM VIEW

TSOC PACKAGE



TOP VIEW

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2502-E48+	-40°C to +85°C	3 TO-92
DS2502P-E48+	-40°C to +85°C	6 TSOC
DS2502P-E48+T&R	-40°C to +85°C	6 TSOC

+ Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

DESCRIPTION

The DS2502-E48 is a variant of the DS2502 1024-bit add-only memory. It differs from the standard DS2502 in its custom ROM family code 89h, and the UniqueWare Identifier 5E7h in place of the upper 12 bits of the standard ROM serialization field. Otherwise, the electrical and logical behavior is identical to that of the DS2502. For technical details please refer to the DS2502 data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

The first 32 bytes of the DS2502-E48's EPROM memory contain a globally unique 48-bit node address and are write-protected. The data structure follows the conventions of UniqueWare devices using Default Data Structure (Figure 1). This format is also known as UDP (universal data packet) and is commonly used in 1-Wire APIs. Therefore, if using one of those APIs one can call a high level function to read and verify the inverted CRC16. The UDP is defined in Application Note 114, *1-Wire File Structure*, and the APIs can be found in the *1-Wire Software Development Kits*.

Figure 1. NODE ADDRESS CHIP DATA STRUCTURE

(UNUSED)	$\overline{\text{CRC16}}$ MSB LSB	COMPANY ID VALUE MSB LSB	EXTENSION ID VALUE MSB LSB	PROJECT ID MSB LSB	LENGTH
19 BYTES FFh	2 BYTES	3 BYTES CONSTANT 006035h	3 BYTES SERIALIZATION	4 BYTES CONSTANT 00001129h	1 BYTE 0Ah

HIGH ADDRESS LOW ADDRESS

The data record starts with a length byte (0Ah) and the 4-byte UniqueWare Project ID 00001129h. The next 6 bytes contain the 48-bit node address which consists of an incrementing 24-bit extension identifier and the IEEE-assigned 24-bit company ID value 006035h. An inverted 16-bit CRC ends the data record. The remaining bytes of the 32-byte memory page remain unprogrammed. Neither the 24-bit extension identifier nor the 24-bit company ID are related to the 64-bit ROM registration number. The ROM registration number is used to provide a unique address to access the DS2502-E48 when multidropped on a 1-Wire bus.

EXAMPLE

Assume that a manufacturer's company ID value is 006035h and the 24-bit extension identifier is 67ABCDh. The 48-bit node address value generated from these two numbers is 00603567ABCDh, whose byte and bit representations are illustrated in Figure 2.

Figure 2. SAMPLE NODE ADDRESS VALUE

MOST SIGNIFICANT BYTE					LEAST SIGNIFICANT BYTE	
00	60	35	67	AB	CD	HEX
0000 0000	0110 0000	0011 0101	0110 0111	1010 1011	1100 1101	BINARY
MOST SIGNIFICANT BIT					LEAST SIGNIFICANT BIT	

This information is stored in the DS2502-E48 as 48-bit number with the least significant byte at the lower address. Including the length byte and the inverted CRC, the complete set of data is shown in Figure 3.

Figure 3. PHYSICAL ADDRESS AND DATA MAPPING INSIDE THE DEVICE

ADDRESS	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
DATA	8D	DD	00	60	35	67	AB	CD	00	00	11	29	0A

The four bytes at memory addresses 01h to 04h contain the UniqueWare Project ID 00001129h. The two bytes at addresses 0Bh and 0Ch are the inverted 16-bit CRC over the length byte, Project ID and node address value. The least significant byte of the CRC is stored at address 0Bh. This CRC is generated according to the standardized CRC16 polynomial function $X^{16} + X^{15} + X^2 + 1$. For more details on generating CRC values including examples in both hardware and software, see Application Note 27, *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products*.

The contents of the memory address range 0Dh to 1Fh is FFh. These cells cannot be altered since the whole memory page is write-protected. The memory range from 20h to 7Fh, however, is user-programmable. It can be write-protected by programming the corresponding write-protect bit in the status memory of the DS2502-E48.

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
12/09	Changed the *Ordering Information* to lead free.	1
	Included an explanation of "Default Data Structure" above Figure 1.	2
	Emphasized that the 16-bit CRC is inverted.	2
	Deleted paragraph on how to set up a UniqueWare project.	2
	Inserted actual CRC value to Figure 3.	2
	Reformatted Figures 1 to 3.	2
	Corrected notation of hexadecimal numbers from H to h.	1, 2, 3

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