MAX20754

Dual-Output, Configurable Multiphase Power-Supply Controller with PMBus Interface and Internal Buck Converter

General Description

The MAX20754 is a PMBus™-compatible, dual-output, configurable multiphase power-supply controller for communication and networking applications. The controller is optimized for use with Maxim's Dual Powertrain™ integrated power stages, which support a wide range of output current and voltage requirements. The controller generates six pulse-width modulated outputs, or "phases." The number of phases per output channel is configurable to support high current requirements and one or two output voltages.

This highly versatile controller also includes an integrated switching regulator that supplies power for both the controller and the power-stage devices. The controller features accurate load-current reporting, power-stage temperature monitoring, fault detection, and extensive PMBus-command support. The controller allows the user to save desired PMBus parameters to nonvolatile memory.

The controller can be used with traditional discrete inductors, or with coupled-inductor topologies. Coupled inductors reduce the effective inductor value and size without increasing ripple current, reducing required output capacitance, and improving transient response.

The MAX20754 uses Maxim's advanced modulation scheme (AMS) to provide improved transient response and reduce the required output capacitance compared to conventional pulse-width modulation (PWM) control. The AMS can be disabled if strict fixed-frequency PWM operation is desired.

Applications

- Communication, Networking, Servers, and Storage Equipment
- ASICs, DSPs, and FPGAs
- Microprocessor Chipsets
- DDR Memory

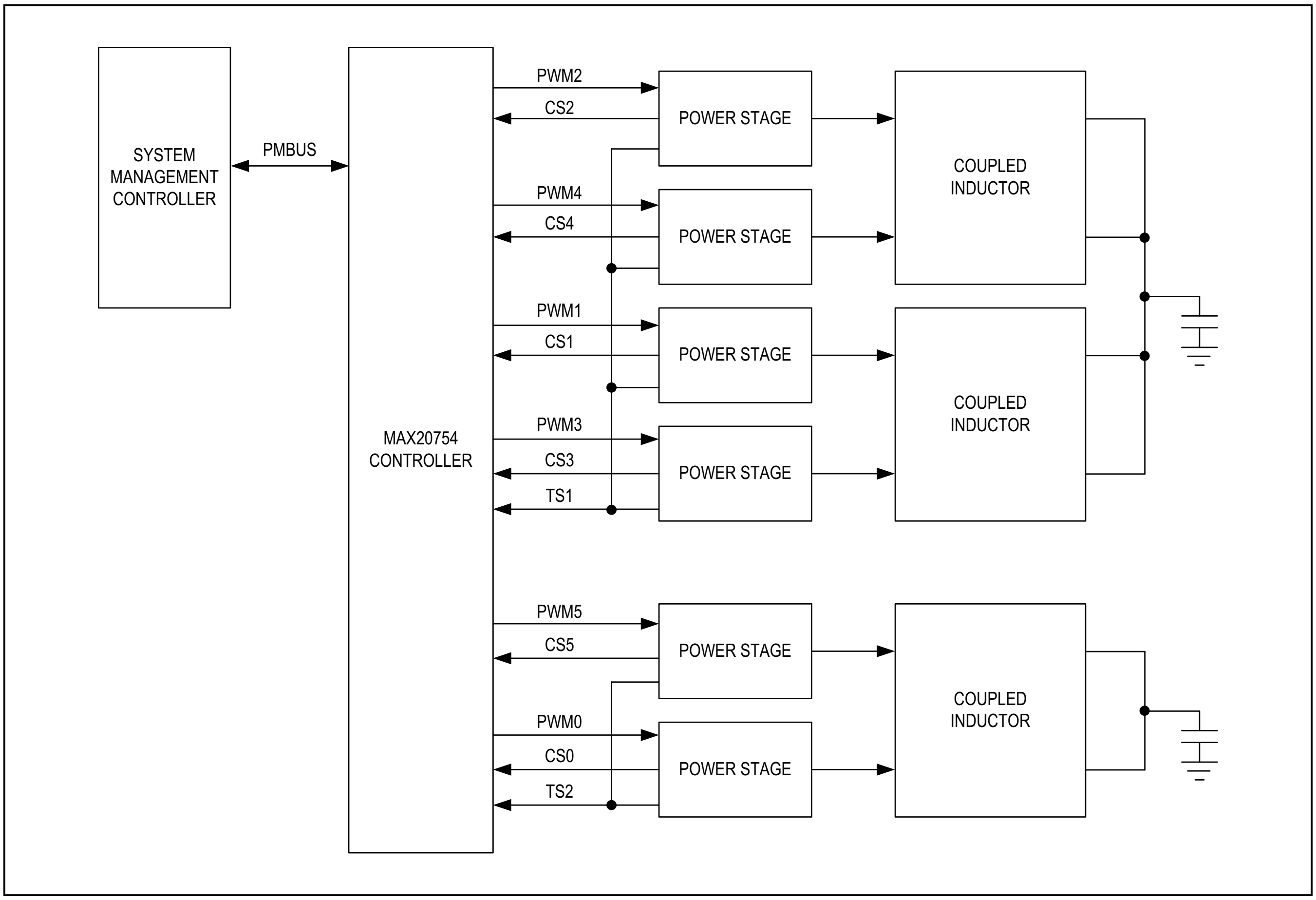
Benefits and Features

- Versatile and Flexible Controller
  - Generates Up to Six PWM Signals
  - Single- or Dual-Voltage Output with Flexible Phase Assignment
  - 0.5V to 2.0V Output-Voltage Range (MAX20754ETMA1+)
  - 0.25V to 2.0V Output-Voltage Range (MAX20754ETMA2+)
  - 4.5V to 16V Input-Voltage Range
  - 300kHz to 800kHz Switching Frequency Range
- High-Power Density in a Small Overall Solution Size
  - Supports Coupled-Inductor Technology
  - Advanced Modulation Scheme Improves Transient Response
  - High-Loop Bandwidth Reduces Output-Capacitance Requirements
  - 48-Pin (7mm x 7mm) TQFN Package
  - Phase-Current Steering for Thermal Balancing
  - Efficient Integrated Internal Switching Regulator Powers Controller and Power Stages
- Simple System Configuration
  - Four External Resistors Set Output Voltage, Bus Address, Switching Frequency, and Current Limit
- Comprehensive PMBus Configuration, Control, and Telemetry
  - Compatible with PMBus Standard, Revision 1.3
  - 10kHz to 1MHz Bus Speed
  - PMBus Command Settings Stored in Nonvolatile Memory
  - Accurate Current, Voltage, and Temperature Reporting

***Ordering Information* appears at end of data sheet.**

19-8090; Rev 6; 5/19

Basic Application Circuit



Absolute Maximum Ratings

V_{DD} .... -0.3V to +2.2V
V_{DD3P3}, UV_IN, ENx, PGOODx, $\overline{FAULT}$, SNSPx .. -0.3V to +4V
LX to PGND .... -0.6V to V_{DD3P3} +0.6V
SDA, SCL, $\overline{ALERT}$ .... -0.3V to +6V
SNSNx .... -0.3V to +2.2V
RREF, PGMx, PWMx, TSx, CSx .... -0.3V to V_{DD} +0.3V
A1_OUTx, A2_INx, A2_OUTx, A2B_OUTx, A3_INx, A3_OUTx .... -0.3V to V_{DD} +0.3V
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Peak Reflow .... +260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 48 TQFN	
Package Code	T4877+4
Outline Number	21-0144
Land Pattern Number	90-0130
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	+25°C/W
Junction to Case (θ_{JC})	+1°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(Typical Application Circuit, unless otherwise noted, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, -40°C ≤ T_J ≤ +125°C; specifications are 100% production tested at T_A = +25°C; limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLIES (V_{DD3P3}, V_{DD})						
Supply Voltage Range	V_{DD3P3}		2.97	3.30	3.63	V
Supply Current	I_{VDD3P3}	Integrated regulator disabled		30		µA
		Integrated regulator enabled, no external load		3		mA
V_{DD3P3} Supply UVLO Rising Threshold				2.81	2.97	V
V_{DD3P3} Supply UVLO Falling Threshold			2.70	2.75		V
V_{DD} Input Voltage Range	V_{DD}		1.71	1.875	1.98	V
V_{DD} Supply Current	I_{VDD}	PWMx outputs idle 3:3		30	40	mA
		PWMx outputs idle 6:0		24	35	
V_{DD} Supply UVLO Rising Threshold				1.66	1.71	V
V_{DD} Supply UVLO Falling Threshold			1.54	1.60		V

Electrical Characteristics (continued)

(Typical Application Circuit, unless otherwise noted, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, -40°C ≤ T_J ≤ +125°C; specifications are 100% production tested at T_A = +25°C; limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTEGRATED BUCK REGULATOR (V_{DD3P3}, LX, PGND)							
Regulator Set Point		Valley voltage			1.86		V
Regulator Output Capability		L = 1µH			700		mA
Load Regulation		V_{DD3P3} = 3.3V, L = 1µH, C = 100µF, I_{LOAD} = 400mA			20		mV
Line Regulation		2.97V ≤ V_{DD3P3} ≤ 3.63V, L = 1µH, C = 100µF, I_{LOAD} = 400mA			20		mV
On-Time Per Cycle		MXIM_CORE_CONFIG[1:0] = 0		0.52	0.65	0.78	µs
		MXIM_CORE_CONFIG[1:0] = 1		1.06	1.32	1.59	
		MXIM_CORE_CONFIG[1:0] = 2 (default)		1.56	1.95	2.34	
		MXIM_CORE_CONFIG[1:0] = 3		2.24	2.80	3.36	
		Startup and output short circuit			0.65		
PULSE-WIDTH MODULATION (PWM) CONTROLLERS							
FREQUENCY_SWITCH Programmable Range (Note 1)	f_{SW}	Nominal values: 300, 350, 400, 450, 500, 600, 700, 800kHz		300		800	kHz
Switching-Frequency Tolerance		Relative to nominal values		-10		+10	%
UV_IN Rising Threshold	$V_{UV\_IN,R}$			343	355	367	mV
UV_IN Falling Threshold	$V_{UV\_IN,F}$			318	328		mV
VOUT_COMMAND Range (Note 1)		No external divider		0.500		2.000	V
VOUT_COMMAND Resolution		VOUT_MODE = 0x2C (VID)			5		mV
		VOUT_MODE = 0x16 (SLINEAR16)			0.977		mV
Output-Voltage Accuracy		0°C ≤ T_J ≤ +105°C	1.520V < V_{FB} ≤ 2.000V (Note 2)	-1.4		+1.4	%
			1.000V ≤ V_{FB} ≤ 1.520V (Note 2)	-1.1		+1.1	%
			0.250V ≤ V_{FB} < 1.000V (Note 2)	-10		+10	mV
		0.5V ≤ V_{FB} ≤ 1.0V (Note 2) T_J = +25°C		-6		+6	mV
		V_{FB} = 1.0V (Note 2) -40°C ≤ T_J ≤ +105°C		-1.1		+1.1	%

Electrical Characteristics (continued)

(Typical Application Circuit, unless otherwise noted, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, -40°C ≤ T_J ≤ +125°C; specifications are 100% production tested at T_A = +25°C; limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLIFIER A1						
Closed-Loop Differential Gain, Error-Amplifier A1	A_{V1}			2.2		V/V
Closed-Loop Bandwidth, Error-Amplifier A1				11		MHz
SNSPx Bias Current	I_{SNSP}	V_{SNSPx} = 2.5V, V_{SNSNx} = 0V	3.5	7	14	µA
		V_{SNSPx} = 1.31V, V_{SNSNx} = 0V, T_J = +25°C	-1		+1	
SNSNx Bias Current	I_{SNSN}	V_{SNSPx} = 0V, V_{SNSNx} = -0.1V	-25	-10	-5	µA
AMPLIFIER A2						
Allowable Closed-Loop Gain, Amplifier A2 (Note 1)	A_{V2}		1		4	V/V
Allowable Resistance Value, A1_OUTx to A2_INx (Note 1)			400		800	Ω
Open-Loop Gain, Amplifier A2	A_{OL2}			65		dB
Closed-Loop Bandwidth, Amplifier A2		Gain = 2		15		MHz
AMPLIFIER A2B						
Closed-Loop Gain, Amplifier A2B	A_{DM}			1		V/V
Closed-Loop Bandwidth, Amplifier A2B				16		MHz
AMPLIFIER A3						
Allowable Resistance Value A2B_OUTx to A3_INx (Note 1)	R_{DES}		165		2490	Ω
Open-Loop Gain, Amplifier A3	A_{OL3}			65		dB
Closed-Loop Bandwidth, Amplifier A3		Gain = 2		15		MHz
MODULATOR RAMP RATE						
MRAMP Tolerance		Constant mode	-11		+11	%
		V_{DDH} feed-forward mode	-13.7		+13.7	

Electrical Characteristics (continued)

(Typical Application Circuit, unless otherwise noted, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, -40°C ≤ T_J ≤ +125°C; specifications are 100% production tested at T_A = +25°C; limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERCURRENT PROTECTION						
Positive Current Limit, (V_{A3_INx} - V_{A2B_OUTx})	V_{RDES}	Inception	472.5	525	577.5	mV
		Sustaining	450	500	550	
Negative Current Limit, (V_{A3_INx} - V_{A2B_OUTx})	V_{RDES}	Inception	-214.5	-195	-175.5	mV
		Sustaining	-198	-180	-162	
OVERVOLTAGE PROTECTION						
Tracking Overvoltage Threshold		Relative to target V_{FB} (Note 2)		240		mV
Tracking Overvoltage-Fault Blanking Time		From end of V_{OUT} transition		90		µs
Umbrella Overvoltage Threshold		Absolute V_{FB} (Note 2)		2.7		V
Umbrella Overvoltage-Fault Response Time				1		µs
ENABLE INPUTS (EN1, EN2)						
Input Logic-High	$V_{EN,IH}$		1.3			V
Input Logic-Low	$V_{EN,IL}$				0.6	V
Leakage Current	I_{EN}	0V ≤ V_{ENx} ≤ V_{DD3P3}, T_J = +25°C	-5		5	µA
		V_{DD3P3} = 0V, V_{ENx} = 3.63V, T_J = +25°C	-5		5	
Deglitch Filter Time				2		µs
FAULT OUTPUT ($\overline{FAULT}$)						
Output Logic-Low		Sinking 4mA			0.3	V
Leakage Current		$V_{\overline{FAULT}}$ = 3.63V, T_J = +25°C			5	µA
POWER-GOOD OUTPUTS (PGOOD1, PGOOD2)						
Analog Power-Good Threshold	Setting 000	Falling, relative to target V_{FB} (Note 2)		-284		mV
	Setting 001			-227		
	Setting 010			-182		
	Setting 011			-148		
	Setting 100			-125		
	Settings 101, 110, 111			-102		
Analog Power-Good Hysteresis				20		mV
Output Logic-Low	$V_{PG,OL}$	Sinking 4mA			0.3	V
Leakage Current	I_{PG}	V_{PG} = 3.63V, T_J = +25°C			5	µA

Electrical Characteristics (continued)

(Typical Application Circuit, unless otherwise noted, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, -40°C ≤ T_J ≤ +125°C; specifications are 100% production tested at T_A = +25°C; limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM TIMING						
Power-Up Initialization Time	t_{READY}	From V_{DD3P3} and V_{DD} UVLO satisfied until ready for PMBus commands		6		ms
Enable Latency		TON_DELAY = 0ms		300		μs
Disable Latency		TOFF_DELAY = 0ms		4		μs
TON_DELAY, TOFF_DELAY Range (Note 1)			0		130	ms
TON_RISE, TOFF_FALL Range (Note 1)			0.25		10	ms
DIGITAL TELEMETRY						
READ_TEMPERATURE_2 Reporting Resolution				1		°C
READ_TEMPERATURE_2 Measurement Range		At TSx input	350		1350	mV
READ_TEMPERATURE_2 Accuracy		Gain error; TSx conversion	-1.5		+1.5	%
		Offset error; 1 LSB = 1.17mV at TSx	-8		+8	LSB
Current-Sense Measurement Range (V_{A3_INx} - V_{A2B_OUTx})	V_{RDES}		-180		+500	mV
READ_IOUT Accuracy		Gain error; V_{RDES} conversion	-1.5		+1.5	%
		Offset error; 1 LSB = 1.17mV at V_{RDES}	-5		+5	LSB
UV_IN Measurement Range	V_{UV_IN}		0.317		1.383	V
READ_VIN Accuracy		Gain error	-1.5		+1.5	%
		Offset error LSB = 1.17mV at UV_IN	-8		+8	LSB
Output-Voltage Measurement Range		Relative to V_{FB} set point (Note 2)	-230		+230	mV
READ_VOUT Accuracy		Output voltage within ±36mV of VOUT_COMMAND value	-1		+1	%
		Output voltage within ±230mV of VOUT_COMMAND value	-8.5		+8.5	mV

Electrical Characteristics (continued)

(Typical Application Circuit, unless otherwise noted, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, -40°C ≤ T_J ≤ +125°C; specifications are 100% production tested at T_A = +25°C; limits over the operating temperature range are guaranteed by design and characterization.)

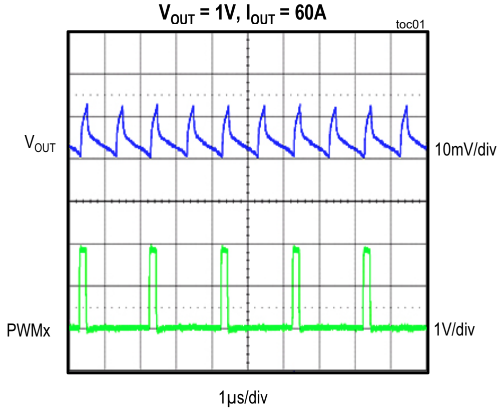
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBUS INTERFACE (SDA, SCL, $\overline{\text{ALERT}}$)						
Logic-Level Range (Pullup Voltage)	V_{PU}	Minimum		1.62		V
		Maximum		5.5		
Input Logic-High	$V_{SMBUS,IH}$		1.5			V
Input Logic-Low	$V_{SMBUS,IL}$				0.8	V
Output Logic-Low, SDA, SCL	$V_{SMBUS,OL}$	Sinking 20mA			0.4	V
Output Logic-Low, $\overline{\text{ALERT}}$	$V_{ALERT,OL}$	Sinking 4mA			0.4	V
Leakage Current	I_{SMBUS}	V_{PU} = 5.5V T_J = +25°C			5	µA
SMBus Clock Frequency Range	f_{SCL}		10		1000	kHz
Data Setup Time (Note 3)	$t_{SDA,SU}$		50			ns
Data Hold Time (Note 3)	$t_{SDA,HLD}$		0			ns
SMBus Timeout		V_{SCL} = 0V to SMBus port reset		30		ms

Note 1: Customer-programmable parameters.
Note 2: V_{FB} is the regulation voltage at the sense pins, $V_{FB} = V_{SNSPx} - V_{SNSNx}$.
Note 3: Design guaranteed by characterization. Limits are not production tested.

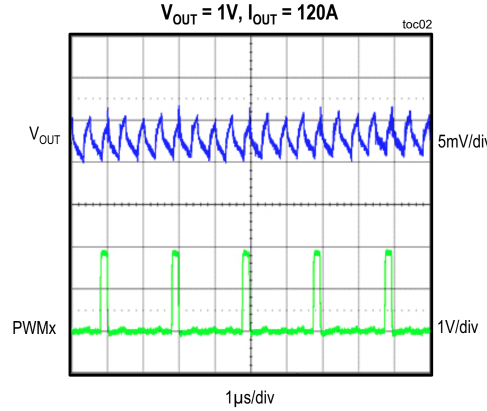
Typical Operating Characteristics

(Typical Application Circuit, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, T_J = +25°C, FREQUENCY_SWITCH = 500kHz, V_{DDH} = 12V, unless otherwise noted.)

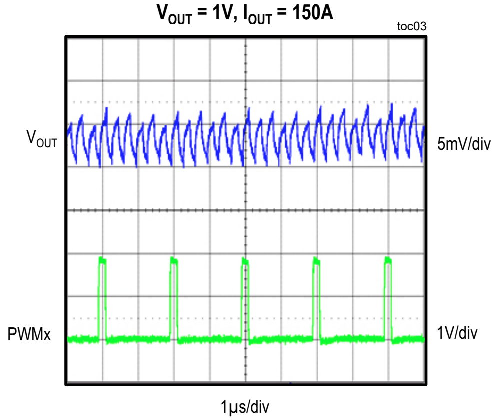
OUTPUT-VOLTAGE RIPPLE - 2 PHASE
V_{OUT} = 1V, I_{OUT} = 60A



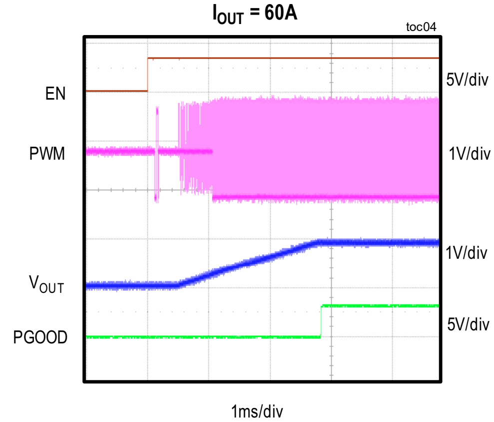
OUTPUT-VOLTAGE RIPPLE - 4 PHASE
V_{OUT} = 1V, I_{OUT} = 120A



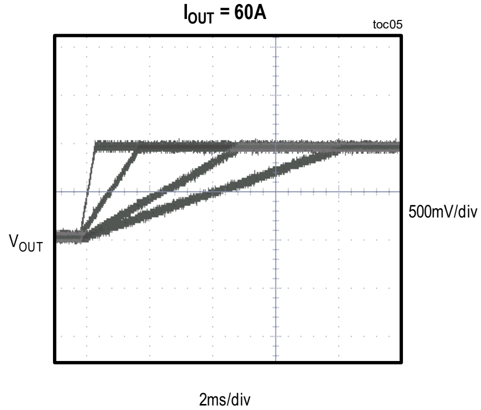
OUTPUT-VOLTAGE RIPPLE - 6 PHASE
V_{OUT} = 1V, I_{OUT} = 150A



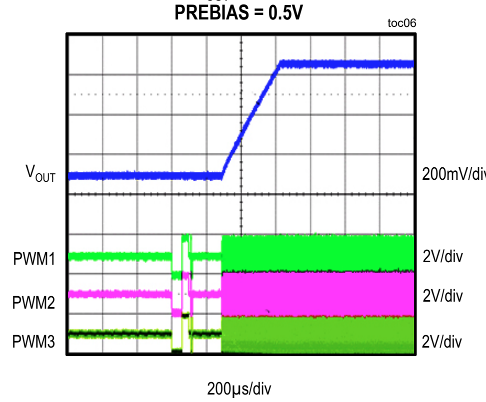
STARTUP
I_{OUT} = 60A



STARTUP
TON_RISE = 0.5ms, 2ms, 5ms, 10ms
I_{OUT} = 60A



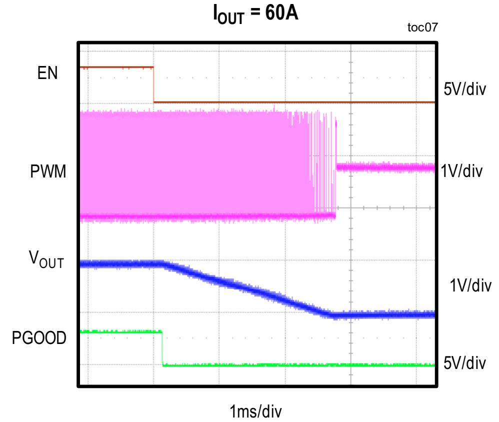
STARTUP - PREBIAS
V_{OUT} = 1.1V
PREBIAS = 0.5V



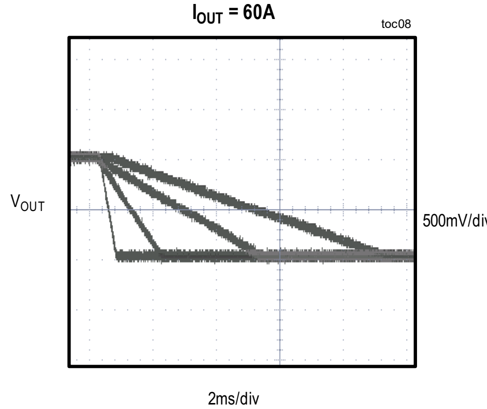
Typical Operating Characteristics (continued)

(Typical Application Circuit, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, T_J = +25°C, FREQUENCY_SWITCH = 500kHz, V_{DDH} = 12V, unless otherwise noted.)

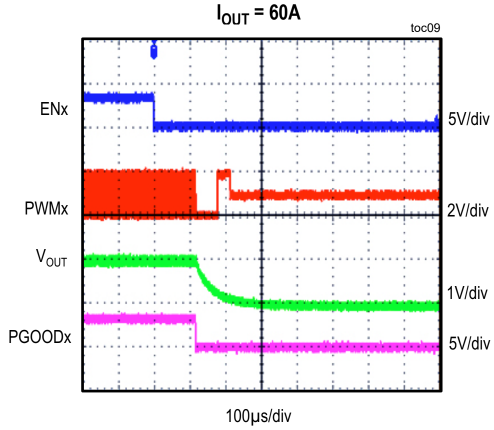
SHUTDOWN
I_{OUT} = 60A



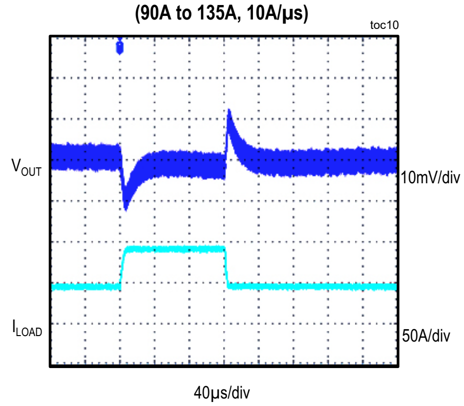
SHUTDOWN
TOFF_FALL = 0.5ms, 2ms, 5ms, 10ms
I_{OUT} = 60A



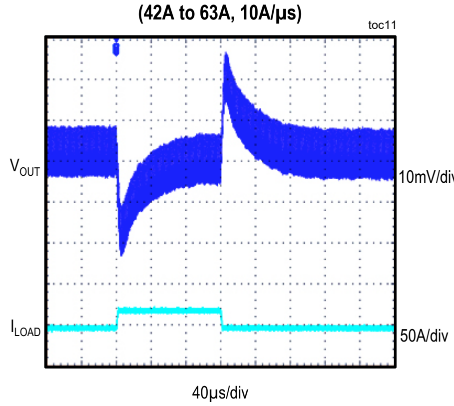
SHUTDOWN IMMEDIATE STOP
I_{OUT} = 60A



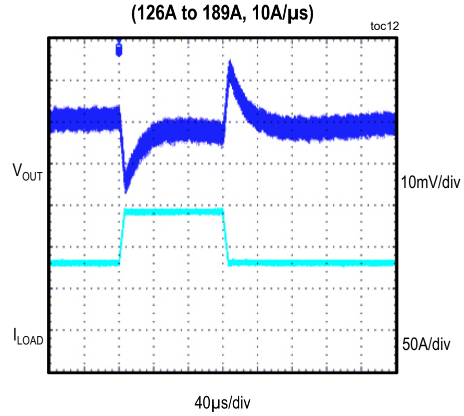
LOAD TRANSIENT - 4 PHASE
(90A to 135A, 10A/µs)



LOAD TRANSIENT - 2 PHASE
(42A to 63A, 10A/µs)

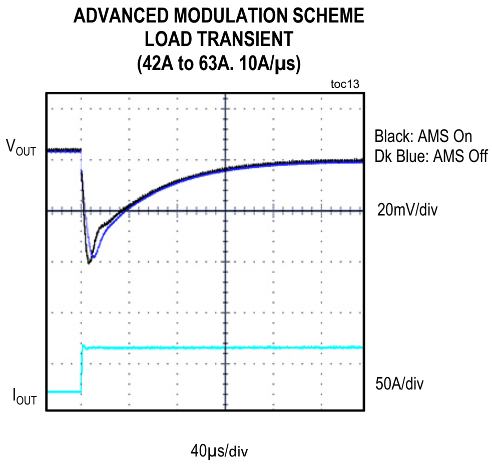


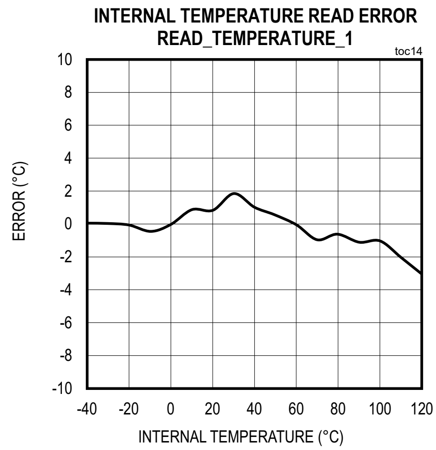
LOAD TRANSIENT - 6 PHASE
(126A to 189A, 10A/µs)

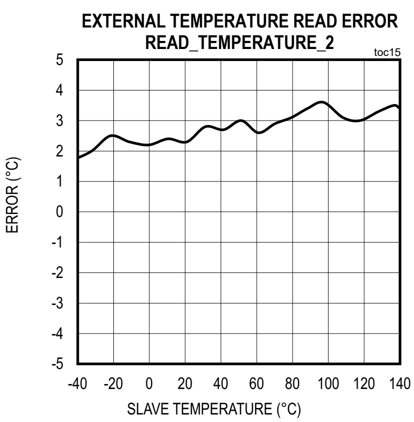


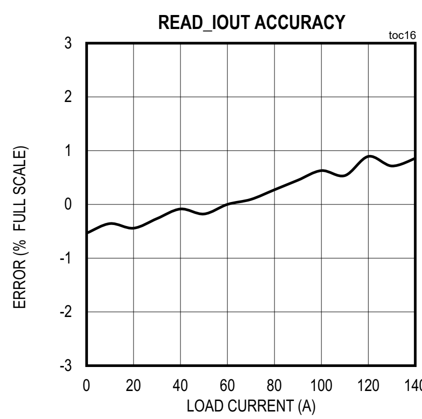
Typical Operating Characteristics (continued)

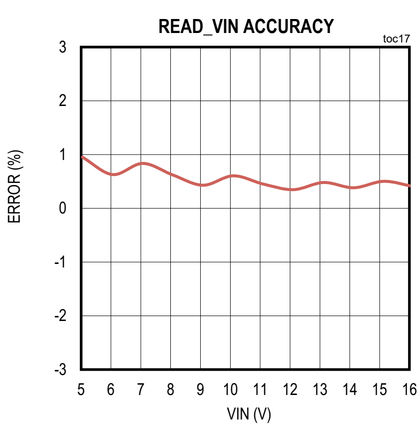
(Typical Application Circuit, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, T_J = +25°C, FREQUENCY_SWITCH = 500kHz, V_{DDH} = 12V, unless otherwise noted.)

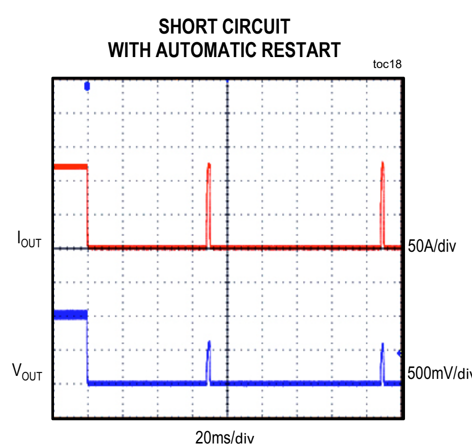








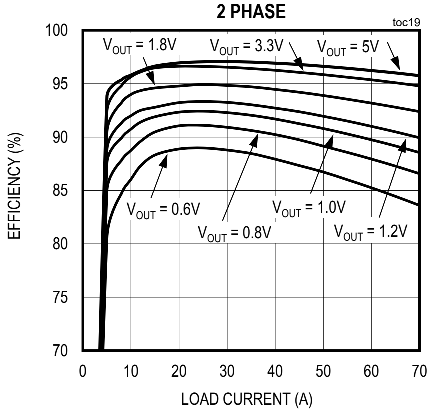




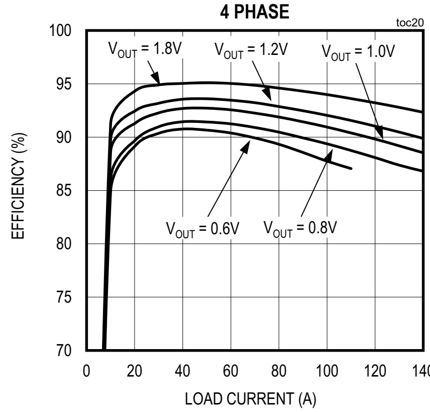
Typical Operating Characteristics (continued)

(Typical Application Circuit, V_{DD3P3} = 3.3V, V_{DD} = 1.875V, T_J = +25°C, FREQUENCY_SWITCH = 500kHz, V_{DDH} = 12V, unless otherwise noted.)

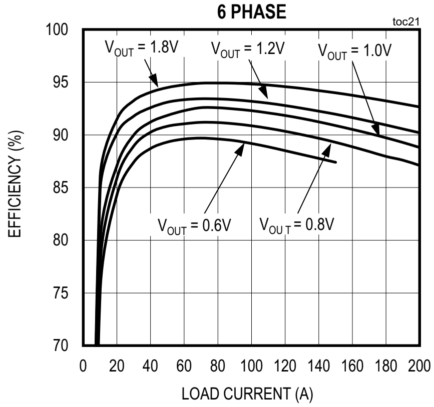
EFFICIENCY vs. LOAD CURRENT
2 PHASE



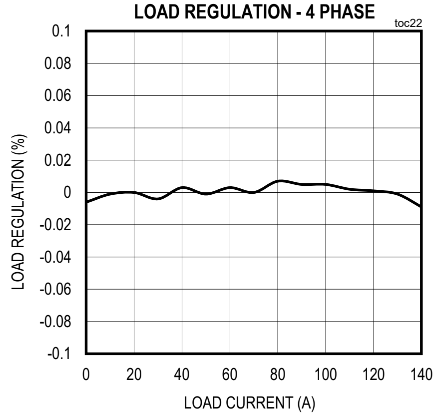
EFFICIENCY vs. LOAD CURRENT
4 PHASE



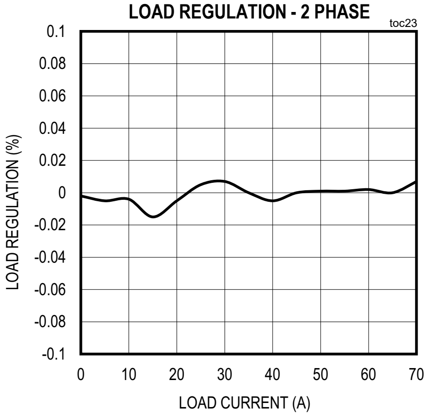
EFFICIENCY vs. LOAD CURRENT
6 PHASE



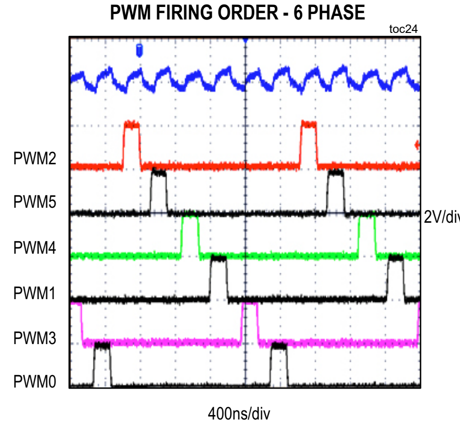
LOAD REGULATION - 4 PHASE



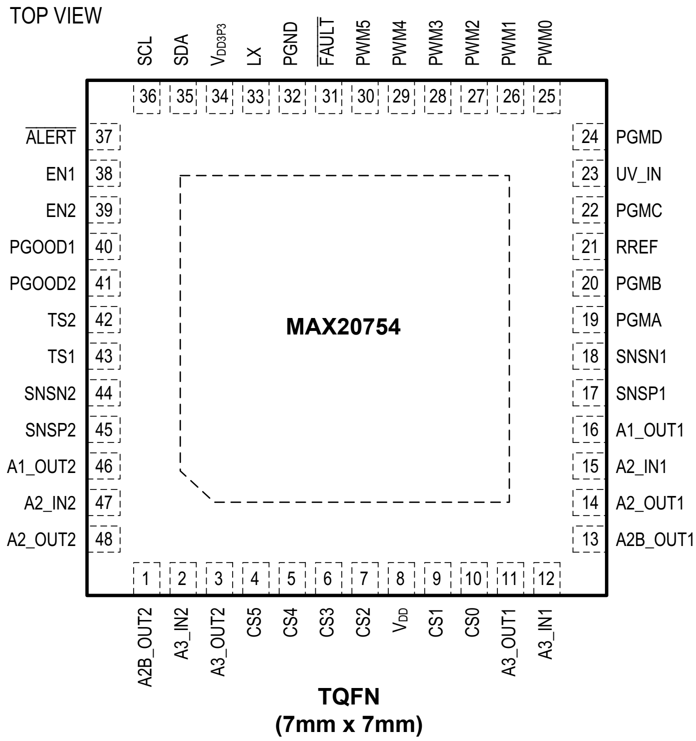
LOAD REGULATION - 2 PHASE



PWM FIRING ORDER - 6 PHASE



Pin Configuration



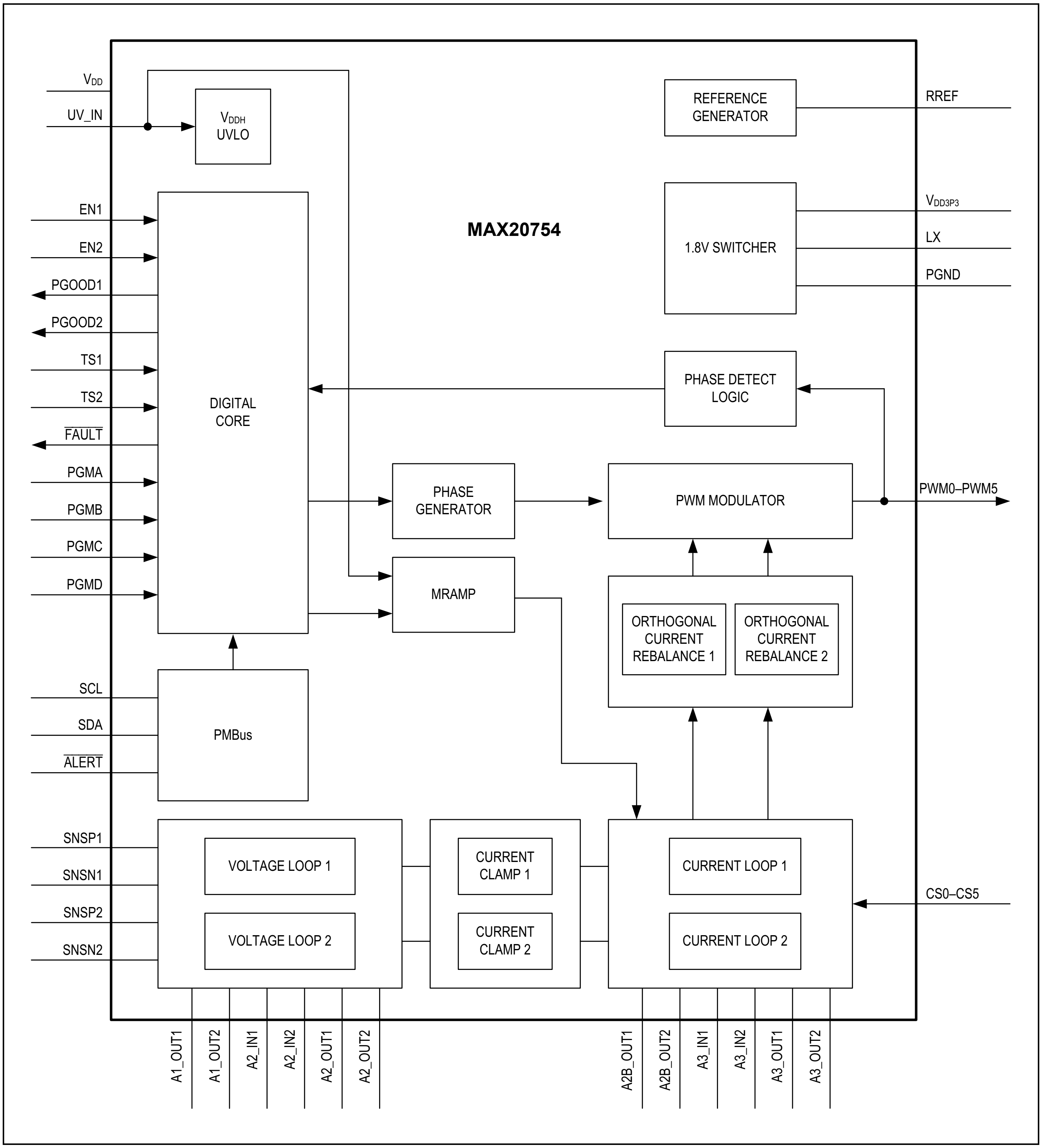
Pin Description

PIN	NAME	FUNCTION
1	A2B_OUT2	A2B Amplifier Output, Output 2
2	A3_IN2	A3 Amplifier Inverting Input, Output 2
3	A3_OUT2	A3 Amplifier Output, Output 2
4–7, 9, 10	CS5-CS0	Current-Sense Input, Phases 5–0. Connect each to the current-sense output of the corresponding power-stage device.
8	V_{DD}	Supply Voltage Connection. Connect to the output of the integrated buck regulator or an external +1.8V supply. Bypass to analog ground (EP) with a 47μF ceramic capacitor.
11	A3_OUT1	A3 Amplifier Output, Output 1
12	A3_IN1	A3 Amplifier Inverting Input, Output 1
13	A2B_OUT1	A2B Amplifier Output, Output 1
14	A2_OUT1	A2 Amplifier Output, Output 1
15	A2_IN1	A2 Amplifier Inverting Input, Output 1
16	A1_OUT1	A1 Amplifier Output, Output 1

Pin Description (continued)

PIN	NAME	FUNCTION
17	SNSP1	Positive Differential-Voltage Remote-Sense Input, Output 1. Connect to the output voltage at the load.
18	SNSN1	Negative Differential-Voltage Remote-Sense Input, Output 1. Connect to ground at the load.
19, 20, 22, 24	PGMA, PGMB, PGMC, PGMD	Configuration Input. Connect each pin to analog ground (EP) through a ±1%, 100ppm/°C resistor to set default operating values; see the *Initial Command Configuration (Resistor Pin Strapping)* section.
21	RREF	Reference Resistance Connection. Connect to analog ground (EP) through a 20.0kΩ, 0.1%, 25ppm/°C (or better) resistor.
23	UV_IN	Input-Voltage Sense. Connect to the midpoint of a resistive voltage-divider between the input voltage and analog ground (EP).
25–30	PWM0-PWM5	PWM Output, Phases 0-5. Connect each pin to the PWM input of the corresponding power-stage device. Connect to ground if unused.
31	$\overline{\text{FAULT}}$	Fault Output, Open-Drain, Active Low. Asserted low whenever a power-stage fault is detected.
32	PGND	Integrated Buck-Regulator Power Ground
33	LX	Integrated Buck-Regulator Switching Output. Connect to V_{DD} through a 1µH (typical) inductor.
34	V_{DD3P3}	Integrated Buck-Regulator Supply-Voltage Connection. Bypass to PGND with a 22µF ceramic capacitor.
35	SDA	SMBus Data Input/Output, Open-Drain
36	SCL	SMBus Clock Input/Output, Open-Drain
37	$\overline{\text{ALERT}}$	SMBus Alert Output, Open-Drain, Active Low
38, 39	EN1, EN2	Enable Input. Active high by default; configurable by PMBus command. Do not leave unconnected.
40, 41	PGOOD1, PGOOD2	Power-Good Output, Open-Drain, Active High
42, 43	TS2, TS1	Power-Stage Temperature-Sense and Fault Input. Connect to the combined power-stage temperature/fault-output pins for each output.
44	SNSN2	Negative Differential-Voltage Remote-Sense Input, Output 2. Connect to ground at the load.
45	SNSP2	Positive Differential-Voltage Remote-Sense Input, Output 2. Connect to the output voltage at the load.
46	A1_OUT2	A1 Amplifier Output, Output 2
47	A2_IN2	A2 Amplifier Inverting Input, Output 2
48	A2_OUT2	A2 Amplifier Output, Output 2
—	EP	Exposed Pad. This is the sole analog ground pin for the device. Connect the exposed pad to the analog ground plane and PGND close to the device using short, wide traces.

Functional Diagram



Detailed Description

The MAX20754 is a fixed-frequency multiphase pulse-width-modulation (PWM) buck controller utilizing a hybrid peak/average current-mode control architecture with discontinuous conduction mode (DCM) used during the startup ramp. It is suitable for high-current, single-output, or dual-output applications, with PMBus control and monitoring. The complete system comprises a dual-output controller driving up to six Maxim power-stage devices. Current- and temperature-feedback signals generated in the power stages are sent back to the controller for monitoring and protection.

The output voltage, output rise time and fall time, switching frequency, PMBus address, slope compensation, and maximum output current for both outputs are set using only five external resistors. This simple configuration method does not require use of the PMBus interface, but all parameters can be adjusted at any time by using the PMBus commands.

The controller also contains an integrated buck regulator that efficiently powers both the controller itself and all associated power stages from a 3.3V system supply voltage.

The compatible Maxim power-stage devices feature highly efficient integrated monolithic MOSFET power switches in a package with low thermal and electrical impedance. Integrated lossless current-sense technology provides accurate load-current information that is unaffected by temperature, process variation, or tolerances of external passive components. With this approach, current-sense signals are sent to the controller as currents instead of differential voltages, as would be the case with inductor direct-current resistance (DCR) or other traditional forms of series-resistance current sensing. This implementation provides superior noise immunity and eliminates resistive losses in the output-current path. The precision load-current information also provides precise load-line control (if desired), especially at light load, which is difficult with DCR-current sensing due to the low signal levels.

Theory of Operation

Figure 1 shows the control-loop architecture of the controller. There are two regulators to control two outputs. Each regulator is comprised of amplifiers and modulators that control the switching of the phases assigned to that regulator based on their individual phase current. The amplifiers and external components for one of the two regulators and one of the six PWM generators are shown In Figure 1. The PWM generators can be assigned to the regulators in various combinations, as shown in Table 2.

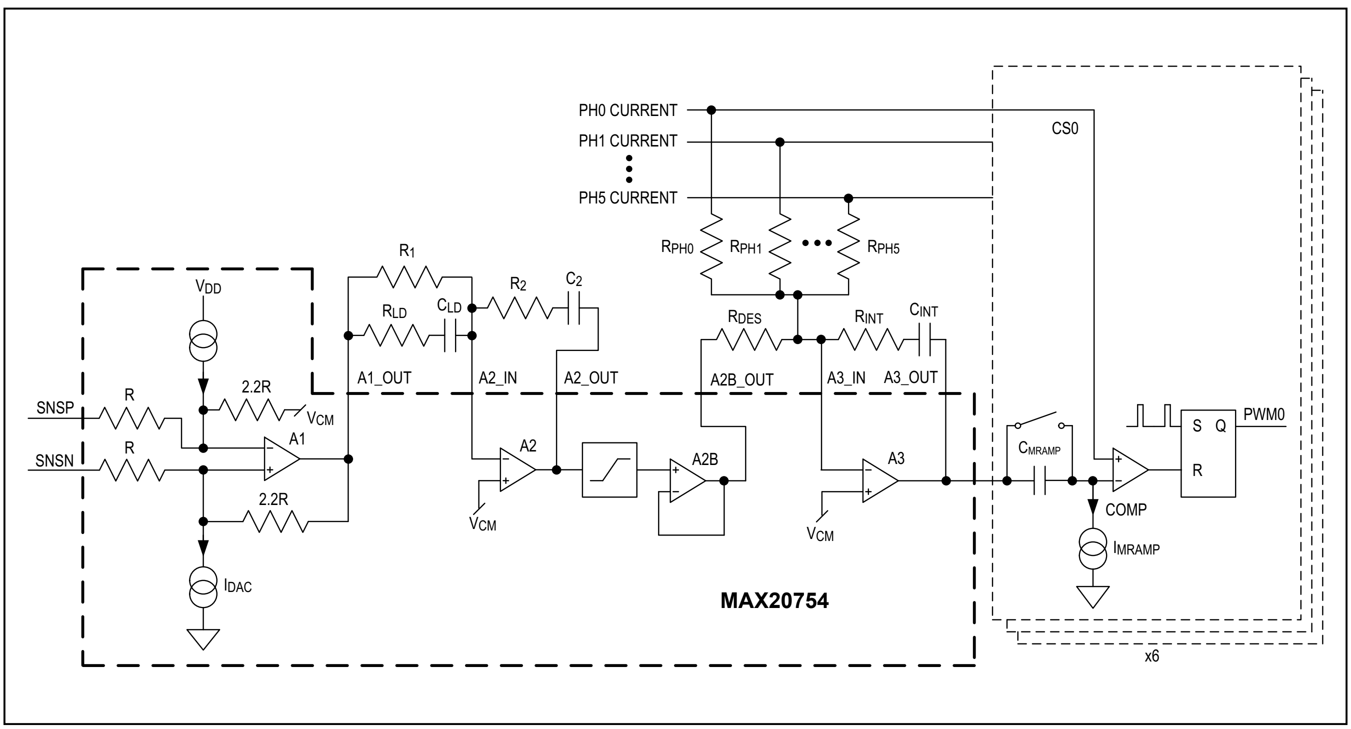


Figure 1. Control-Loop Architecture

The following applies to the operation of the regulators in general terms. The first amplifier stage A1 is a differential amplifier. Its output (A1_OUT) is the error between the reference DAC voltage and the differential voltage-sense lines, with a gain of 2.2. The differential structure of this stage provides true remote voltage sensing and high common-mode rejection to protect from any noise present at the processor ground.

Amplifier A2 then scales this error signal with gain set by resistors R_1 and R_2. Amplifier A2 provides voltage-loop compensation, and its DC gain sets the load-line of the voltage regulator.

If a non-zero load-line (output-voltage droop with load) is desired, the combination of the R_1, R_2, and R_{DES} resistors determine the effective output-resistance R_{LL} according to the equation below:

Equation 1:

$$R_{LL} = \frac{R_1 \times R_{DES}}{R_2 \times 2.2 \times K_I}$$

where K_I is the power-stage current-feedback gain (typically 10^5). Refer to the respective power-stage IC data sheet for the specific value.

Placing capacitor C_2 in series with R_2 to configure the amplifier as an integrator leads to zero load-line (no output-voltage droop under load).

The A2 amplifier is followed by a clamping circuit and buffer-amplifier A2B to provide overcurrent protection. The output of amplifier A2B is converted to a current by resistor R_{DES}; this current represents the desired total system current. This in turn sets the target for the current loop in the third amplifier (A3).

A3 acts as a current-error amplifier, as it receives the current command (through R_{DES}) and each individual sensed current from the power stages (through resistors R_{PH1}–R_{PH5}, as shown in Figure 1). Amplifier stage A3 is used in an integrating configuration. The very large low-frequency gain of the A3 stage guarantees that the total load current equals the current command in steady state.

The system has a programmable modulator ramp rate to increase stability and improve noise immunity. The ramp rate is set by the manufacturer-specific PMBus command, MRAMP. This ramp rate determines the duty-cycle modulator gain and the current-loop compensation.

With the controller's peak current-mode-control architecture, there is a system zero placed at the output LC-filter double pole. The series resistor-capacitor network of R_{INT} and C_{INT} in the feedback path of amplifier A3 establishes this system zero.

Adding series- or parallel-RC networks across the voltage-loop and current-loop amplifiers (A2 and A3, respectively) implements system loop compensation. Use a series-RC network across the R_1 resistor, as shown in Figure 1 (R_{LD} and C_{LD}), to add lead compensation for the voltage loop. Add a series resistor-capacitor network at R_2 and C_2 to increase lag compensation. Place a series resistor-capacitor network across the current-loop amplifier feedback at R_{INT} and C_{INT} for current-loop compensation. This network provides extremely high gain at low frequency, which guarantees tight current regulation.

Advanced Modulation Scheme (AMS)

The AMS in the controller is able to advance or delay the next PWM pulse after a load transient. In the event of an increase in load current, the next pulse occurs early; for a load decrease, the next pulse is delayed. This control method improves load-transient response significantly compared to a conventional PWM controller where the rising edge of the PWM pulse always occurs at a fixed interval ($1/f_{SW}$) relative to the rising edge of the previous pulse.

The AMS can be disabled by a PMBus command. This may be desirable in applications that require a strict fixed-frequency-modulation system.

Orthogonal Current-Rebalancing Circuit (OCR)

The OCR circuit ensures that load current for a given output is evenly shared between all phases. To accomplish this, the output of the A3 amplifier is modified for each individual phase. Instead of feeding the A3 output voltage directly to the PWM comparator, a control voltage (V_{Ci}) is used. The equation for V_{Ci} is shown below:

Equation 2:

$$V_{Ci} = V_{A3} - K(V_{FBi} - V_{AVG})$$

where:

- V_{FBi} = Voltage proportional to the filtered-current feedback for the phase
- V_{AVG} = Average current per phase (total current divided by phase count)
- K = OCR gain

The difference between the current of a phase from the average current (with some gain, K) is subtracted from V_{A3} to determine the control voltage V_{Ci}. If the current in any phase is greater than the average, then the V_{A3} signal is reduced and the subsequent PWM pulse for that phase is shorter, reducing the phase-current imbalance.

OCR gain K can be adjusted with the manufacturer-specific PMBus command, OCR_GAIN. The available options are shown in Table 1.

Single-Output or Dual-Output Modes and Phase Configurations

The user must select both the desired mode of operation (single output or dual output) and the number of phases per output. To configure the controller for single-output mode, connect SNSP2 to GND and connect SNSN2 to V_{DD}. Connect these remote-sense pins to the second output in the normal manner to configure for dual-output operation. Any unused PWMx-output pins and CSx-input pins must be grounded.

Table 1. Orthogonal Current-Rebalance Gain Options

OCR_GAIN COMMAND VALUE	GAIN
0	0
1	1.8
2	3.5 (default setting)
3	4.4

The controller provides flexible phase assignment in both single-output and dual-output modes. Table 2 lists the phase firing order for all valid configurations. There is no fixed-timing relationship between PWMx signals assigned to one output and those assigned to the other output.

The phase count for the second output cannot exceed that of the first output, and only certain phase assignments are valid. Configurations that are not listed explicitly in Table 2 are prohibited. Attempting to use unsupported phase assignments causes a configuration fault during the device-initialization self-test procedure, and halts operation to prevent damage.

When V_{DD} power is applied, the controller checks differential remote-sense pins (SNSP2 and SNSN2) to determine if it is in single- or dual-output mode. The controller probes the A3_IN1 pin to detect the desired phase configuration to determine which phases are connected to regulator 1. Similarly, the A3_IN2 pin is probed to determine which phases are connected to the second regulator.

Table 2. Valid Phase Configurations

PHASE CONFIGURATION (OUTPUT 1:OUTPUT 2)	PHASE SPACING (OUTPUT 1:OUTPUT 2)	OUTPUT 1 PHASES AND FIRING ORDER	OUTPUT 2 PHASES AND FIRING ORDER
6:0	60°:N/A	2, 5, 4, 1, 3, 0	None (single output)
5:0	72°:N/A	2, 4, 1, 3, 0	None (single output)
5:1	72°:360°	2, 4, 1, 3, 0	5
4:0	90°:N/A	2, 4, 1, 3	None (single output)
4:1	90°:360°	2, 4, 1, 3	5
4:2	90°:180°	2, 4, 1, 3	5, 0
3:0	120°:N/A	2, 1, 3	None (single output)
3:1	120°:360°	2, 1, 3	5
3:2	120°:180°	2, 1, 3	5, 0
3:3	120°:120°	2, 1, 3	5, 0, 4
2:0	180°:N/A	2, 1	None (single output)
2:1	180°:360°	2, 1	5
2:2	180°:180°	2, 1	5, 0
1:0	360°:N/A	2	None (single output)
1:1	360°:360°	2	5

***Note:** When using less than six phases, connect unused PWMx and CSx pins to ground. There is no fixed firing-order relationship between phases assigned to output 1 and phases assigned to output 2.*

Initialization

When V_{DD} and V_{DD3P3} are above their rising undervoltage-lockout (UVLO) thresholds, the controller begins its initialization and phase-detection procedure. First, the A3_INx pins are checked for invalid configurations. If the IC detects an invalid configuration, it sets appropriate flags in the STATUS_MFR_SPECIFIC fault register (refer to AN6257: MAX20754 PMBus Command Set User Guide for more information). If the A3 amplifier configuration is valid, the controller checks the SNSP2 and SNSN2 pins to determine if it is in single- or dual-output configuration. The controller then measures the external resistances at the PGMx pins and sets the initial command values per the applicable pin-strap tables. The SMBus slave address is set and serial communication is enabled.

Startup and Shutdown

The combination of the ENx pins and the PMBus commands (OPERATION and ON_OFF_CONFIG) enable the two outputs. Additionally, the voltage at the UV_IN pin must be above the rising-UVLO threshold before enabling the outputs. The default configuration allows the outputs to start with an active-high ENx signal, with no PMBus-command changes needed.

When all conditions are met and the output is enabled, the output voltage begins to ramp up from 0V to VOUT_COMMAND after the TON_DELAY time. The default TON_DELAY value is 0ms. The ramp time is set by TON_RISE; the default TON_RISE value is set by the pin-strap resistors. After the output voltage has reached VOUT_COMMAND, the PGOODx signal is asserted.

The combination of the ENx pins and PMBus commands OPERATION and ON_OFF_CONFIG disables the outputs. As soon as the output is disabled, the PGOODx signal clears (deasserts). Depending on the PMBus configuration, the controller output turns off immediately or with sequencing. When the output turns off with sequencing, the output continues to regulate for a delay time determined by the TOFF_DELAY command, then ramps down to 0V and stops switching. The TOFF_FALL command sets the ramp-down time; the pin-strap resistors set the default value of TOFF_FALL.

Setting the VOUT_COMMAND below 250mV disables the output voltage, also setting the VOUT_MIN warning condition.

If the V_{DD} or V_{DD3P3} supplies go below their falling UVLO thresholds, both outputs turn off and the system resets. If the voltage at the UV_IN pin goes below the falling UVLO threshold, the output is also disabled.

PMBus Interface

The MAX20754 features a serial-bus interface compatible with the PMBus Specification, Revision 1.3. The physical layer follows the SMBus specification and supports clock speeds of 10kHz to 1MHz. The controller uses and supports clock stretching. The SMBus timeout function is also supported.

The controller employs standard SMBus protocols to set output voltage, set warning and fault thresholds and their responses, read monitored data, and provide access to all manufacturer-specific commands. The protocols include Send Byte, Write Byte, Read Byte, Write Word, Read Word, Write Block, Read Block, and Block Read/Write Process Call.

The controller also supports the Group Command Protocol for the OPERATION and ON_OFF_CONFIG commands only. This protocol is used to send commands to more than one PMBus device to achieve essentially simultaneous execution of those commands. It is not required that all the devices receive the same command. However, no more than one command can be sent to any one device in one group command packet. The group command must not be used with commands that require the receiving device to respond with data. When the controller receives a command through this protocol, it begins execution of the received command only after detecting the STOP condition.

Refer to AN6257: MAX20754 PMBus Command Set User Guide for detailed descriptions of all supported PMBus commands.

Nonvolatile PMBus Memory

The controller features nonvolatile memory for storage of PMBus command values. The memory capacity is such that there are 108 possible storage “slots.” One slot can store the entire PMBus command set for a given output, so if both outputs are stored, then two slots are used. In addition, certain “shared” command data, such as PMBus inventory commands, require the use of an additional slot if they have changed since they were last stored.

The contents of the “default” and “user” stores overrides pin-strap command values where appropriate, according to the parameter loading-precedence requirements of the PMBus specification.

At any time, the number of remaining storage slots can be determined by reading the OTP_REMAINING command. Refer to AN6257: MAX20754 PMBus Command Set User Guide for more information.

Integrated Switching Regulator

The controller features an integrated switching regulator that provides power to the controller itself and to the associated power stages. This step-down regulator efficiently converts power from the V_{DD3P3} supply using a constant on-time pulse-frequency-modulation (PFM) mode of operation. The regulator's external inductor-capacitor output filter is small and inexpensive. The control scheme is voltage-mode, constant on-time with the inductor always operated in discontinuous-conduction mode (DCM), which is achieved by only allowing high-side turn-on when the inductor current reaches zero. This provides inherent current-limiting protection as well as soft-start capability.

The inductor peak current is shown below:

Equation 3:

$$I_P = \frac{V_{DD3P3} - V_{DD}}{L} \times t_{ON}$$

where:

- I_P = Inductor peak current
- V_{DD3P3} = Input voltage to the switcher
- V_{DD} = 1.87V output voltage
- L = Inductor value
- t_{ON} = Constant on-time (default setting is 1.9μs)

The maximum output current is shown below:

Equation 4:

$$I_{MAX} = \frac{V_{DD3P3} - V_{DD}}{2L} \times t_{ON}$$

If load current is higher than I_{MAX}, the V_{DD} output voltage decreases to maintain DCM operation. If V_{DD} drops below the falling UVLO threshold, the integrated regulator resets.

The on-time (t_{ON}) is programmable using the bits 1:0 of the MXIM_CORE_CONFIG command, as shown in Table 3. Before V_{DD} has risen above the undervoltage-lockout (UVLO) threshold, the on-time is set to 0.65μs. When V_{DD} has risen above the UVLO threshold, the switcher uses the programmed on-time. The default value for on-time is 1.90μs.

The inductor must be selected to support the maximum peak current without saturating because the inductor impedance determines the peak current. The highest peak current occurs during startup from zero output voltage; a 1.2μH inductor rated for 8A saturation is typically suitable.

The output-voltage peak-to-peak ripple (ΔV_{P-P}) depends on the output capacitor (C_{VDD}). The worst-case ripple occurs at light load, as shown below:

Equation 5:

$$\Delta V_{P\text{-}P} = \left(\frac{I_P}{2C_{VDD}}\right)\left(\frac{V_{DD3P3}}{V_{DD}}\right) \times t_{ON}$$

The peak-to-peak ripple should be less than 100mV. The internal switcher regulates the valley voltage, so the peak voltage is the valley voltage plus the peak-to-peak ripple voltage.

The input power from the V_{DD3P3} supply occurs in pulses of charge given by the following equation:

Equation 6:

$$Q_{VDD3P3} = \frac{I_P}{2} \times t_{ON}$$

Capacitor C_{VDD3P3} at the V_{DD3P3} pin should be chosen to supply the peak charge pulses without excessive voltage drop; three ceramic capacitors of at least 22μF each are recommended. To estimate the average V_{DD3P3} current to the integrated switching regulator, scale the output current by the inverse of the step-down ratio and assume a typical efficiency of 80% for the integrated switching regulator.

The constant on-time (t_{ON}) is programmable to accommodate a range of output currents and inductor choices. The on-time is set using the manufacturer-specific PMBus command, (MXIM_CORE_CONFIG). There are four possible settings, as shown in Table 3.

The integrated switching regulator can be disabled by removing the output inductor and connecting a 10Ω resistor from LX to V_{DD3P3}. An external 1.8V supply must then be connected to V_{DD}.

Table 3. Integrated Switcher On-Time Options

MXIM_CORE_CONFIG[1:0] VALUE	t_{ON} (μs)
0	0.65
1	1.32
2	1.95 (default setting)
3	2.80

Initial Command Configuration (Resistor Pin Strapping)

The initial values for basic operating parameters such as output voltage, switching frequency, startup rise time, and slope compensation, can be set for both outputs by appropriate selection of just four external resistors. The resistor range is from 0Ω to 10.2kΩ, divided into 32 bins, each of which is centered at a nominal E96 resistor value (standard 1% tolerance resistors), as shown in Table 4.

Table 4. Pin-Strap Resistor Bins

BIN NUMBER	NOMINAL RESISTANCE (Ω)
0	0
1	178
2	332
3	487
4	649
5	806
6	953
7	1150
8	1330
9	1540
10	1780
11	2000
12	2260
13	2490
14	2740
15	3010
16	3320
17	3650
18	4020
19	4320
20	4640
21	4990
22	5360
23	5760
24	6190
25	6650
26	7150
27	7680
28	8250
29	8870
30	9530
31	≥10200

The binned resistances at PGMA–PGMD are used as indices into lookup tables that establish the initial PMBus command values.

There are two sets of lookup tables, one for single-output operation and one for dual-output operation.

Dual-Output Pin-Strap Configuration

To select appropriate pin-strap resistor values for a dual-output configuration, identify the following parameters for both outputs:

- Switching frequency (FREQUENCY_SWITCH)
- Output voltage (VOUT_COMMAND)
- Startup and shutdown rise/fall time (TON_RISE, TOFF_FALL)
- Slope compensation (MRAMP)
- Slave addresses (from 0x50 to 0x5F in adjacent pairs)

Begin with the switching frequency for output 2, and note whether PGMD and PGMC need to be in the upper or lower halves of their resistor ranges in Table 5.

Table 5. PGMC and PGMD – Output 2 Switching Frequency Pin-Strap Options

OUTPUT 2 FREQUENCY_SWITCH, (kHz)	PGMD BIN GROUP	PGMC BIN GROUP
500	Low	Low
600	Low	High
700	High	Low
800	High	High

Next, use Table 6 and the desired voltages for output 1 and output 2 to select the appropriate value of PGMC and PGMD, respectively, being sure to use the upper or lower halves of the range for each, as determined previously.

Table 6. PGMD and PGMC – Outputs 1 and 2 Voltage Pin-Strap Options

PGMD		
BIN GROUP	OUTPUT 2 VOUT_COMMAND (V)	R (Ω)
Low	0.600	0
	0.700	178
	0.800	332
	0.900	487
	1.000	649
	1.100	806
	1.200	953
	1.300	1150
	1.400	1330
	1.500	1540
	1.600	1780
	1.700	2000
	1.800	2260
	1.900	2490
	2.000	2740
	2.000	3010
High	0.600	3320
	0.700	3650
	0.800	4020
	0.900	4320
	1.000	4640
	1.100	4990
	1.200	5360
	1.300	5760
	1.400	6190
	1.500	6650
	1.600	7150
	1.700	7680
	1.800	8250
	1.900	8870
	2.000	9530
	2.000	≥10200

PGMC		
BIN GROUP	OUTPUT 1 VOUT_COMMAND (V)	R (Ω)
Low	0.600	0
	0.650	178
	0.700	332
	0.750	487
	0.800	649
	0.850	806
	0.900	953
	0.950	1150
	1.000	1330
	1.050	1540
	1.100	1780
	1.150	2000
	1.200	2260
	1.250	2490
	1.300	2740
	1.350	3010
High	0.600	3320
	0.650	3650
	0.700	4020
	0.750	4320
	0.800	4640
	0.850	4990
	0.900	5360
	0.950	5760
	1.000	6190
	1.050	6650
	1.100	7150
	1.150	7680
	1.200	8250
	1.250	8870
	1.300	9530
	1.350	≥10200

To set the switching frequency for output 1 and the slave addresses for both outputs, use Table 7 to select an appropriate resistor for PGMA. Begin with the switching-frequency selection, and choose a suitable pair of slave addresses within the group of resistor values for the desired switching frequency.

Finally, to select the slope compensation for both outputs and the startup rise time, refer to Table 8 for the PGMB resistor value.

Begin by selecting a value for the startup rise time (TON_RISE) that is suitable for both outputs. There are two possible values, either 0.5ms or 2.5ms. Longer rise times are better suited to higher-output voltages, to minimize the inrush current during startup. The value chosen for TON_RISE is also used for TOFF_FALL by default, but can be overwritten using the PMBus commands as needed.

Choosing the TON_RISE value narrows the PGMB resistor values to one-half of the overall range. Within this range, select a value that combines the desired MRAMP settings for both outputs. There are four possible pin-strap settings for the MRAMP command: Low (LL), Medium-Low, (ML), Medium-High (MH), and High (HH). See the *Modulator Ramp Rate* section for more details. Start with output 2 and then narrow the selection further to a single value by choosing the MRAMP value for output 1.

Table 7. PGMA – Output 1 Switching Frequency and Slave Address Pin-Strap Options

PGMA			
OUTPUT 1 FREQUENCY_ SWITCH (kHz)	**OUTPUT 1 ADDRESS**	**OUTPUT 2 ADDRESS**	**R (Ω)**
500	0x50	0x51	0
	0x52	0x53	178
	0x54	0x55	332
	0x56	0x57	487
	0x58	0x59	649
	0x5A	0x5B	806
	0x5C	0x5D	953
	0x5E	0x5F	1150
600	0x50	0x51	1330
	0x52	0x53	1540
	0x54	0x55	1780
	0x56	0x57	2000
	0x58	0x59	2260
	0x5A	0x5B	2490
	0x5C	0x5D	2740
	0x5E	0x5F	3010

PGMA			
OUTPUT 1 FREQUENCY_ SWITCH (kHz)	**OUTPUT 1 ADDRESS**	**OUTPUT 2 ADDRESS**	**R (Ω)**
700	0x50	0x51	3320
	0x52	0x53	3650
	0x54	0x55	4020
	0x56	0x57	4320
	0x58	0x59	4640
	0x5A	0x5B	4990
	0x5C	0x5D	5360
	0x5E	0x5F	5760
800	0x50	0x51	6190
	0x52	0x53	6650
	0x54	0x55	7150
	0x56	0x57	7680
	0x58	0x59	8250
	0x5A	0x5B	8870
	0x5C	0x5D	9530
	0x5E	0x5F	≥10200

Table 8. PGMB – Slope Compensation and Startup Rise-Time Pin-Strap Options

PGMB			
TON_RISE, TOFF_FALL (ms)	OUTPUT 2 MRAMP	OUTPUT 1 MRAMP	R (Ω)
0.5	LL	LL	0
		ML	178
		MH	332
		HH	487
	ML	LL	649
		ML	806
		MH	953
		HH	1150
	MH	LL	1330
		ML	1540
		MH	1780
		HH	2000
	HH	LL	2260
		ML	2490
		MH	2740
		HH	3010
2.5	LL	LL	3320
		ML	3650
		MH	4020
		HH	4320
	ML	LL	4640
		ML	4990
		MH	5360
		HH	5760
	MH	LL	6190
		ML	6650
		MH	7150
		HH	7680
	HH	LL	8250
		ML	8870
		MH	9530
		HH	≥10200

Table 9. PGMC and PGMA – Single-Output Rise/Fall Time Pin-Strap Options

TON_RISE, TOFF_FALL (ms)	PGMC BIN GROUP	PGMA BIN GROUP
0.5	Low	Low
2.0	Low	High
5.0	High	Low
10.0	High	High

Single-Output Pin-Strap Configuration

To select appropriate pin-strap resistor values for a single-output configuration, identify the following operating parameters:

- Switching frequency (FREQUENCY_SWITCH)
- Output voltage (VOUT_COMMAND), to the nearest 5mV increment
- Startup and shutdown rise/fall time (TON_RISE, TOFF_FALL)
- Slope compensation (MRAMP)
- Slave address (even addresses from 0x50 to 0x6E)

Begin with the startup and shutdown rise/fall time (TON_RISE, TOFF_FALL), and note whether PGMC and PGMA need to be in the upper or lower halves of their resistor ranges according to Table 9.

Next, use Table 10 and the desired output voltage to select the appropriate value of PGMC and PGMB, respectively, being sure to use the upper or lower halves of the range for PGMC, as determined previously. Note that PGMC sets the "coarse" portion of the output voltage, in steps of 160mV, while PGMB sets the "fine" portion in steps of 5mV. The correct V_{OUT} coarse and fine values can be found quickly by determining the VID code according to the following equation:

Equation 7:

$$VID = \frac{(V_{OUT} - 0.25\,V)}{0.005\,V} + 1$$

Convert this VID code into a binary number and use the upper 4 bits to determine the V_{OUT} coarse value (PGMC resistor) and the lower 5 bits to determine the V_{OUT} fine value (PGMB resistor) according to Table 10.

Table 10. PGMC and PGMB – Single-Output-Voltage Pin-Strap Options

PGMC				PGMB		
BIN GROUP	V_{OUT} COARSE	VR12.0 VID BITS [8:5]	R (Ω)	V_{OUT} FINE	VR12.0 VID BITS [4:0]	R (Ω)
Low	0.250	0000	0	-0.005	00000	0
	0.410	0001	178	0.000	00001	178
	0.570	0010	332	0.005	00010	332
	0.730	0011	487	0.010	00011	487
	0.890	0100	649	0.015	00100	649
	1.050	0101	806	0.020	00101	806
	1.210	0110	953	0.025	00110	953
	1.370	0111	1150	0.030	00111	1150
	1.530	1000	1330	0.035	01000	1330
	1.690	1001	1540	0.040	01001	1540
	1.850	1010	1780	0.045	01010	1780
			2000	0.050	01011	2000
			2260	0.055	01100	2260
			2490	0.060	01101	2490
			2740	0.065	01110	2740
			3010	0.070	01111	3010
High	0.250	0000	3320	0.075	10000	3320
	0.410	0001	3650	0.080	10001	3650
	0.570	0010	4020	0.085	10010	4020
	0.730	0011	4320	0.090	10011	4320
	0.890	0100	4640	0.095	10100	4640
	1.050	0101	4990	0.100	10101	4990
	1.210	0110	5360	0.105	10110	5360
	1.370	0111	5760	0.110	10111	5760
	1.530	1000	6190	0.115	11000	6190
	1.690	1001	6650	0.120	11001	6650
	1.850	1010	7150	0.125	11010	7150
			7680	0.130	11011	7680
			8250	0.135	11100	8250
			8870	0.140	11101	8870
				0.145	11110	9530
			≥10200	0.150	11111	≥10200

To set the SMBus slave address, use Table 11 to select an appropriate resistor for PGMA. Remember to select from the appropriate half of the bin range, as determined previously by Table 9.

Finally, to select the slope compensation and switching frequency, refer to Table 12 for the PGMD resistor value. Begin by narrowing the resistor range by selecting the slope-compensation setting, and then select the desired switching frequency within that range.

Table 11. PGMA – Single-Output Slave Address Options

PGMA		
BIN GROUP	**ADDRESS**	**R (Ω)**
Low	0x50	0
	0x52	178
	0x54	332
	0x56	487
	0x58	649
	0x5A	806
	0x5C	953
	0x5E	1150
	0x60	1330
	0x62	1540
	0x64	1780
	0x66	2000
	0x68	2260
	0x6A	2490
	0x6C	2740
	0x6E	3010
High	0x50	3320
	0x52	3650
	0x54	4020
	0x56	4320
	0x58	4640
	0x5A	4990
	0x5C	5360
	0x5E	5760
	0x60	6190
	0x62	6650
	0x64	7150
	0x66	7680
	0x68	8250
	0x6A	8870
	0x6C	9530
	0x6E	≥10200

Table 12. PGMD – Single-Output Switching-Frequency and Slope-Compensation Options

PGMD		
MRAMP	**FREQUENCY_SWITCH (kHz)**	**R (Ω)**
LL	300	0
	350	178
	400	332
	450	487
	500	649
	600	806
	700	953
	800	1150
ML	300	1330
	350	1540
	400	1780
	450	2000
	500	2260
	600	2490
	700	2740
	800	3010
MH	300	3320
	350	3650
	400	4020
	450	4320
	500	4640
	600	4990
	700	5360
	800	5760
HH	300	6190
	350	6650
	400	7150
	450	7680
	500	8250
	600	8870
	700	9530
	800	≥10200

Table 13a. MAX20754ETMA1+ Power-Stage Device Pin-Strap Options

CREF (pF)	POWER-STAGE	GAIN (mV/°C)	0°C OFFSET (mV)	TEMPERATURE_2_ GAIN	TEMPERATURE_2_OFF-SET
0	MAX20768	3.223	894.7	0x64B8 (decimal 25784)	0xF20B (decimal -3573)
100	MAX20766	2.947	831.0	0x5C18 (decimal 23576)	0x05F0 (decimal 1520)
330	Dual power-stage	3.010	829.0	0x5E10 (decimal 24080)	0x0690 (decimal 1680)
1000	MAX20768	3.223	894.7	0x64B8 (decimal 25784)	0xF20B (decimal -3573)

Table 13b. MAX20754ETMA2+ Power-Stage Device Pin-Strap Options

CREF (pF)	POWER-STAGE	GAIN (mV/°C)	0°C OFFSET (mV)	TEMPERATURE_2_ GAIN	TEMPERATURE_2_ OFFSET
0	MAX20768	3.223	894.7	0x64B8 (decimal 25784)	0xF20B (decimal -3573)
100	MAX20766	3.010	832.0	0x5E10 (decimal 24080)	0x05A0 (decimal 1440)
330	MAX16604	3.197	810.0	0x63E8 (decimal 25576)	0x0C80 (decimal 3200)
1000	MAX20790	3.083	821.0	0x6058 (decimal 24664)	0x0910 (decimal 2320)

Power-Stage Device Selection

The controller includes a pin-strap option to allow temperature reporting for power-stage devices with different temperature signal voltage scaling. This feature sets the same value of TEMPERATURE_2_GAIN and TEMPERATURE_2_OFFSET for both outputs to match the characteristics of the selected power-stage device; this requires the use of power-stage devices with the same temperature-signal gain and offset characteristics on both outputs. This feature is used by placing a capacitor from the RREF pin to ground in parallel with the RREF resistor. See Table 13 for the capacitor pin-strap choices.

Other Maxim power-stage devices can be accommodated in any combination on both outputs by manually setting the TEMPERATURE_2_GAIN and TEMPERATURE_2_OFFSET commands to the appropriate values (refer to AN6257: MAX20754 PMBus Command Set User Guide for a full description).

Input Undervoltage Lockout Using the UV_IN Pin

The controller's UV_IN pin connects to the midpoint of a resistive voltage-divider from V_{DDH} (input power) to ground. This provides input supply undervoltage-lockout (UVLO) protection by comparing the UV_IN voltage to the internal 350mV threshold. When the UV_IN voltage exceeds the rising threshold, the system allows regulation (see the *Electrical Characteristics* table for more details).

The voltage at UV_IN is also digitized to provide the READ_VIN telemetry data. The voltage is corrected for the external divider ratio using the VIN_SCALE_MONITOR command. The default value of 0.06824 accommodates a typical resistive voltage-divider of 2.49kΩ and 34.0kΩ, which sets the input UVLO rising threshold at 5.13V. A 100pF capacitor should be connected from UV_IN to ground to filter noise.

Power-Good Outputs

The PGOODx pins are active-high, open-drain outputs that indicate whether the respective output is ready to accept loading. The PGOODx signal asserts 90μs after the conclusion of the startup ramp, and deasserts when any of the following conditions occur:

- The output voltage drops below the power-good falling threshold (relative to the nominal output voltage) for any reason
- A fault resulting in shutdown is detected
- The output is disabled

Power-Stage Fault Output

The $\overline{\text{FAULT}}$ pin is an active-low, open-drain output that pulls to ground when a power-stage fault has occurred on one or both outputs. Specifically, if the TSx pin pulls low for any reason during regulation, the controller detects a power-stage fault and asserts $\overline{\text{FAULT}}$ low. This output deasserts when the power stage successfully restarts.

Overcurrent Protection

The controller has two different overcurrent-protection systems. The first is based on digital telemetry, and is adjustable using the IOUT_OC_FAULT_LIMIT command. The second protection is based on an analog circuit that actively limits the total output current to maintain a 500mV potential across the R_{DES} resistor. This second "umbrella" limit establishes a maximum operating current, reported through the IOUT_MAX command.

Both overcurrent-protection systems have user-selectable fault responses; the controller can shut down and await user interaction, retry automatically, or ignore the fault condition and continue normal operation. The setting of the corresponding IOUT_OC_FAULT_RESPONSE command determines the system response to the telemetry-based IOUT_FAULT_LIMIT protection, while the IOUT_UMB_FAULT_RESPONSE command determines the response to the "hardware" maximum current limit (refer to AN6257: MAX20754 PMBus Command Set User Guide for more information).

Output Overvoltage Protection

The controller has three systems for output overvoltage protection. The first is based on telemetry results, with threshold and response set by the VOUT_OV_FAULT_LIMIT and VOUT_OV_FAULT_RESPONSE commands. The second system is a fast-acting analog limit at 240mV above VOUT_COMMAND, and the response to this fault is determined by the VOUT_TRK_FAULT_RESPONSE command. Finally, the third protection system is a catastrophic-failure "umbrella" fault limit at a fixed threshold of 2.7V absolute; the response to this fault is set by the VOUT_UMB_FAULT_RESPONSE command.

Application-Circuit Design Procedure

Phase Count

The typical starting point for a voltage-regulator design using the MAX20754 is the maximum-output current (IOUT_MAX). The value of IOUT_MAX is determined by the controller's hardware "umbrella" overcurrent protection. This value should be chosen to accommodate the maximum anticipated-load current with some margin; typically designing for IOUT_MAX = $I_{LOAD,MAX}$ x 120% is sufficient.

Next, determine the number of phases required to support this output current by dividing the IOUT_MAX value by the maximum safe power-stage current under the anticipated environmental conditions. The maximum power-stage current is documented in the device data sheets and design guidelines.

Switching Frequency

The controller supports eight different switching frequencies, as shown in Table 14. In dual-output applications, the upper-four supported frequencies can be set by pin-strap resistor selection. In single-output applications, any of the eight can be set by the pin-strap resistors. Sending the FREQUENCY_SWITCH command allows the use of any of the eight options regardless of the pin-strap resistor settings, for both single- and dual-output applications.

Because the MAX20754 derives the PWM fundamental frequencies by division from a fixed high-frequency clock, the resulting switching frequency varies slightly from the nominal value, depending on the number of phases assigned to a given output, as shown in Table 15.

Table 14. Switching-Frequency Options

NOMINAL SWITCHING FREQUENCY (kHz)	DUAL-OUTPUT CONFIGURATION	SINGLE-OUTPUT CONFIGURATION
300	Use FREQUENCY_SWITCH	PGMD
350	Use FREQUENCY_SWITCH	PGMD
400	Use FREQUENCY_SWITCH	PGMD
450	Use FREQUENCY_SWITCH	PGMD
500	PGMD low, PGMC low	PGMD
600	PGMD low, PGMC high	PGMD
700	PGMD high, PGMC low	PGMD
800	PGMD high, PGMC high	PGMD

Table 15. Switching Frequency vs. FREQUENCY_SWITCH and Phase Count

FREQUENCY_SWITCH (NOMINAL VALUE) (kHz)	NUMBER OF PHASES	
	1, 2, 3, 4, OR 6	5
	ACTUAL f_{SW} (kHz)	ACTUAL f_{SW} (kHz)
300	304	302
350	344	352
400	396	396
450	440	452
500	495	487
600	609	576
700	720	704
800	792	792

Maximum Output Current

When the number of phases and power-stage part numbers are determined, select the R_{DES} resistor to yield the correct IOUT_MAX value. Because R_{DES} is also used by the telemetry circuitry to measure the output current (READ_IOUT), the value of R_{DES} should be selected from Table 16.

For example, if a maximum load current of 90A is required, IOUT_MAX should be a minimum of 90A x 120% ≈ 108A. The best fit is R_{DES} = 442Ω, which yields IOUT_MAX = 113.1A.

Values of R_{DES} other than those listed in Table 16 can also be used; simply set the IOUT_CAL_GAIN command to R_{DES} x 10^{-5}, in units of mΩ. Refer to AN6257: MAX20754 PMBus Command Set User Guide for more information.

Output Capacitance

The primary factors in determining the total required output capacitance (C_{OUT}) are the maximum allowable output-voltage overshoot and undershoot (“sag” and “soar”) during load transients. In step-down converters, the voltage overshoot (ΔV_{OST}) during unloading is the dominant factor in setting the required C_{OUT} because less forcing voltage is available to reduce the inductor current.

For a maximum unloading current-step (ΔI) and maximum allowed output-voltage overshoot (ΔV_{OST}), the required output capacitance is shown in the equation below:

Equation 8:

$$C_{OUT} \geq \frac{\Delta I^2 \times \frac{L}{N}}{2 \times \Delta V_{OST} \times V_{OUT}} + \frac{\Delta I}{2\pi \times BW \times \Delta V_{OST}}$$

where:

- L = Inductance per phase
- N = Number of phases
- V_{OUT} = Nominal output voltage
- BW = Open-loop bandwidth (crossover frequency)

Selecting a higher total C_{OUT} value increases design margin against component variation and effective capacitance loss due to voltage bias.

While the capacitor equivalent-series resistance and inductance (ESR, ESL) do affect output-voltage ripple, these effects are generally not significant contributors to the overall C_{OUT} requirement when multiple large-value output capacitors are necessary, as is the case with high-current, multiphase power supplies such as the MAX20754.

Table 16. R_{DES} – Maximum Output Current Pin-Strap Options

IOUT_MAX (Amps)	NOMINAL R_{DES} (Ω)	IOUT_CAL_GAIN (mΩ)	BIN NUMBER
303.0	165	1.65	1
232.6	215	2.15	2
182.5	274	2.74	3
150.6	332	3.32	4
130.6	383	3.83	5
113.1	442	4.42	6
100.2	499	4.99	7
86.8	576	5.76	8
69.9	715	7.15	9
60.6	825	8.25	10
50.0	1000	10.0	11
40.3	1240	12.4	12
35.0	1430	14.3	13
30.3	1650	16.5	14
25.0	2000	20.0	15
20.1	2490	24.9	16

Inductor Phase-Current Ripple

For conventional inductors, the peak-to-peak phase-current ripple ($I_{PH,PP}$) is shown below:

Equation 9:

$$I_{PH,PP} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

For coupled inductors driven with (duty cycle) ≤ 1/N, the approximate inductor peak-to-peak phase-current ripple can be calculated as follows:

Equation 10:

$$I_{PH,PP} = \frac{V_{OUT}}{f_{SW} \times L}\left(\frac{1}{n_{CW}} - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

- $I_{PH,PP}$ = Peak-to-peak phase-current ripple in the inductor
- f_{SW} = Switching frequency
- L = Inductance per phase
- n_{CW} = Number of coupled windings
- V_{IN} = Input voltage
- V_{OUT} = Output voltage

The output current ripple for (duty cycle) ≤ 1/N is given by:

Equation 11:

$$I_{P\text{-}P} = \frac{V_{OUT}}{f_{SW}}\left(\frac{1}{N} - \frac{V_{OUT}}{V_{IN}}\right)\frac{N}{L}$$

where:

- $I_{P\text{-}P}$ = Peak-to-peak output current ripple
- L = Inductance per phase
- N = Number of phases

Setting the Output Load-Line Characteristic

If the A2 amplifier feedback network of R_2 and C_2 is replaced by resistor R_2 only, the controller operates with an accurate output load-line characteristic. The effective load-line resistance (R_{LL}) is set by the combination of the R_1, R_2, and R_{DES} resistors, according to the following:

Equation 12:

$$R_{LL} = \frac{R_1 R_{DES}}{R_2(2.2)K_I}$$

where:

- K_I = Power-stage current-sense gain
- R_1 = Having a typical value of 400Ω to 800Ω
- 3 ≥ R_2/R_1 ≥ 1
- If R_2/R_1 < 1, then R_1 should be between 600Ω and 800Ω, R_2 should be 353Ω (min), and the ratio of R_2/R_1 should be 0.45 (min).
- If R_2/R_1 > 1, then R_1 should be between 400Ω and 800Ω. R_2 should be 400Ω (min).

Adding capacitor C_2 in series with R_2 in the A2 stage achieves a zero load-line (no-droop) operation. It is recommended to place the zero of R_2C_2 near or lower than the resonant pole of the power stage. The value of C_2 is determined according to the following equation:

Equation 13:

$$C_2 \geq \frac{\sqrt{\frac{L}{N} C_{OUT}}}{R_2}$$

Above the corner frequency set by R_2 and C_2, the voltage-regulator impedance approaches R_{LL}.

Above the frequency (f_{ZINT}) given by the following:

Equation 14:

$$f_{ZINT} = \frac{1}{2\pi\left(R_{INT} + \frac{R_{PH}}{N}\right)C_{INT}}$$

the output impedance approaches:

Equation 15:

$$R_{LL}\left(\frac{R_{INT} + \frac{R_{PH}}{N}}{R_{INT}}\right)$$

R_{INT} Selection

For single-phase designs, set resistor R_{INT} according to:

Equation 16:

$$R_{INT} \leq \frac{0.25\,V}{\left(\frac{I_{P-P}}{K_I}\right)}$$

where:

- $I_{P\text{-}P}$ = Peak-to-peak ripple of the output current
- K_I = Power-stage current-sense gain

Note that a larger R_{INT} value provides a larger loop bandwidth for the total inductor current (see the *Voltage-Loop and Current-Loop Bandwidths* section).

Phase-Resistor Selection

All of the power-stage current-sense pins connect to the controller's A3_IN pin through individual phase-resistors (R_{PH}). The value of the phase resistors determines the voltage amplitude of the phase-current signals, which must be below 400mV for all load-current conditions, up to and including the overcurrent limit IOUT_MAX.

To help prevent phase-current imbalance due to load transients, set R_{PH} according to the following:

Equation 17:

$$R_{PH} \geq \frac{R_{INT}}{(G_{OCR} + 1)}$$

where G_{OCR} is the gain of the OCR circuit (set by the OCR_GAIN command). A phase-resistor value of approximately 500Ω is generally adequate for most applications.

The phase-current balancing circuitry keeps the average voltages across the R_{PH} resistors approximately equal. By increasing the R_{PH} resistor from the nominal value on a particular phase, the steady-state current in that phase can be reduced with respect to the other phases. This can reduce the temperature of a power-stage device that runs hotter than neighboring devices due to differences in component placement or other thermal effects. When using coupled inductors, the relative balance of phase currents is important; take care that the inductors of the other phases do not saturate.

Modulator Ramp Rate

The controller has an adjustable modulator ramp rate (S_{RAMP}) with input-voltage feed-forward characteristics. A smaller value of S_{RAMP} provides a larger loop-bandwidth for the total inductor current (see the *Voltage-Loop and Current-Loop Bandwidths* section). The correct modulator ramp rate can be determined using the switching frequency, the steady-state ramp voltage (V_{RAMPD}), and duty cycle ($D = V_{OUT}/V_{IN}$) according to the following:

Equation 18:

$$S_{RAMP} = \frac{V_{RAMPD}}{D} f_{SW}$$

V_{RAMPD} voltage typically ranges from 100mV to 300mV. An alternative method to calculate the optimal modulator ramp rate is shown below:

Equation 19:

$$S_{RAMP} = (1.5V - V_{PH,PP})\, f_{SW} / D$$

where $V_{PH,PP}$ is the peak ripple voltage at the output of amplifier A3. The approximate upper range of the amplifier output is 1.5V; the peak value $V_{PH,PP}$ must not exceed 1.5V, as shown in Figure 2. The peak-ripple voltage $V_{PH,PP}$ is found by:

Equation 20:

$$V_{PH,PP} = V_{CM} + \frac{R_{PH}}{K_I}\left(\frac{I_{MAX}}{N} + \frac{I_{PH,PP}}{2}\right)$$

where:

- V_{CM} = Common-mode voltage of amplifier A3 (specifically 850mV)
- R_{PH} = Phase resistance, typically 500Ω (Equation 13)
- I_{MAX} = Maximum output current, 500mV x (K_I/R_{DES})
- K_I = Power-stage current gain, typically 10^5
- N = Phase count (i.e., number of interleaved PWM signals)
- $I_{PH,PP}$ = Inductor ripple current in one phase (Equation 9)

Once a ramp-rate value has been determined, the correct value of the MRAMP command is calculated according to:

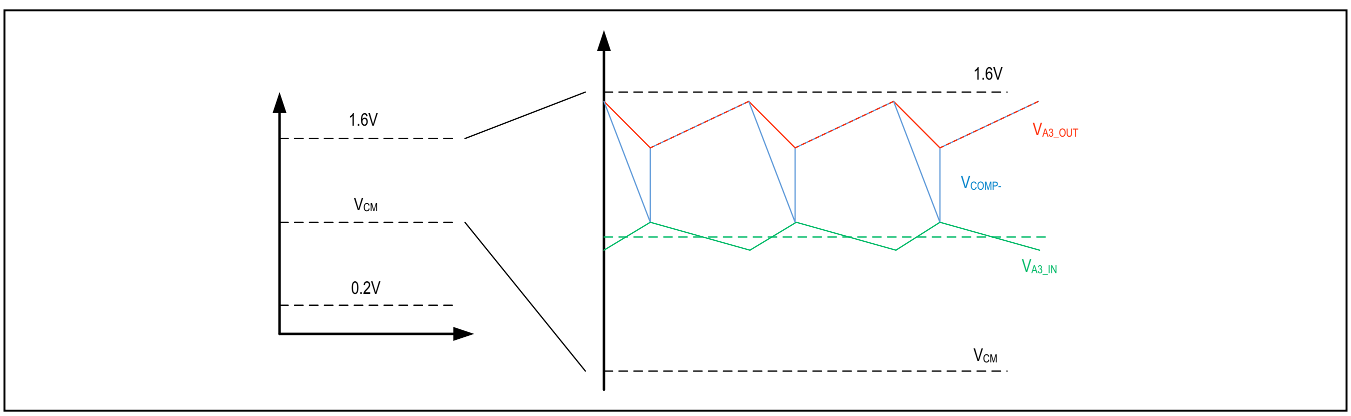


Figure 2. Modulator Ramp-Rate Illustration

Equation 21:

$$MRAMP = \left(\frac{S_{RAMP} \times 0.56\,V \times 64}{V_{UV\_IN} \times 2.46 \times 10^6}\right) - 1$$

where V_{UV_IN} is the voltage at the UV_IN pin, taking into account the external divider ratio and the anticipated input voltage range. Fore example, the voltage at the UV_IN pin is 0.82V with 12V input and a voltage-divider of 2.49kΩ and 34.0kΩ. The MRAMP command can accept decimal values from 0 to 63 (hexadecimal 0x00 to 0x3F).

The default MRAMP command value is set by resistor pin strapping; there are four starting values (see Table 17), but any value can be set using the PMBus interface.

C_{INT} Selection

C_{INT} should be selected to match the time constant of the output-filter double pole according to the following:

Equation 22:

$$C_{INT} \geq \frac{\sqrt{\frac{L}{N} C_{OUT}}}{\left(R_{INT} + \frac{R_{PH}}{N}\right)}$$

Voltage-Loop and Current-Loop Bandwidths

The voltage control-loop bandwidth (BW_V) is given by:

Equation 23:

$$BW_V = \frac{1}{2\pi R_{LL} \left(\frac{R_{INT} + \frac{R_{PH}}{N}}{R_{INT}}\right) C_{OUT}}$$

The loop bandwidth and phase margin can be increased through use of a phase-lead compensation network. The current-control loop-bandwidth BW_I for the total inductor current is given by:

Equation 24:

$$BW_I < \frac{V_{IN} \times f_{SW} \times N \left(R_{INT} + \frac{R_{PH}}{N}\right)}{S_{RAMP} \times 2\pi L \times A_I}$$

where:

- L = Inductance per phase
- A_I = Power-stage current-sense gain

The loop bandwidths should meet the conditions given by:

Equation 25:

$$BW_V < BW_I - 50kHz$$

Equation 26:

$$BW_V < \frac{f_{SW}}{3}$$

If these conditions cannot be met, additional phase margins can be added with a lead-compensation network.

Lead Compensation Network

A lead compensation network can be constructed by placing R_{LD} and C_{LD} in parallel with R1 for the amplifier of A2 when the loop dynamic response needs to be improved. It is recommended to select R_{LD} and C_{LD} so that the frequency of the zero f_{ZLD} is near or above the voltage loop bandwidth to boost phase margin, and the frequency of the pole f_{PLD} is at 2~3 times of the loop bandwidth to guarantee enough gain margin.

Equation 27:

$$f_{ZLD} = \frac{1}{2\pi C_{LD}(R_{LD} + R1)}$$

Equation 28:

$$f_{PLD} = \frac{1}{2\pi \times C_{LD} \times R_{LD}}$$

Table 17. MRAMP Pin-Strap Options

BIN NAME	MRAMP SETTING	NOMINAL dV/dt (for V_{UV_IN} = 0.82V) (V/µs)
Low (LL)	0x09 (9 decimal)	0.56
Mid-Low (ML)	0x10 (16 decimal)	0.96
Mid-High (MH)	0x25 (37 decimal)	2.14
High (HH)	0x34 (52 decimal)	2.98

PCB Layout Guidelines

For electrical and thermal reasons, the second copper layer from the top and bottom of the PCB should be reserved for contiguous ground planes. It is recommended to place the controller outside the load-current path. An analog ground copper polygon or island can be used, and the exposed pad should be connected to it, along with all analog control-signal grounds. This “quiet” analog ground polygon should extend underneath the controller and be connected to the PGND pin at one point through a single wide trace and multiple vias. The analog ground should be used as a shield and ground reference for the control signals (CSx, PWMx, SNSPx, SNSNx, and TSx).

The V_{DD} bypass capacitors should also be connected to the analog ground, and placed as close as possible to the V_{DD} pin.

The compensation components should be placed as close as possible to the controller and the amplifier inputs/outputs they connect to, away from noisy signals.

The pin-strap resistors (PGMA–PGMD and RREF) should be placed close to the controller and away from noisy signals.

Integrated Regulator Layout

Use the following guidelines for layout:

- The V_{DD3P3} supply requires a 100nF ceramic capacitor close to the pin, followed by at least a 10μF ceramic capacitor.
- Place the inductor as close as possible to the LX pin.
- A 47μF ceramic capacitor is required at the output of the inductor.
- Place a 0.5Ω resistor between the integrated switcher output and the V_{DD} pin (V_{DDS} power to the power stages).
- Place both a 100nF and a 22μF ceramic capacitor close to the V_{DD} pin.
- Use a power ground plane or polygon underneath the switcher external components and connect the PGND pin to this PGND plane.

Increasing Output Voltage Using a Feedback Divider

To set an output voltage above 2.0V, a resistive voltage-divider feedback circuit must be used. The controller regulates and monitors the voltage from SNSPx to SNSNx; therefore, all PMBus commands related to output voltage must be manually scaled by the feedback divider ratio. The VOUT_COMMAND setting should be 1.31V when the output is at the desired voltage; the equations for choosing R_1 and R_2 are thus:

Equation 29:

$$R_2 = \frac{(V_O - 1.31V)R_1}{1.31V}$$

Equation 30:

$$R_1 = 100\Omega$$

where V_O is the desired output voltage.

The resistors in the divider circuit must be sized appropriately to accommodate the power dissipation. Typically, 1/8W resistors are sufficient.

PMBus Commands

The MAX20754 features comprehensive support for PMBus commands relevant to point-of-load controllers. Full details on the individual commands and their use are included in AN6257: MAX20754 PMBus Command Set User Guide. Table 18 shows all supported commands for reference. The table indicates those commands shared between the two regulators and those that are independent for each regulator.

Table 18. Supported PMBus Commands

COMMAND CODE	COMMAND NAME	READ/WRITE/SEND	DATA BYTES	SHARED/INDEPENDENT
0x01	OPERATION	R/W	1	Independent
0x02	ON_OFF_CONFIG	R/W	1	Independent
0x03	CLEAR_FAULTS	S	0	Independent
0x10	WRITE_PROTECT	R/W	1	Independent
0x11	STORE_DEFAULT_ALL	S	0	Independent
0x12	RESTORE_DEFAULT_ALL	S	0	Independent
0x15	STORE_USER_ALL	S	0	Independent
0x16	RESTORE_USER_ALL	S	0	Independent
0x19	CAPABILITY	R	1	Shared
0x1A	QUERY	R	—	Shared
0x1B	SMBALERT_MASK	R/W	—	Independent
0x20	VOUT_MODE	R/W	1	Independent
0x21	VOUT_COMMAND	R/W	2	Independent
0x22	VOUT_TRIM	R/W	2	Independent
0x23	VOUT_CAL_OFFSET	R/W	2	Independent
0x24	VOUT_MAX	R/W	2	Independent
0x25	VOUT_MARGIN_HIGH	R/W	2	Independent
0x26	VOUT_MARGIN_LOW	R/W	2	Independent
0x27	VOUT_TRANSITION_RATE	R/W	2	Independent
0x2B	VOUT_MIN	R/W	2	Independent
0x33	FREQUENCY_SWITCH	R/W	2	Independent
0x35	VIN_ON	R	2	Shared
0x36	VIN_OFF	R	2	Shared
0x38	IOUT_CAL_GAIN	R/W	2	Independent
0x39	IOUT_CAL_OFFSET	R/W	2	Independent
0x40	VOUT_OV_FAULT_LIMIT	R/W	2	Independent
0x41	VOUT_OV_FAULT_RESPONSE	R/W	1	Independent
0x42	VOUT_OV_WARN_LIMIT	R/W	2	Independent
0x43	VOUT_UV_WARN_LIMIT	R/W	2	Independent
0x44	VOUT_UV_FAULT_LIMIT	R/W	2	Independent
0x45	VOUT_UV_FAULT_RESPONSE	R/W	1	Independent
0x46	IOUT_OC_FAULT_LIMIT	R/W	2	Independent
0x47	IOUT_OC_FAULT_RESPONSE	R/W	1	Independent
0x4A	IOUT_OC_WARN_LIMIT	R/W	2	Independent

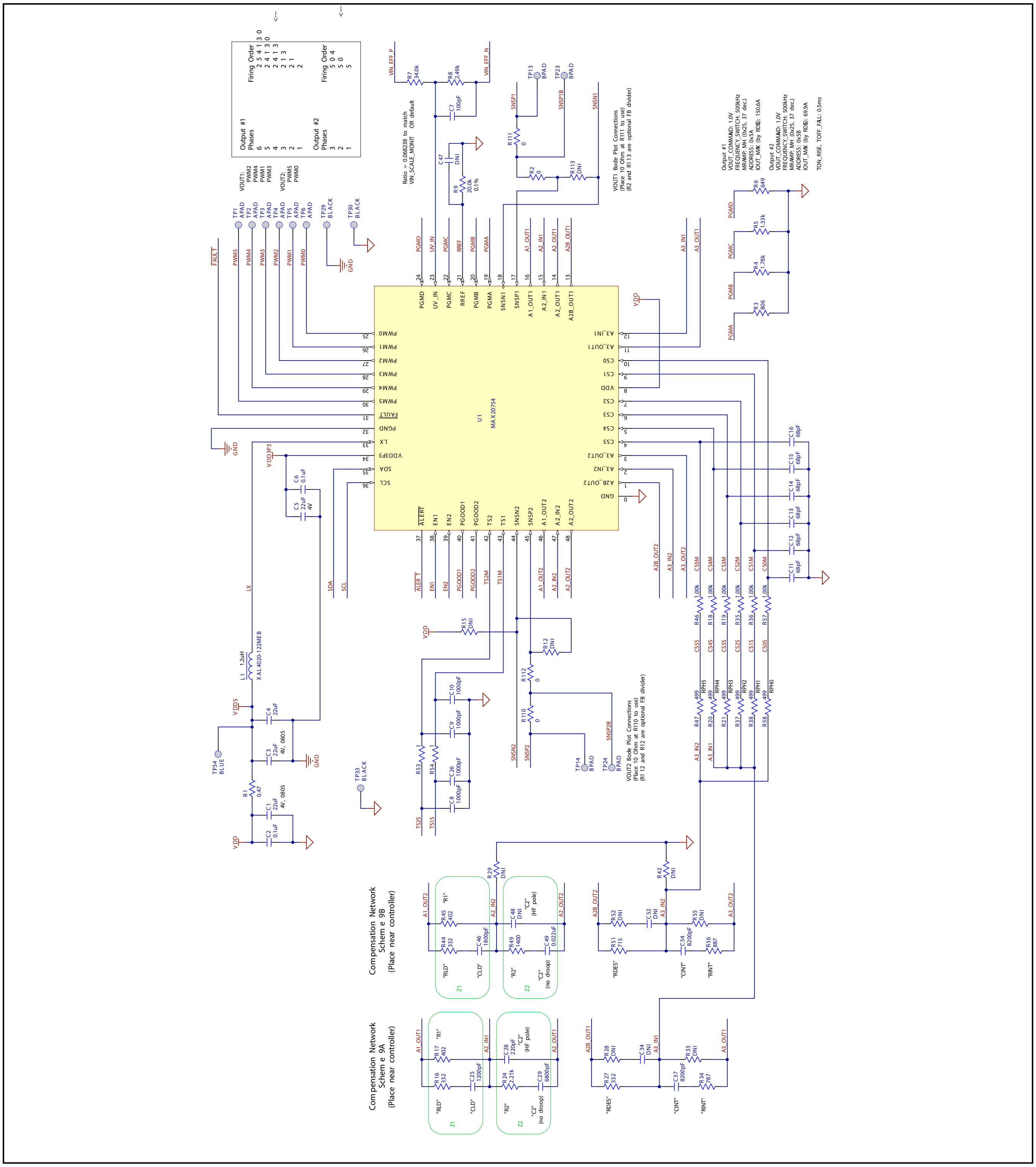
Table 18. Supported PMBus Commands (continued)

COMMAND CODE	COMMAND NAME	READ/WRITE/SEND	DATA BYTES	SHARED/INDEPENDENT
0x4F	OT_FAULT_LIMIT	R/W	2	Independent
0x50	OT_FAULT_RESPONSE	R/W	1	Independent
0x51	OT_WARN_LIMIT	R/W	2	Independent
0x52	UT_WARN_LIMIT	R/W	2	Independent
0x60	TON_DELAY	R/W	2	Independent
0x61	TON_RISE	R/W	2	Independent
0x62	TON_MAX_FAULT_LIMIT	R/W	2	Independent
0x63	TON_MAX_FAULT_RESPONSE	R/W	1	Independent
0x64	TOFF_DELAY	R/W	2	Independent
0x65	TOFF_FALL	R/W	2	Independent
0x78	STATUS_BYTE	R	1	Independent
0x79	STATUS_WORD	R	2	Independent
0x7A	STATUS_VOUT	R	1	Independent
0x7B	STATUS_IOUT	R	1	Independent
0x7C	STATUS_INPUT	R	1	Independent
0x7D	STATUS_TEMPERATURE	R	1	Independent
0x7E	STATUS_CML	R	1	Independent
0x80	STATUS_MFR_SPECIFIC	R	1	Independent
0x88	READ_VIN	R	2	Shared
0x8B	READ_VOUT	R	2	Independent
0x8C	READ_IOUT	R	2	Independent
0x8D	READ_TEMPERATURE_1	R	2	Shared
0x8E	READ_TEMPERATURE_2	R	2	Independent
0x98	PMBUS_REVISION	R	1	Shared
0x99	MFR_ID	R/W	1–24	Shared
0x9A	MFR_MODEL	R/W	1–24	Shared
0x9B	MFR_REVISION	R/W	1–24	Shared
0x9C	MFR_LOCATION	R/W	1–24	Shared
0x9D	MFR_DATE	R/W	1–24	Shared
0x9E	MFR_SERIAL	R/W	1–24	Shared
0xA4	MFR_VOUT_MIN	R/W	2	Shared
0xAD	IC_DEVICE_ID	R	6–10	Shared
0xAE	IC_DEVICE_REV	R	2	Shared
0xD1	VIN_SCALE_MONITOR	R/W	2	Shared

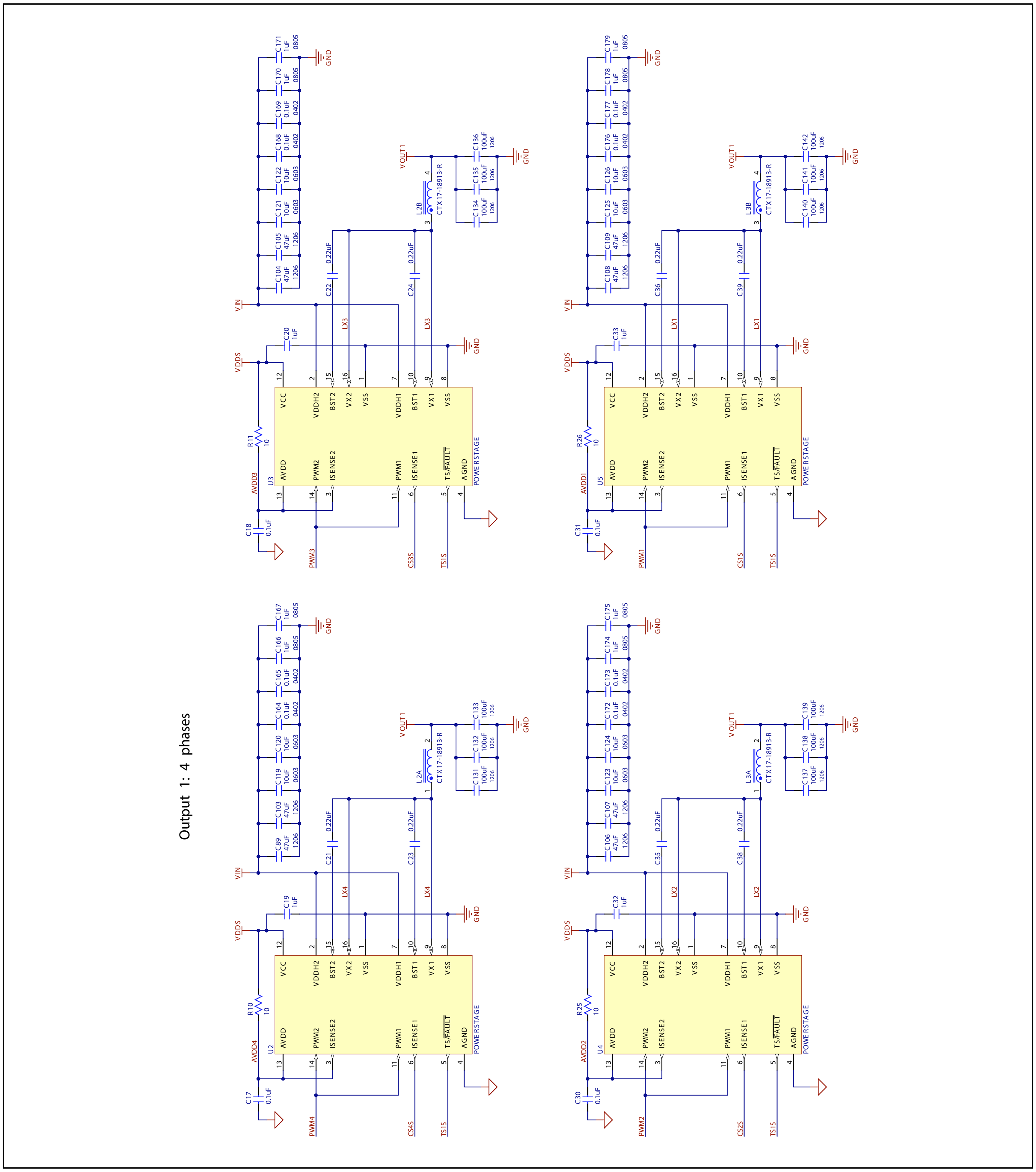
Table 18. Supported PMBus Commands (continued)

COMMAND CODE	COMMAND NAME	READ/WRITE/SEND	DATA BYTES	SHARED/INDEPENDENT
0xD4	MRAMP	R/W	2	Independent
0xD7	HARDWARE_FLAGS	R	2	Independent
0xD9	SLV_FAULT_RESPONSE	R/W	1	Independent
0xDC	STRAP_DISABLE	R/W	2	Independent
0xDD	OTP_REMAINING	R	1	Shared
0xDE	IOUT_MAX	R	2	Independent
0xDF	VOUT_TRK_FAULT_RESPONSE	R/W	1	Independent
0xE0	VOUT_UMB_FAULT_RESPONSE	R/W	1	Independent
0xE1	IOUT_UMB_FAULT_RESPONSE	R/W	1	Independent
0xE2	FAULT_LOG	R	5	Independent
0xF1	OCR_GAIN	R/W	1	Independent
0xF2	MXIM_CORE_CONFIG	R/W	1	Shared
0xF3	MXIM_RAIL_CONFIG	R/W	1	Independent
0xF8	TEMPERATURE_2_GAIN	R/W	2	Independent
0xF9	TEMPERATURE_2_OFFSET	R/W	2	Independent

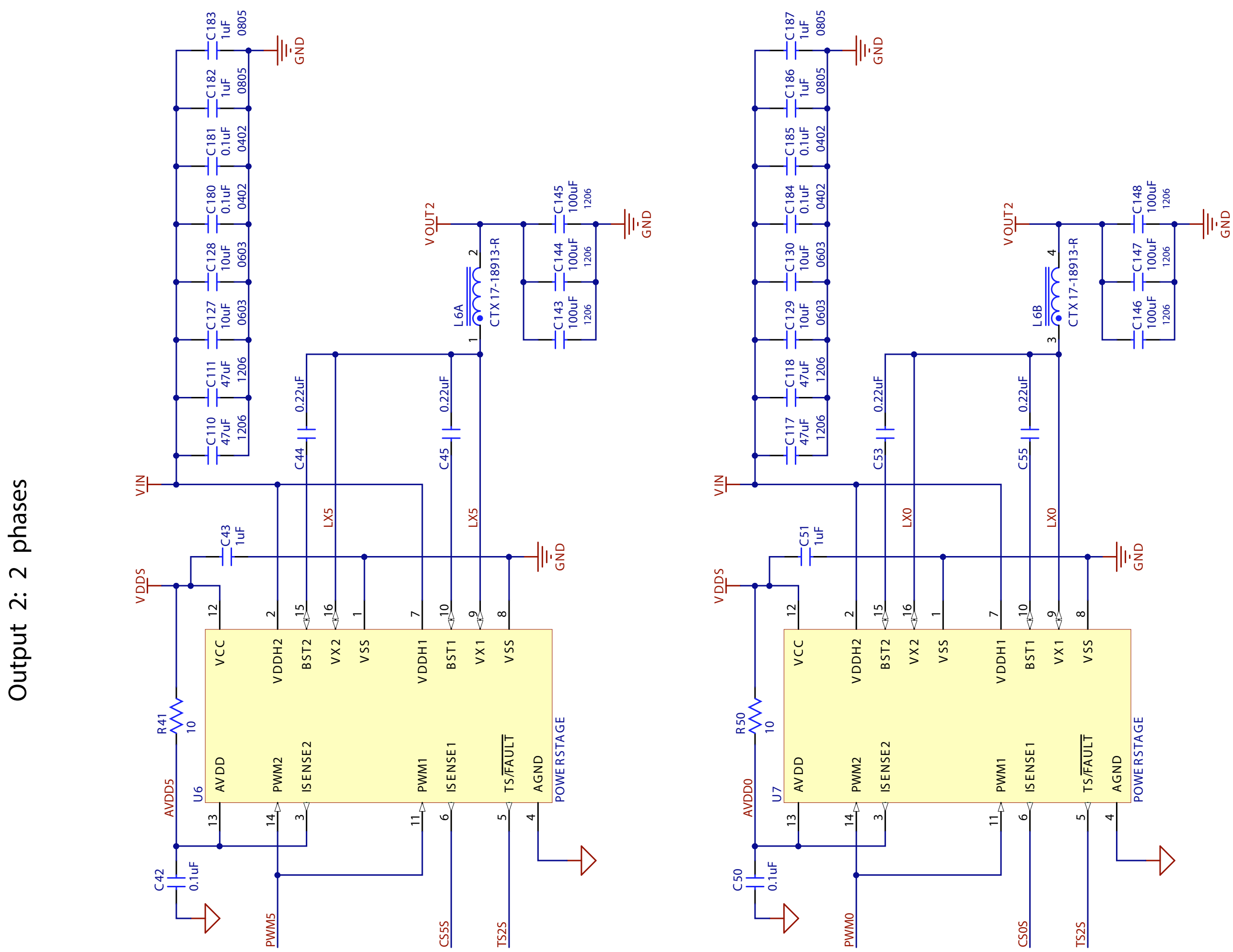
Typical Application Circuit



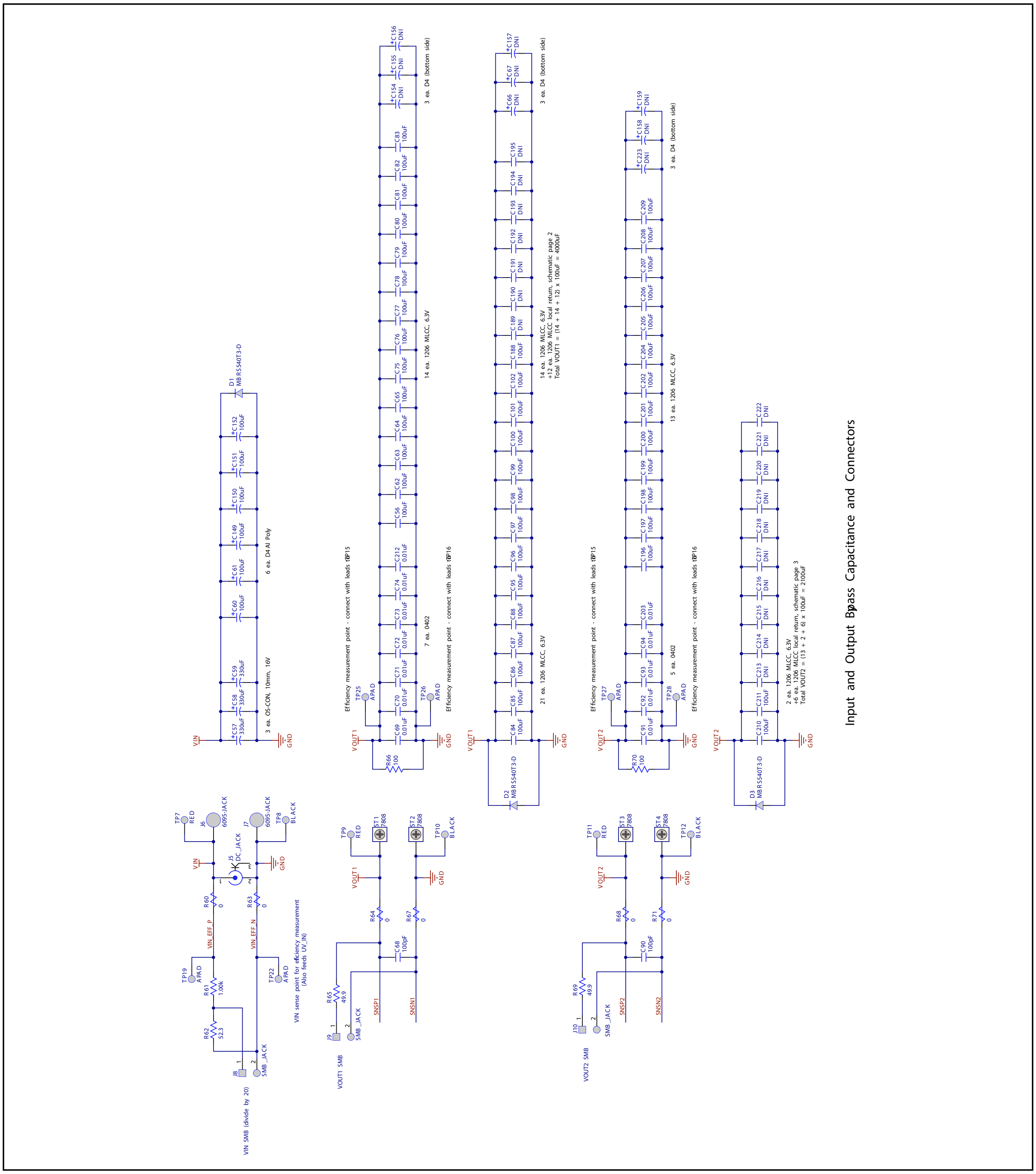
Typical Application Circuit (continued)



Typical Application Circuit (continued)



Typical Application Circuit (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION
MAX20754ETMA1+	-40°C to +125°C	48 TQFN	VOUT_MIN ≥ 0.5V (Standard Product)
MAX20754ETMA1+T	-40°C to +125°C	48 TQFN	VOUT_MIN ≥ 0.5V (Standard Product)
MAX20754ETMA2+	-40°C to +125°C	48 TQFN	VOUT_MIN ≥ 0.25V (Low-Voltage Applications)
MAX20754ETMA2+T	-40°C to +125°C	48 TQFN	VOUT_MIN ≥ 0.25V (Low-Voltage Applications)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/16	Initial release	—
1	5/17	Updated *Benefits and Features, Typical Operating Characteristics, Detailed Description, Startup and Shutdown, Integrated Switching Regulator, Maximum Output Current, Output Capacitance, Setting the Output Load-Line Characteristic, R_{INT} Selection, Modulator Ramp Rate,* and *Increasing Output Voltage Using a Feedback Divider* sections. Updated *Electrical Characteristics*, *Package Information*, and *Ordering Information* tables, and Tables 3, 6, 10, 13, 17 and 18. Updated Equation 8, 12, 16, 18, 20, and 21. Added *Lead Compensation Network* section, new Equation 27 and 28, and renumbered Equations 27–28 to 29–30	1–2, 4, 9–10, 16, 19, 20, 22, 25, 27, 29–34, 41
2	11/17	Updated Equation 19, and replaced the *Typical Application Circuit*	31, 37–40
3	12/17	Updated Equation 9	30
4	5/18	Updated the *Single-Output Pin-Strap Configuration* section, Table 12, and the *Ordering Information* table	24, 27, 41
5	6/18	Expanded Output Voltage Range to 0.25V in *Benefits and Features*. Clarified "on-chip switcher on-time" command name in *EC* Table and text. Updated Output-Voltage Accuracy in EC Table. Added "Dual power-stage" note to row 3 of Table 13. Added ≥ sign to highest value in pin-strap tables to show device behavior for "open-pin" configuration	1, 4, 13, 20-27
6	5/19	Added Table 13b to show power-stage pin-strap settings for MAX20754ETMA2+	27