

AM3352-SOM, board revision C - GPIO pinout

Double check the orientation of the connectors and the starting pin. Pin numbers 1 & 2 are printed near the plastic connector.

DOUBLE CHECK WHICH OF THE POWER PINS ARE INPUTS BEFORE PROVIDING POWER. THE SCHEMATIC OF AM3352-SOM IS AVAILABLE AND SHOULD BE USED TO VERIFY ANY SUSPICIOUS INFORMATION.

“AM3352 PIN” field has the pin names as per AM335x datasheet. For full details about a specific pin (multiplexing, usage, registers, etc) please refer to the mentioned AM335x datasheet – the ball package is ZC2. It is highly recommended to refer to source documentation released by Texas Instruments. If you are implementing additional interfaces you would also need to recompile the kernel of the default image. Instructions might be found at the wiki. The pin definitions are found in the dts file – you would need to edit it. The default file we use is am335x-olimex-som.dts and it is located in arch/arm/boot/dts/.

The processor AM3352 has a lot of multiplexing pins! Make sure to use the “Pin Mux Utility” tool provided by Texas Instruments to determine what are the pins of each interface and which ball goes.

Signals with (NC) in the name are routed to the corresponding processor pin but are disconnected by default.

“AM3352 BALL” marked with “-” indicate that the signal is related to the power supply circuit. Such signals are not directly connected to the microcontroller and you should be careful when operating those signals. Improper use might lead to short-circuits.

The field “MULTIPLEXING” refers only to the design of AM3352-SOM; there might be multiplexing on the corresponding pin in design of the board of peripherals (AM3352-SOM-EVB).

AM_CON-LCD										
MULTIPLEXING	FUNCTION (S)	AM3352 BALL	SIGNAL # NAME	#		#	SIGNAL # NAME	AM3352 BALL	FUNCTION (S)	MULTIPLEXING
-	POWER INPUT	-	+5V	1	o	2	GND	-	POWER GROUND	-
-	POWER OUTPUT	-	3.3V	3	o	4	GND	-	POWER GROUND	-
NO	LCD DATA	T11	P0_26/LCD_D21	5	o	6	P1_13/LCD_D18	R12	LCD DATA	NO
NO	LCD DATA	U13	P1_15/LCD_D16	7	o	8	P2_6/LCD_D0	R1	LCD DATA	INITIAL BOOT
INITIAL BOOT	LCD DATA	R2	P2_7/LCD_D1	9	o	10	P2_8/LCD_D2	R3	LCD DATA	INITIAL BOOT
INITIAL BOOT	LCD DATA	R4	P2_9/LCD_D3	11	o	12	P2_10/LCD_D4	T1	LCD DATA	INITIAL BOOT
NO	LCD DATA	T10	P0_23/LCD_D22	13	o	14	P1_12/LCD_D19	T12	LCD DATA	NO
INITIAL BOOT	LCD DATA	T2	P2_11/LCD_D5	15	o	16	P2_12/LCD_D6	T3	LCD DATA	INITIAL BOOT
INITIAL BOOT	LCD DATA	T4	P2_13/LCD_D7	17	o	18	P2_14/LCD_D8	U1	LCD DATA	INITIAL BOOT
INITIAL BOOT	LCD DATA	U2	P2_15/LCD_D9	19	o	20	P2_16/LCD_D10	U3	LCD DATA	INITIAL BOOT
NO	LCD DATA	U10	P0_22/LCD_D23	21	o	22	P0_27/LCD_D20	U12	LCD DATA	NO
NO	LCD DATA	V13	P1_14/LCD_D17	23	o	24	P2_17/LCD_D11	U4	LCD DATA	INITIAL BOOT
INITIAL BOOT	LCD DATA	V2	P0_8/LCD_D12	25	o	26	P0_9/LCD_D13	V3	LCD DATA	INITIAL BOOT
INITIAL BOOT	LCD DATA	V4	P0_10/LCD_D14	27	o	28	P0_11/LCD_D15	T5	LCD DATA	INITIAL BOOT
NO	LCD HSYNC	R5	P2_23/LCD_HSYNC	29	o	30	P2_22/LCD_VSYNC	U5	LCD VSYNC	NO
NO	LCD CLOCK	V5	P2_24/LCD_CLK	31	o	32	P2_25/LCD_DE	R6	LCD DATA ENABLE	NO
NO	NOT CONNECTED	-	NC*	33	o	34	NC*	-	NOT CONNECTED	NO
NO	LCD POWER ENABLE	C13	P3_19/LCD_PWR_EN	35	o	36	P0_7/PWM0_OUT**	C18	LCD BACKLIGHT	NO
NO	TOUCHSCREEN	Y22	TPX1	37	o	38	TPX2	AA22	TOUCHSCREEN	NO
NO	TOUCHSCREEN	Y23	TPY1	39	o	40	TPY2	AA23	TOUCHSCREEN	NO

*PINS 33 AND 34 DO NOT REACH THE PROCESSOR DUE TO THE MISSING RESISTORS R29 AND R32. THE VALUES OF THESE PINS CAN BE USED TO CHANGE THE SCANNING MODE (ORIENTATION) OF THE OLIMEX DISPLAYS DYNAMICALLY. THE DEFAULT SCANNING MODE IS “UP TO DOWN, RIGHT TOLEFT”. REFER TO THE DISPLAY DATASHEET FOR POSSIBLE VALUES. REFER TO THE DISPLAY SCHEMATIC TO FURTHER TRACE THE LCD SIGNALS (THEY CAN BE FOUND ON GPIO1 PINS 2-15 AND 2-24).

**PIN 36 PROVIDES OPTION ON WHICH SIGNAL WOULD DRIVE THE BACKLIGHT. BY DEFAULT PWM0_OUT IS CHOSEN. THE OTHER TWO OPTIONS PROVIDED ARE P1_18/EHRPWM1A/TXD3 AND P3_15/SP11_D0(MISO). YOU WOULD NEED TO REMOVE R38 AND PLACE IT ON THE PADS OF EITHER R36 OR R37. PLACING R36 WOULD ENABLE P1_18/EHRPWM1A/TXD3. PLACING R37 WOULD ENABLE P3_15/SP11_D0(MISO). WARNING! RE-CONFIGURATION MIGHT BRICK YOUR DEVICE! IT IS NEITHER NEEDED FOR TYPICAL OPERATION NOR RECOMMENDED.

**LCD DATA PINS #0 TO #15 ARE USED DURING INITIAL BOOT TO SET THE SYSTEM BOOT CONFIGURATION. THE DEFAULT BOOT PRIORITY SET BY LCD DATA PINS IS USB0->NAND->SPI0->MMC0. REFER TO THE AM3352 DOCUMENTATION FOR MORE INFORMATION ABOUT THE SYSTEM BOOT CONFIGURATION.

ONLY NOTABLE FUNCTIONS ARE MENTIONED. FOR FULL LIST OF FUNCTIONS AND PIN MULTIPLEXING - REFER TO THE PROCESSOR'S DATASHEET.

AM_CON-GPIO1										
MULTIPLEXING	FUNCTION (S)	AM3352 BALL	SIGNAL # NAME	#		#	SIGNAL # NAME	AM3352 BALL	FUNCTION (S)	MULTIPLEXING
-	POWER INPUT	-	+5V	1	o	2	GND	-	POWER GROUND	-
-	POWER OUTPUT	-	3.3V	3	o	4	GND	-	POWER GROUND	-
YES, UART DEBUG	UART0_RX	E15	P1_10/UART0_RX	5	o	6	P1_31/NDQ5	V9		NO
YES, UART DEBUG	UART0_TX	E16	P1_11/UART0_TX	7	o	8	P1_7/NDQ7	T9	NAND CONTROLLER	YES, NAND PADS
YES, NAND PADS	NAND CONTROLLER	U6	P2_4/NWE	9	o	10	P1_6/NDQ6	R9	NAND CONTROLLER	YES, NAND PADS
YES, NAND PADS	NAND CONTROLLER	R7	P2_2/NALE	11	o	12	P1_5/NDQ5	V8	NAND CONTROLLER	YES, NAND PADS
YES, NAND PADS	NAND CONTROLLER	T6	P2_5/NCLE	13	o	14	P1_4/NDQ4	U8	NAND CONTROLLER	YES, NAND PADS
NO	NAND; LCD UP/DOWN DIRECTION	U9	P1_30/NCE1/LCD_U/D	15	o	16	P1_3/NDQ3	T8	NAND CONTROLLER	YES, NAND PADS
YES, NAND PADS	NAND CONTROLLER	V6	P1_29/NCE0	17	o	18	P1_2/NDQ2	R8	NAND CONTROLLER	YES, NAND PADS
YES, NAND PADS	NAND CONTROLLER	T7	P2_3/NRE	19	o	20	P1_1/NDQ1	V7	NAND CONTROLLER	YES, NAND PADS
YES, NAND PADS	NAND CONTROLLER	T17	P0_30/NRB0/CRS	21	o	22	P1_0/NDQ0	U7	NAND CONTROLLER	YES, NAND PADS
NO		U18	P1_28/ECOL	23	o	24	SYS_RESETN	A10	RESET LINE	YES, GPIO2 AND GPIO3
NO		A15	P0_19/EMU2	25	o	26	P2_0/LCD_L/R	T13	NO; LCD LEFT/RIGHT DIRECTION	NO
NO		V17	P1_27/RXD0	27	o	28	P2_1/NRB1	V12	NAND CONTROLLER	YES, NAND PADS
NO		U16	P1_25/RXD2	29	o	30	P1_16/TXEN	R13		NO
NO		T16	P1_26/RXD1	31	o	32	P0_31/NWP/RXERR	U17	NAND CONTROLLER	YES, NAND PADS
NO		V16	P1_24/RXD3	33	o	34	P1_20/TXD1	R14		NO
NO		T15	P1_23/RXCLK	35	o	36	P1_19/TXD2	T14		NO
NO		U15	P1_22/TXCLK	37	o	38	P1_18/EHRPWM1A/TXD3	U14		NO
NO		V15	P1_21/TXD0	39	o	40	P1_17/RXDV	V14		NO

AM3352-SOM DOESN'T HAVE NAND FLASH PLACED BY DEFAULT; IT IS SAFE TO CONSIDER ALL PINS MULTIPLEXED WITH THE NAND FLASH PADS FREE UNTIL YOU HAVE PLACED NAND FLASH MEMORY.

AM_CON-GPIO2										
MULTIPLEXING	FUNCTION (S)	AM3352 BALL	SIGNAL # NAME	#		#	SIGNAL # NAME	AM3352 BALL	FUNCTION (S)	MULTIPLEXING
-	POWER INPUT	-	+5V	1	o	2	GND	-	POWER GROUND	-
-	POWER OUTPUT	-	3.3V	3	o	4	GND	-	POWER GROUND	-
NO		T18	USB1-VBUS	5	o	6	USB1_ID	P17		NO
NO		R17	USB1_DP	7	o	8	USB1_CE	P18		NO
NO		R18	USB1_DM	9	o	10	USB1_DRV	F15		NO
NO		P15	USB0-VBUS	11	o	12	USB0-ID	P16		NO
NO		N17	USB0_DP	13	o	14	USB0_CE	M15		NO
NO		N18	USB0_DM	15	o	16	USB0_DRV	F16		NO
NO		C15	MMC0-SDCD#/EMU4	17	o	18	PMIC_POWER_EN	C6		NO
NO		B15	PMRONRSTN	19	o	20	EXT_WAKEUP	C5		NO
GPIO1 and GPIO3		A10	SYS_RESETN	21	o	22	NNMI	B18		NO
NO		K17	P0_28/ETXD0	23	o	24	P2_21/ERXD0	M16		NO
NO		K16	P0_21/ETXD1	25	o	26	P2_20/ERXD1	L15		NO
NO		K15	P0_17/ETXD2	27	o	28	P2_19/ERXD2	L16		NO
NO		J18	P0_16/ETXD3	29	o	30	P2_18/ERXD3	L17		NO
NO		J16	P3_3/ETXEN	31	o	32	P3_4/ERXDV	J17		NO
NO		K18	P3_9/ETXCK	33	o	34	P3_10/ERXCK	L18		NO
NO		J15	P3_2/ERXERR	35	o	36	P0_1/EMDC	M18		NO
NO		H16	P3_0/ECOL	37	o	38	P0_0/EMDIO	M17		NO
NO		H17	P3_1/ECRS	39	o	40	P0_29/EPHY-RST#/RFCLK	H18		NO

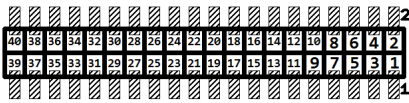
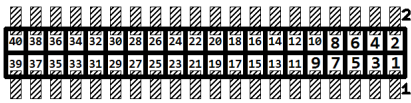
AM_CON-GPIO3

MULTIPLEXING	FUNCTION (S)	AM3352 BALL	SIGNAL # NAME	#	#	SIGNAL # NAME	AM3352 BALL	FUNCTION (S)	MULTIPLEXING
-	POWER INPUT	-	+5V	1	2	GND	-	POWER GROUND	-
-	POWER OUTPUT	-	3.3V	3	4	GND	-	POWER GROUND	-
NO	UART1 TX	D15	P0_15/UART1_TXD	5	6	P0_14/UART1_RXD	D16	UART1 RX	NO
NO	I2C #2	D17	P0_13/I2C2_SCL	7	8	P0_12/I2C2_SDA	D18	I2C #2	NO
NO	SPI0	B17	P0_3/SPI0_D0(MISO)	9	10	P0_4/SPI0_D1(MOSI)	B16	SPI0	NO
NO	SPI0	A17	P0_2/SPI0_SCLK	11	12	P0_5/SPI0_CS0	A16	SPI0	NO
NO	UART4 TX	E17	P1_9/UART4_TXD	13	14	P1_8/UART4_RXD	E18	UART4 RX	NO
NO	I2C #0	C16	P3_6/I2C0-SCL	15	16	P3_5/I2C0-SDA	C17	I2C #0	NO
NO	SPI1	B13	P3_15/SPI1_D0(MISO)	17	18	P3_16/SPI1_D1(MOSI)	D12	SPI1	NO
NO	SPI1	A13	P3_14/SPI1_CLK	19	20	P3_17/SPI1_CS0	C12	SPI1	NO
NO		B12	P3_18/LED1	21	22	P0_20/EMU3	D14		NO
NO		D13	P3_20/LED2	23	24	P3_21/LED3	A14		NO
NO		C14	P3_7/EMU0	25	26	P3_8/EMU1	B14		NO
NO		C18	P0_7/PWM0_OUT	27	28	SYS_RESETN	A10		YES; GPIO1 AND GPIO2
NO	JTAG	A12	JTAG_TCK	29	30	JTAG_TRST	B10	JTAG	NO
NO	JTAG	B11	JTAG_TDI	31	32	JTAG_TMS	C11	JTAG	NO
NO	JTAG	A11	JTAG_TDO	33	34	VREFP	B9	ADC POSITIVE REFERENCE	NO
NO	ADC I/O	C8	AIN4	35	36	AIN7	C9	ADC	NO
NO	ADC OUTPUT	B8	AIN5	37	38	AIN6	A8	ADC	NO
NO		D8	VDDA_ADC	39	40	GNDA	-	POWER GROUND	-

UART DEBUG

MULTIPLEXING	FUNCTION (S)	AM3352 BALL	SIGNAL # NAME	#
YES, GPIO1	UART0 TX	E16	P1_11/UART0_TX	1
YES, GPIO1	UART0 RX	E15	P1_10/UART0_RX	2
-	POWER GROUND	-	GND	3
-	POWER GROUND	-	GND	4
-	POWER OUTPUT	-	+5V	5

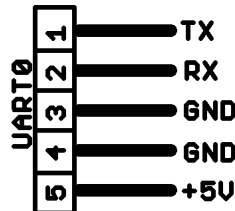
POWER	+5V PINS ARE INPUTS. YOU CAN PROVIDE REGULATED 5V DC TO POWER THE BOARD AT ONE OF THESE PINS; 3.3V PINS ARE OUTPUTS - DO NOT USE THEM TO POWER THE BOARD; GND IS DIGITAL GROUND - COMMON FOR THE BOARD
PWMs 1, 2, 3	PULSE WIDTH MODULATION OUTPUTS #1, #2, #3
I2Cs 0, 2	I2C INTERFACES #0, #1, #2
UART0	SERIAL INTERFACE #0 - DEBUG
UART1; UART4	SERIAL INTERFACES #1; #4
JTAG	JTAG DEBUG INTERFACE
SPI0; SPI1	SPI INTERFACES #0; #1
ADC	ADC SIGNALS



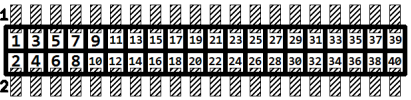
The step between the pinholes of each of the GPIO connectors (including the LCD connector) is 0.05''

The step between the pins of the UART0 debug header is 0.1''

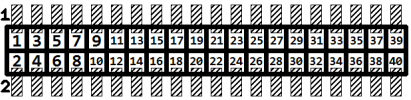
You need a cable with a level shifter to establish a proper serial connection with the UART0 debug header



AM_CON-LCD



AM_CON-GPIO1



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Authorized Distributor

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