RC32312, RC32308

FemtoClock™ 3 Jitter Attenuator and Multi-Frequency Clock Synthesizer

The RC32312/RC32308 is an ultra-low phase noise jitter attenuator, multi-frequency synthesizer, synchronous Ethernet synchronizer, and digitally controlled oscillator (DCO). This flexible, low-power device outputs clocks with 25fs RMS jitter supporting 112Gbps and 224Gbps SerDes.

Applications

- Jitter attenuation for:
  - 112Gbps and 224Gbps SerDes
  - 100 / 200 / 400 / 800 / 1600 Gbps Ethernet PHYs
- Synchronous Ethernet timing cards and line cards
- Switches and routers
- Medical imaging
- Test and measurement

Features

- Jitter 25fs RMS, 12kHz to 20MHz with 4MHz HPF
- Output frequency range:
  - 4kHz to 1GHz for differential outputs
  - 4kHz to 250MHz for single-ended outputs
- Up to 12 HCSL or LVDS outputs with independent integer dividers; differential outputs can be configured as two single-ended outputs
- Up to four clock inputs that can each be configured as differential or as two single-ended inputs
- Input frequency range:
  - 1kHz to 1GHz for differential inputs
  - 1kHz to 250MHz for single-ended inputs
- Compliant to ITU-T G.8262 and G.8262.1
- Hitless reference switching, manual or automatic
- DPLL input-to-output phase variation ≤ 500ps
- DCO frequency resolution < 10^{-13}
- Factory programmable internal OTP
- RC32312
  - 4 inputs and 12 outputs
  - 9 × 9 mm, 64-VFQFPN
- RC32308
  - 3 inputs and 8 outputs
  - 7 × 7 mm, 48-VFQFPN
- Operating voltage: 1.8V
  - Serial ports support 1.8V or 3.3V
- Operating temperature:
  - -40°C to 85°C ambient
  - -40°C to 105°C board

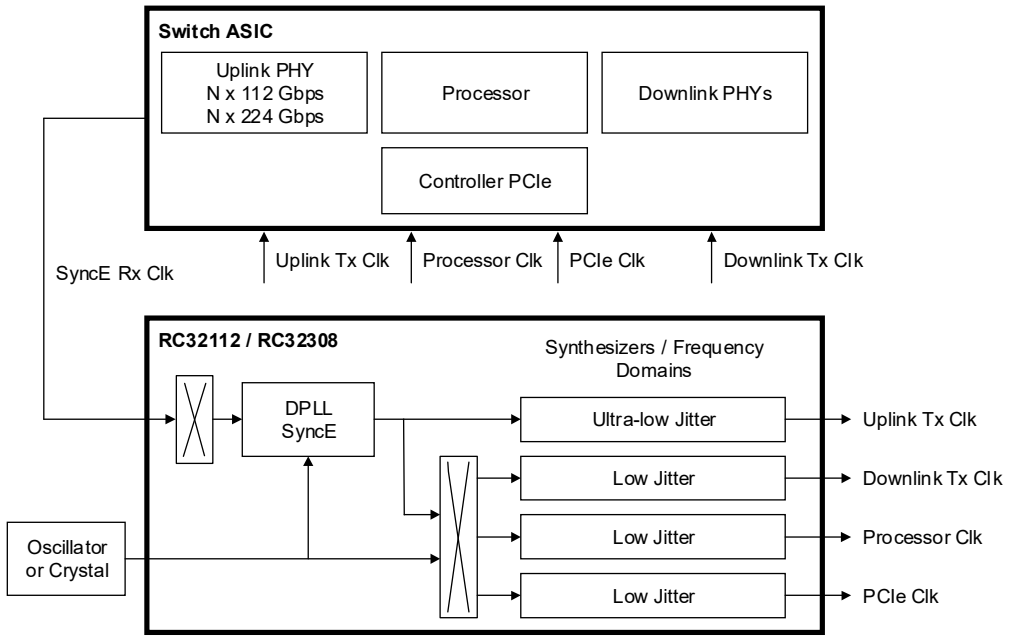

Figure 1. Typical Wireline Infrastructure Use Case

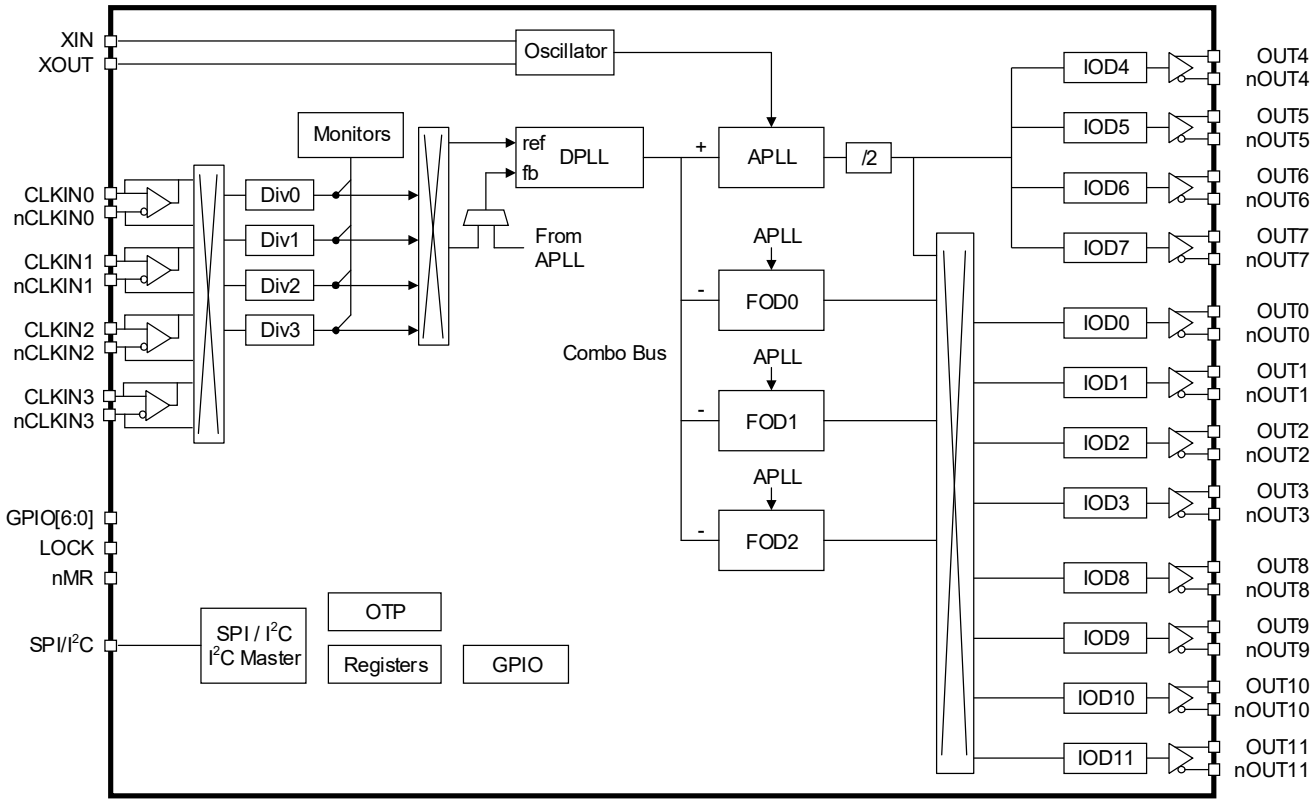

Figure 2. RC32312 Block Diagram

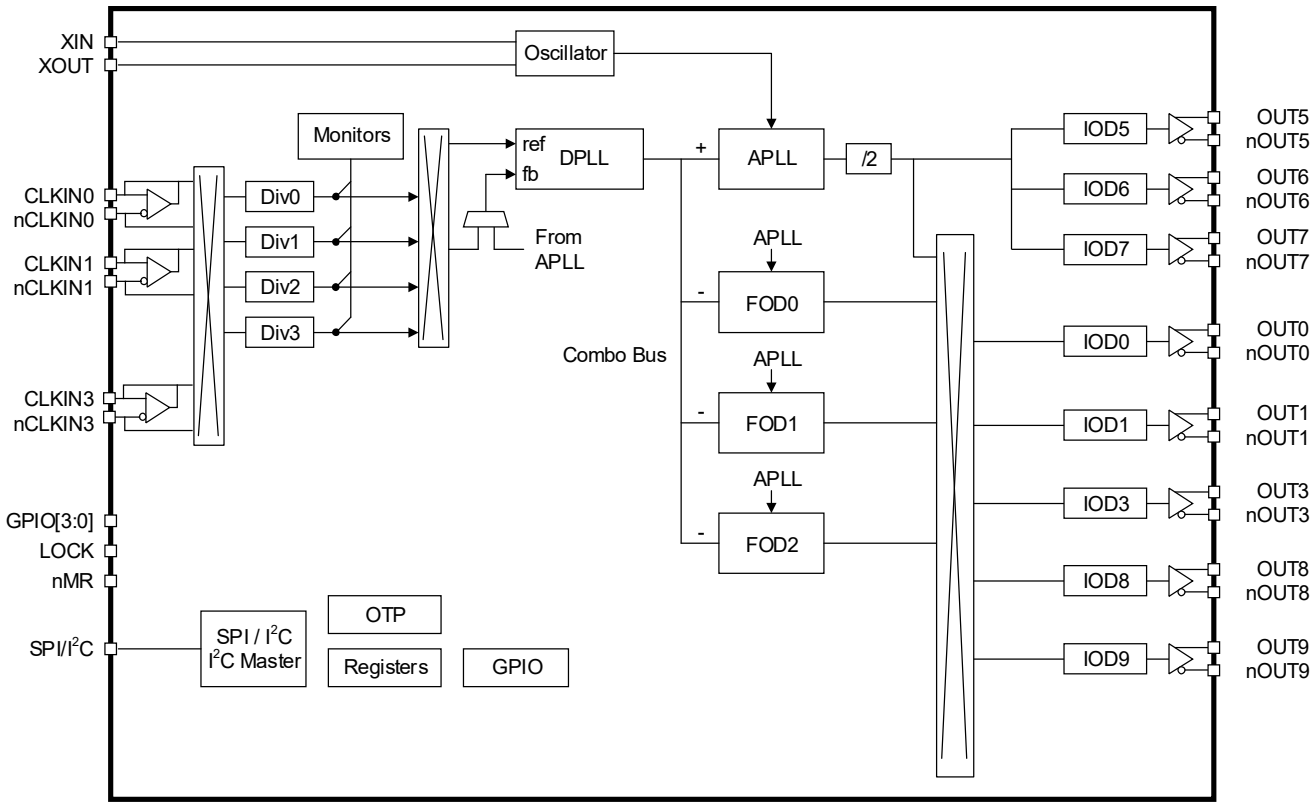

Figure 3. RC32308 Block Diagram

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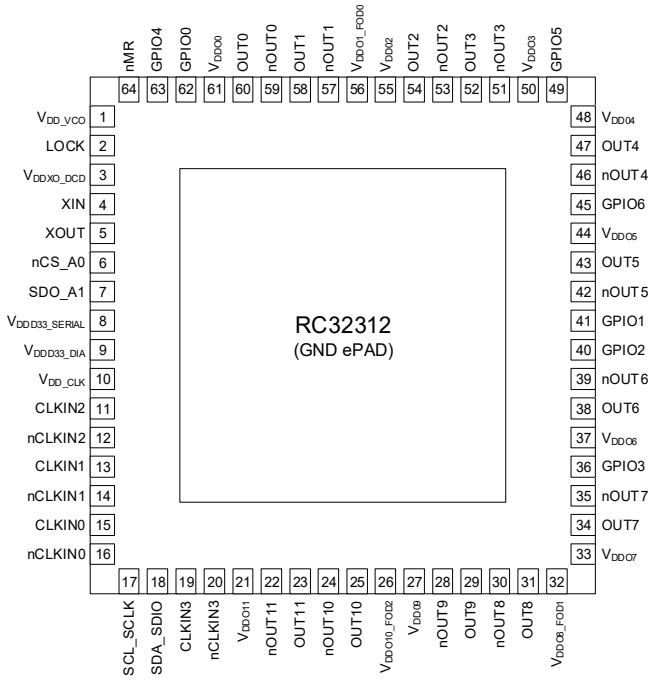
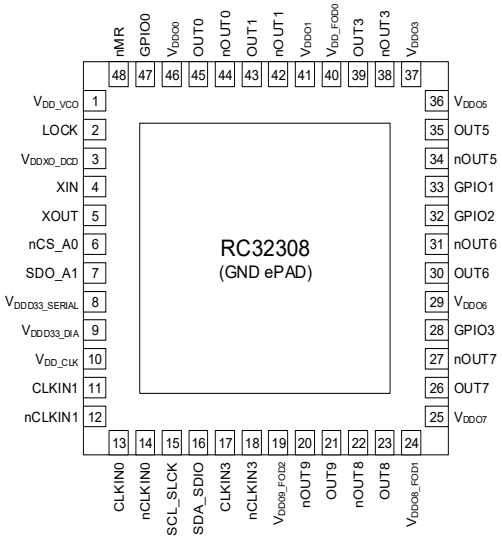
1.1 Pin Assignments

Top View
(9 × 9 mm, 0.5mm lead pitch)



Top View
(7 × 7 mm, 0.5mm lead pitch)



1.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number		Type	Description
	RC32312	RC32308		
XIN	4	4	I	Crystal oscillator / xCXO input.
XOUT	5	5	O	Crystal oscillator output.
CLKIN0	15	13	I	Clock reference input, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair. nCLKINx indicates the negative pin of differential pair.
nCLKIN0	16	14	I	
CLKIN1	13	11	I	
nCLKIN1	14	12	I	
CLKIN2	11	-	I	
nCLKIN2	12	-	I	
CLKIN3	19	17	I	
nCLKIN3	20	18	I	

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Number		Type	Description
	RC32312	RC32308		
OUT0	60	45	O	Clock output, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair. nOUTx indicates the negative pin of a differential pair.
nOUT0	59	44	O	
OUT1	58	43	O	
nOUT1	57	42	O	
OUT2	54	-	O	
nOUT2	53	-	O	
OUT3	52	39	O	
nOUT3	51	38	O	
OUT4	47	-	O	Clock output, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair. nOUTx indicates the negative pin of a differential pair.
nOUT4	46	-	O	
OUT5	43	35	O	
nOUT5	42	34	O	
OUT6	38	30	O	
nOUT6	39	31	O	
OUT7	34	26	O	
nOUT7	35	27	O	
OUT8	31	23	O	Clock output, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair. nOUTx indicates the negative pin of a differential pair.
nOUT8	30	22	O	
OUT9	29	21	O	
nOUT9	28	20	O	
OUT10	25	-	O	
nOUT10	24	-	O	
OUT11	23	-	O	
nOUT11	22	-	O	
nMR	64	48	I	Active-low master reset. The V_{DDO0} pin must be powered to ensure proper operation. GPIO DC electrical characteristics apply to this pin.
nCS_A0	6	6	I	I2C mode: address bit 0. SPI mode: active-low chip select. GPIO DC electrical characteristics apply to this pin.
SCL_SCLK	17	15	I/O	I^2C Mode: I^2C interface bi-directional clock. SPI Mode: serial clock. GPIO DC electrical characteristics apply to this pin.
SDA_SDIO	18	16	I/O	I^2C mode: I^2C interface bi-directional serial data. SPI 3-wire mode: bi-directional serial data. SPI 4-wire mode: input serial data. GPIO DC electrical characteristics apply to this pin.
SDO_A1	7	7	I/O	I^2C mode: address bit 1. SPI 3-wire mode: unused. SPI 4-wire mode: output serial data. GPIO DC electrical characteristics apply to this pin.

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Number		Type	Description
	RC32312	RC32308		
GPIO0	62	47	I/O	General purpose input/output.
GPIO1	41	33	I/O	
GPIO2	40	32	I/O	
GPIO3	36	28	I/O	
GPIO4	63	-	I/O	
GPIO5	49	-	I/O	
GPIO6	45	-	I/O	
LOCK	2	2	O	Lock indicator. This pin is GPIO8 with gpio_func default = 0x1B (APLL lock).
V_{DD_CLK}	10	10	Power	Power supply for CLKINx buffers, dividers, muxes, and the TDC. 1.8V is supported.
V_{DD_VCO}	1	1	Power	Power supply for the VCO. 1.8V is supported.
V_{DDD33_DIA}	9	9	Power	Power supply for digital core, digital in FODs, and digital in the APLL. 1.8V and 3.3V are supported. 1.8V is recommended for lowest power consumption during normal operation.
V_{DDD33_SERIAL}	8	8	Power	Power supply for serial port. 1.8V and 3.3V are supported.
V_{DDO0}	61	46	Power	Power supply for OUT0/nOUT0, IOD0, GPIO0, GPIO4, and nMR. 1.8V is supported.
V_{DDO1_FOD0}	56	-	Power	Power supply for OUT1/nOUT1, IOD1, and FOD0. 1.8V is supported.
V_{DDO1}	-	41	Power	Power supply for OUT1/nOUT1 and IOD1. 1.8V is supported.
V_{DD_FOD0}	-	40	Power	Power supply for FOD0. 1.8V is supported.
V_{DDO2}	55	-	Power	Power supply for OUT2/nOUT2 and IOD2. 1.8V is supported.
V_{DDO3}	50	37	Power	Power supply for OUT3/nOUT3, IOD3, and GPIO5. 1.8V is supported.
V_{DDO4}	48	-	Power	Power supply for OUT4/nOUT4, IOD4, and GPIO6. 1.8V is supported.
V_{DDO5}	44	36	Power	Power supply for OUT5/nOUT5, IOD5 and GPIO1. 1.8V is supported.
V_{DDO6}	37	29	Power	Power supply for OUT6/nOUT6, IOD6, and GPIO2. 1.8V is supported.
V_{DDO7}	33	25	Power	Power supply for OUT7/nOUT7, IOD7, and GPIO3. 1.8V is supported.
V_{DDO8_FOD1}	32	24	Power	Power supply for OUT8/nOUT8, IOD8, and FOD1. 1.8V is supported.
V_{DDO9}	27	-	Power	Power supply for OUT9/nOUT9 and IOD9. 1.8V is supported.
V_{DDO9_FOD2}	-	19	Power	Power supply for OUT9/nOUT9, IOD9, and FOD2. For the RC32308, the V_{DDO9_FOD2} pin must be powered if “any” of the FODs are used. 1.8V is supported.

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Number		Type	Description
	RC32312	RC32308		
V_{DDO10_FOD2}	26	-	Power	Power supply for OUT10/nOUT10, IOD10, and FOD2. For the RC32312, the V_{DDO10_FOD2} pin must be powered if “any” of the FODs are used. 1.8V is supported.
V_{DDO11}	21	-	Power	Power supply for OUT11/nOUT11 and IOD11. 1.8V is supported.
V_{DDXO_DCD}	3	3	Power	Power supply for the analog reference and the LOCK output. 1.8V is supported.
V_{SS}	ePad	ePad	Power	Device ePad. Must be connected to ground.

Table 2. Input Characteristics

Symbol	Parameter		Condition	Minimum	Typical	Maximum	Unit
C_{IN}	Input capacitance	CLKIN/nCLKIN		-	3	-	pF
		nMR, nCS_A0, SDO_A1, GPIOx, SCL_SCLK, SDA_SDIO		-	4	-	
R_{PULLUP}	Input pull-up resistor	nMR		-	98	-	kΩ
		nCS_A0, SDO_A1, GPIOx		-	53	-	
$R_{PULLDOWN}$	Input pull-down resistor	nCS_A0, SDO_A1, GPIOx		-	53	-	kΩ

2. Specifications

2.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{DD33}	Supply Voltage with Respect to Ground	V_{DDD33_Serial}, V_{DDD33_DIA}	-0.5	3.63	V
V_{DD18}	Supply Voltage with Respect to Ground	V_{DD_CLK}, V_{DDXO_DCD}, V_{DD_VCO}, V_{DD05_FOD0}, V_{DDO6_FOD1}, V_{DDO9_FOD2}	-0.5	1.89	V
V_{IN}	Input Voltage	XIN [1]	-0.5	1.32	V
		GPIOx used as inputs, nMR [2]	-0.5	V_{DDOx} + 0.3	
		CLKINx	-0.5	V_{DD_CLK} + 0.3	
		nCS_A0, SDO_A1, SCL_SCLK, SDA_SDIO	-0.5	3.63	
I_{IN}	Input Current	GPIOx used as inputs, nMR	-	±25	mA
		CLKINx	-	±50	
		nCS_A0, SDO_A1, SCL_SCLK, SDA_SDIO	-	±25	
I_{OUT}	Output Current - Continuous	OUTx, nOUTx	-	30	mA
		LOCK, SDO_A1, SCL_SCLK, SDA_SDIO	-	25	
		GPIOx used as outputs	-	25	
	Output Current - Surge	OUTx, nOUTx	-	60	mA
		LOCK, SDO_A1, SCL_SCLK, SDA_SDIO	-	50	
		GPIOx used as outputs	-	50	
T_J	Maximum Junction Temperature		-	150	°C
T_S	Storage Temperature	Storage Temperature	-65	150	°C
-	Human Body Model (Tested per JESD22-A114 (JS-001) Classification)		-	2000	V
-	Charged Device Model (Tested per JESD22-C101 Classification)		-	250	V

1. This limit only applies when XIN is overdriven by an external oscillator. No limit is implied when connected directly to a crystal.
2. V_{DDOx} refers to the supply powering the GPIO or nMR. For V_{DD} pin mapping, see Pin Assignments.

2.2 Recommended Operating Conditions

Table 4. Recommended Operating Conditions [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature		-	-	125	°C
T_A	Ambient Operating Temperature		-40	-	85	°C
V_{DDx}	Supply Voltage with Respect to Ground	V_{DD} pins with 1.8V supply	1.71	1.8	1.89	V
		V_{DD} pins with 3.3V supply	3.135	3.3	3.465	V
t_{PU}	Power up time for all V_{DD} to reach minimum specified voltage	Power ramps must be monotonic	-	-	10	ms

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise.
2. All conditions in this table must be met to guarantee device functionality and performance.

2.3 APLL Phase Jitter

Table 5. APLL Phase Jitter [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[11:0] differential, APLL configured as synthesizer, XIN = 62.5MHz, VCO = 10.625GHz	156.25MHz	-	51	60	fs RMS
		312.5MHz	-	47	56	
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[11:0] differential, APLL steered by DPLL, BW = 25Hz, CLKIN = 25MHz, XIN = 63MHz, VCO = 10.625GHz [5]	156.25MHz	-	63	85	fs RMS
		312.5MHz	-	60	93	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the crystal interface.
3. Measured after the APLL has locked and settled.
4. All outputs enabled and generating clocks with the same frequency sourced from the APLL via integer output dividers.
5. Measured after the DPLL has locked and settled using a jitter free and wander-free reference to the DPLL.

2.4 FOD Phase Jitter

Table 6. FOD Phase Jitter [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[3:0] and OUT[11:8] differential, APLL configured as a synthesizer, XIN = 60MHz, VCO = 10.86GHz	106.25MHz	-	100	165	fs RMS
		212.5MHz	-	82	97	
		425MHz	-	75	101	
		156.25MHz	-	100	165	
		312.5MHz	-	79	115	
		625MHz	-	68	97	
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[3:0] and OUT[11:8] differential, APLL steered by DPLL, BW = 25Hz, CLKIN = 25MHz, FOD configured as synthesizer / DCO, XIN = 60MHz, VCO = 10.15625GHz [5]	156.25MHz	-	89	105	fs RMS
		312.5MHz	-	78	97	
		625MHz	-	73	89	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the crystal interface.
3. Measured after the APLL has locked and settled.
4. All outputs enabled and generating clocks with the same frequency sourced from the same FOD.
5. Measured after the DPLL has locked and settled using a jitter free and wander-free reference to the DPLL.

2.5 Power Supply Noise Rejection

Table 7. Power Supply Noise Rejection [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
PSNR	Power supply rejection ratio V_{DDx} = 1.8V [2][3][4]	f_{NOISE} = 10kHz	-	-125	-	dBc
		f_{NOISE} = 25kHz	-	-127	-	
		f_{NOISE} = 50kHz	-	-117	-	
		f_{NOISE} = 100kHz	-	-99	-	
		f_{NOISE} = 250kHz	-	-92	-	
		f_{NOISE} = 500kHz	-	-80	-	
		f_{NOISE} = 1MHz	-	-81	-	

1. The device will meet specifications after thermal equilibrium is reached.
2. 100mV peak-to-peak sine wave applied to any V_{DDO}, excluding V_{DDO} of the output being measured and excluding V_{DD_VCO}.
3. Relative to 156.25MHz carrier frequency.
4. Measured on any differential output.

2.6 Crystal Oscillator Input and APLL AC/DC Electrical Characteristics

Table 8. Crystal Oscillator Input and APLL AC/DC Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
-	Mode of oscillation	-	Fundamental			-
f_{IN}	Input frequency	Using a crystal with APLL in Integer mode [1]	25	-	80	MHz
		Over-driving crystal interface with APLL in Integer mode [1]	25	-	150	
		Using a crystal with APLL not in Integer mode [2]	25	-	73	
		Over-driving crystal interface with APLL not in Integer mode [2]	25	-	63	
V_{BIAS}	Bias point for XIN	Over-driving crystal interface	-	0.6	-	V
V_{IVS}	Input voltage swing for XIN	Over-driving crystal interface	0.6	-	1.2	V
C_T	Internal crystal oscillator tuning capacitance	xobuf_digicap_x1 = 0x0 xobuf_digicap_x2 = 0x0	-	8	-	pF
		xobuf_digicap_x1 = 0xF xobuf_digicap_x2 = 0xF	-	11.5 [3]	-	
f_{VCO}	Analog PLL VCO operating frequency		9.7	-	10.75	GHz
f_{PULL}	APLL frequency pulling range [4]		-450 + $\lvert F_{TOL} \rvert$	-	450 - $\lvert F_{TOL} \rvert$	ppm

1. APLL configured with integer_mode = 1, apll_fb_div_frac = 0, and the DPLL configured with dpll_mode = 0 (Freerun). Note this configuration does not permit the APLL to be steered by the DPLL/DCO.
2. APLL configured with integer_mode = 0, apll_fb_div_frac ≠ 0.
3. Capacitance increases by 0.25pF for each step of both xobuf_digicap_x1 and xobuf_digicap_x2.
4. F_{TOL} refers to the frequency tolerance of the frequency reference being used (e.g., if F_{TOL} is ±100PPM then f_{PULL} will be ±350PPM).

2.7 Recommended Crystal Characteristics

Table 9. Recommended Crystal Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
ESR	Equivalent series resistance	8pF ≤ C_L ≤ 12pF	-	-	50	Ω
C_O	Shunt capacitance		-	-	4	pF
C_L	Load capacitance		-	-	10	pF
Drive	Drive level [1]	C_L = 8pF	-	-	160	µW
		C_L = 12pF	-	-	290	
F_{TOL}	Frequency tolerance [2][3]	-40°C to 85°C	-450	-	450	PPM

1. Refers to power in the crystal (equivalent series resistance).
2. Inclusive of initial tolerance at 25C, temperature stability, and aging.
3. Applies to the frequency reference, either a crystal connected between XIN and XOUT, or an oscillator connected to XIN and overdriving the crystal interface.

2.8 Clock Input (CLKIN/nCLKIN) AC/DC Characteristics

Table 10. Clock Input (CLKIN/nCLKIN) AC/DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IPP}	Differential input peak-to-peak voltage [1]		0.15	-	1.20	V
V_{CMR}	Differential input common mode voltage [2]	PMOS buffer (HCSL) input	$V_{I(PP)}$ / 2	0.35	V_{DD_CLK} - 1.2	V
		NMOS buffer (LVDS) input	0.7	-	V_{DD_CLK} - $V_{I(PP)}$	
F_{IN}	Input frequency	Differential input	-	-	1000	MHz
		Single-ended input	-	-	150	
F_{PD}	DPLL phase detector frequency [3]		0.001	-	33	MHz
I_{IH}	Differential input high current, CLKIN	V_{IN} = $V_{DD\_CLK\ (max)}$	-	-	5	µA
	Differential input high current, nCLKIN		-	-	5	
I_{IL}	Differential input low current, CLKIN	V_{IN} = 0V	-5	-	-	µA
	Differential input low current, nCLKIN		-5	-	-	
V_{IH}	Input high voltage	V_{DD_CLK} = $V_{DD\_CLK\ (max)}$	0.65 × V_{DD_CLK}	-	V_{DD_CLK} + 0.3	V
V_{IL}	Input low voltage	V_{DD_CLK} = $V_{DD\_CLK\ (max)}$	-0.3	-	0.35 × V_{DD_CLK}	V
I_{IH}	Input high current	V_{IN} = $V_{DD\_CLK\ (max)}$	-	-	5	µA
I_{IL}	Input low current	V_{IN} = 0V	-5	-	-	µA

1. Single-ended value.
2. Common mode is defined as the cross-point.
3. Internal input dividers can be used to reduce the CLKIN/nCLKIN frequency to be within the valid range.

2.9 Output Frequencies and Start-up Time

Table 11. Output Frequencies and Start-up Time

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency for Clocks Sourced from the APLL	Differential Output	0.004	-	1000	MHz
		LVCMOS Output	0.004	-	250	
Δf_{OUT}	Output frequency tuning resolution	Fractional Output Divider	-	-	0.1	PPT
$t_{Start-up}$	Start-up time [1][2]	Synthesizer mode	-	-	9.9	ms

1. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected. Includes time needed to load a configuration from internal OTP.
2. Start-up time will depend on the actual configuration used. For more information, please contact Renesas Technical Support.

2.10 Phase and Frequency Uncertainty

Table 12. Phase and Frequency Uncertainty [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Δt_{HS}	Output phase change using hitless reference switching	DPLL reference frequency = 25MHz, DPLL bandwidth = 0.1Hz	-	15	65	ps
		DPLL reference frequency = 8kHz, DPLL bandwidth = 0.1Hz		150	910	
Δf_{HO}	Initial frequency offset entering holdover	Using holdover filter with 1mHz bandwidth and allowing settling time of 1 hour	-	0.2	0.7	PPB
Δt_{HO}	Initial Phase Shift entering Holdover	Using LOS monitor to disqualify	-	6	30	ps

1. The device will meet specifications after thermal equilibrium has been reached.
2. Measured after the DPLL has locked and settled using a jitter free and wander-free reference.

2.11 Output-to-Output and Input-to-Output Skew

Table 13. Output-to-Output and Input-to-Output Skew [1][2][3]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-output skew differential outputs [4][5]	Any two outputs within the same output bank	-	20	50	ps
		Any two outputs across all output banks from the same APLL or FOD source	-	40	70	ps
		Any two outputs across all output banks from different APLL or FOD sources	-	50	80	ps
	Output-to-output skew LVCMOS outputs [4][5]	Any two outputs within the same output bank	-	40	70	ps
		Any two outputs across all output banks from the same APLL or FOD source	-	60	90	ps
		Any two outputs across all output banks from different APLL or FOD sources	-	80	100	ps
Δt_{SK}	Output-to-output skew temperature variation [4]	Single device, at a fixed voltage, over temperature	-	0.30	2	ps/°C
	Output-to-output skew variation outputs [4]	Single device, over process, temperature, and voltage	-	2	4	ps
t_{PD}	Input-to-output delay differential inputs and differential outputs [6][7]	DPLL path to any output	1.15	1.35	1.55	ns
Δt_{PD}	Input-to-output delay variation [6][7]	Fixed voltage, over temperature	-	1.2	2.0	ps/°C

1. The device will meet specifications after thermal equilibrium has been reached.
2. Output bank 1 refers to OUT[3:0], output bank 2 refers to OUT[7:4], and output bank 3 refers to OUT[11:8].

3. Measured across the full operating temperature range.
4. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
5. This parameter is defined in accordance with JEDEC Standard 65.
6. Input-to-output delay is defined as the time between the rising edge of a reference clock at CLKINx and the associated rising edge of an output clock at OUTx that is locked to the reference by the DPLL. The reference clock and the output clock must have the same frequency and the reference input dividers must be bypassed.
7. Measured after the DPLL has locked and settled using a jitter free and wander-free reference to the DPLL.

2.12 LVCMOS Output AC/DC Characteristics

Table 14. LVCMOS Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output high voltage [2]	I_{OH} = -2mA	V_{DDO} - 0.45	-	-	V
V_{OL}	Output low voltage [2]	I_{OL} = 2mA	-	-	0.45	V
V_{OH}	Output high voltage [2]	I_{OH} = -100µA	V_{DDO} - 0.2	-	-	V
V_{OL}	Output low voltage [2]	I_{OL} = 100µA	-	-	0.2	V
I_{OZ}	Output leakage current	Outputs tri-stated	-5	-	5	µA
Z_{OUTDC}	DC output impedance	At 25°C	-	46	-	Ω
t_R/t_F	Rise/Fall time 20% to 80%		133	200	310	ps
t_{DC}	Output duty cycle		45	50	55	%

1. Measured with outputs terminated with 50Ω to $V_{DDO}/2$.
2. These values are compliant with JESD8-7A.

2.13 LVDS Output AC/DC Characteristics

Table 15. LVDS Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OD}	Output voltage swing [2]	out_cnf_lvds_amp = 0x0	156	377	526	mV
		out_cnf_lvds_amp = 0x1	336	456	594	mV
V_{OS}	Offset voltage	out_lvds_cm_voltage = 0x1	775	900	1025	mV
		out_lvds_cm_voltage = 0x2	875	1000	1125	
		out_lvds_cm_voltage = 0x3	975	1100	1225	
ΔV_{OS}	Change in V_{OS} between complimentary output states		5	20	50	mV
t_R/t_F	Rise/fall time 20% to 80%	out_cnf_lvds_amp = 0x0	73	125	190	ps
		out_cnf_lvds_amp = 0x1	80	135	200	
t_{DC}	Output duty cycle		45	50	55	%

1. Outputs terminated with 100Ω across OUTx and nOUTx.
2. Differential measurement.

2.14 HCSL Output AC/DC Characteristics

Table 16. HCSL Output AC/DC Characteristics [1]

Symbol	Parameter		Condition	Minimum	Typical	Maximum	Unit
V_{OVS} [2]	Output voltage swing	HCSL Mode	out_cnf_hcsl_swing = 0x0	268	284	383	mV
			out_cnf_hcsl_swing = 0x1	319	357	476	mV
			out_cnf_hcsl_swing = 0x2	368	432	564	mV
			out_cnf_hcsl_swing = 0x3	413	503	640	mV
			out_cnf_hcsl_swing = 0x4	456	573	708	mV
			out_cnf_hcsl_swing = 0x5	492	636	766	mV
			out_cnf_hcsl_swing = 0x6	528	691	809	mV
			out_cnf_hcsl_swing = 0x7	559	738	851	mV
			out_cnf_hcsl_swing = 0x8	587	779	885	mV
			out_cnf_hcsl_swing = 0x9	609	812	914	mV
			out_cnf_hcsl_swing = 0xA	638	843	944	mV
			out_cnf_hcsl_swing = 0xB	659	869	967	mV
			out_cnf_hcsl_swing = 0xC	676	891	985	mV
			out_cnf_hcsl_swing = 0xD	696	911	1008	mV
			out_cnf_hcsl_swing = 0xE	711	929	1023	mV
			out_cnf_hcsl_swing = 0xF	725	945	1038	mV
t_R/t_F	Rise/fall time 20% to 80%	out_cnf_hcsl_swing = Any		105	161	225	ps
t_{DC}	Output duty cycle	FOD, 4kHz ≥ f ≤ 650MHz		47	50	52	%

1. Outputs terminated with 50Ω to GND on each OUTx and nOUTx pin.
2. Peak-to-peak output voltage swing on each OUTx and nOUTx pin.

2.15 Power Supply Current

Table 17. Power Supply Current [1]

Symbol	Parameter	Condition	Typical	Maximum	Unit
I_{DD_CLK}	Supply current for V_{DD_CLK}	DPLL only	15		mA
		Per single-ended input	2	-	
		Per differential input	4	-	
I_{DDD33_SERIAL}	Supply current for V_{DDD33_SERIAL}		-	1	mA
I_{DDXO_DCD}	Supply current for V_{DDXO_DCO}	V_{DDXO_DCD} = 1.89V	45	86	mA
I_{DD_VCO}	Supply current for V_{DD_VCO}	V_{DD_VCO} = 1.89V	230	260	mA
I_{DDD33_DIA}	Supply current for V_{DDD33_DIA}	V_{DDD33_DIA} = 1.89V All FODs off $I_{DD\_FODDIGBASE}$	50	-	mA
		V_{DDD33_DIA} = 1.89V Current adder for one FOD at 100MHz $I_{DD\_PERFODDIG}$	55	-	
		V_{DDD33_DIA} = 1.89V Current adder for one FOD per 100MHz over 100MHz $I_{DD\_FODDIGPERMHZ}$	1	-	
		V_{DDD33_DIA} = 3.465V All FODs off $I_{DD\_FODDIGBASE}$	65	-	mA
		V_{DDD33_DIA} = 3.465V Current adder for one FOD at 100MHz $I_{DD\_PERFODDIG}$	70	-	
		V_{DDD33_DIA} = 3.465V Current adder for one FOD per 100MHz over 100MHz $I_{DD\_FODDIGPERMHZ}$	1	-	
I_{DDOx_FODx} [2]	Supply current for V_{DDOx_FODx}	V_{DDOx_FODx} = 1.89V Current with output on, configured for HCSL with 950mV swing, and FOD off. $I_{DD\_FODBASE}$	36	-	mA
		V_{DDOx_FODx} = 1.89V Current with output on, configured for HCSL with 950mV swing, and FOD on. I_{DD_PERFOD}	55	-	mA
		V_{DDOx_FODx} = 1.89V Current adder for the FOD per 100MHz over 100MHz $I_{DD\_FODPERMHZ}$	1	-	mA

Table 17. Power Supply Current [1] (Cont.)

Symbol	Parameter	Condition		Typical	Maximum	Unit
I_{DDOx} [2]	Supply current for V_{DDOx}	HCSL mode	out_cnf_hcsl_swing = 0x0	20	35	mA
			out_cnf_hcsl_swing = 0x1	21	38	
			out_cnf_hcsl_swing = 0x2	22	40	
			out_cnf_hcsl_swing = 0x3	21	42	
			out_cnf_hcsl_swing = 0x4	24	44	
			out_cnf_hcsl_swing = 0x5	25	46	
			out_cnf_hcsl_swing = 0x6	26	47	
			out_cnf_hcsl_swing = 0x7	27	49	
			out_cnf_hcsl_swing = 0x8	28	49	
			out_cnf_hcsl_swing = 0x9	28	49	
			out_cnf_hcsl_swing = 0xA	29	49	
			out_cnf_hcsl_swing = 0xB	30	49	
			out_cnf_hcsl_swing = 0xC	30	49	
			out_cnf_hcsl_swing = 0xD	31	50	
			out_cnf_hcsl_swing = 0xE	32	50	
			out_cnf_hcsl_swing = 0xF	32	50	
I_{DDOx} [2]	Supply current for V_{DDOx}	LVDS mode	out_cnf_lvds_amp = 0x0	18	34	mA
			out_cnf_lvds_amp = 0x1	27	39	
		Output powered down [3][4][5]		3	-	
		Output Hi-Z		14	-	
		LVCMOS mode	One output	17	-	
			Two outputs	25	-	
		Output disabled		14	-	

1. Internal dynamic switching current at maximum f_{OUT} is included, unless otherwise noted.
2. Measured with outputs unloaded.
3. OUT[11:0] are powered down by setting: out_en_bias = 0x0, out_dis_state = 0x3, and out_driver_en = 0x0.
4. IOD[3:0] and IOD[11:8] are powered down by setting: iod_apll_vco_fanout_en = 0x0, iod_mux_sel = 0x7, and iod_enable = 0x0.
5. IOD[7:4] are powered down by setting: iod_apll_vco_fanout_en = 0x0 and iod_enable = 0x0.

2.16 GPIO DC Electrical Characteristics

Table 18. GPIO DC Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage [2][3]	GPIOx	0.77 × V_{DDOx}	-	V_{DDOx} + 0.3	V
V_{IL}	Input low voltage [2]	GPIOx	-0.3	-	0.31 × V_{DDOx}	V
V_{OH}	Output high voltage [2][3]	GPIOx, I_{OH} = -2mA	V_{DDOx} - 0.45	-	V_{DDOx} + 0.3	V
V_{OL}	Output low voltage [2]	GPIOx, I_{OL} = 2mA	-	-	0.45	V
V_{OH}	Output high voltage [2][3]	GPIOx, I_{OH} = -100µA	V_{DDOx} - 0.2	-	V_{DDOx} + 0.3	V
V_{OL}	Output low voltage [2]	GPIOx, I_{OL} = 100µA	-	-	0.2	V

1. Input specifications refer to signals GPIOx, when acting as inputs. Output specifications refer to signals GPIOx, when acting as outputs.
2. These values are compliant with JESD8-7A.
3. V_{DDOx} refers to the supply powering the GPIO. For V_{DD} pin mapping, see GPIO V_{DD} Pin Assignments.

2.17 CMOS GPIO Common Electrical Characteristics

Table 19. CMOS GPIO Common Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
I_{IL}	Input leakage current[2]	Does not include input pull-up/pull-down resistor current. V_{IL} = 0V, V_{IH} = V_{DD}	-15	-	15	µA
R_P	Pull-up/pull-down resistor	If enabled	-	53	-	kΩ

1. Input specifications refer to signals GPIOx, when acting as inputs. Output specifications refer to signals GPIOx, when acting as outputs. For V_{DD} pin mapping, see GPIO V_{DD} Pin Assignments.
2. V_{DDOx} refers to the supply powering the GPIO. For V_{DD} pin mapping, see GPIO V_{DD} Pin Assignments.

2.18 I²C Bus Slave Timing Diagram

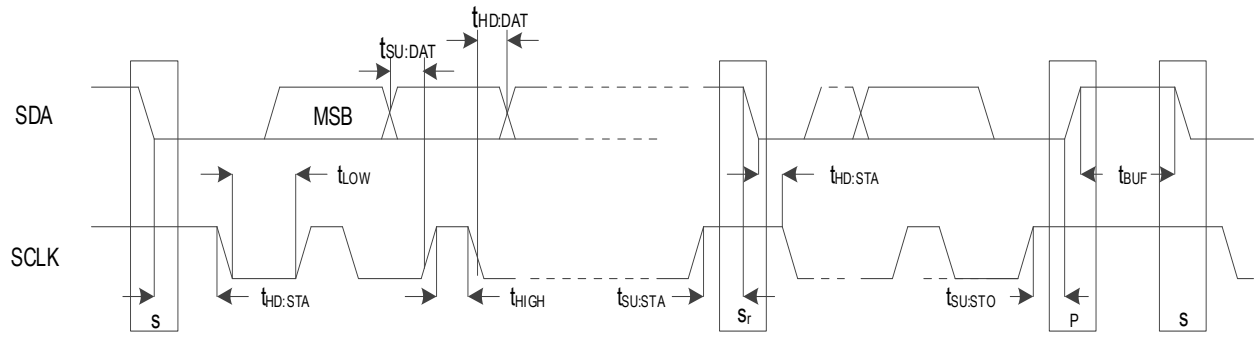


Figure 4. I²C Bus Slave Timing Diagram

2.19 I²C Bus Slave Timing Characteristics

Table 20. I²C Bus Slave Timing Characteristics

Symbol	Parameter	Minimum	Maximum	Unit
f_{SCL}	SCL clock frequency	10	1000	kHz
$t_{HD:STA}$	Hold time after (REPEATED) START Condition	0.26	-	µs
t_{LOW}	Clock low period	0.5	-	µs
t_{HIGH}	Clock high period	0.26	-	µs
$t_{SU:STA}$	REPEATED START Condition setup time	0.26	-	µs
$t_{HD:DAT}$	Data hold time	0	-	ns
$t_{SU:DAT}$	Data setup time	50	-	ns
$t_{SU:STO}$	STOP condition setup time	0.26	-	µs
t_{BUF}	Bus free time between STOP and START Condition	0.5	-	µs

2.20 I²C Bus AC/DC Electrical Characteristics

Table 21. I²C Bus AC/DC Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	High-level input voltage for SCL_SCLK and SDA_nCS		0.8 × V_{DDD33}	-	-	V
V_{IL}	Low-level input voltage for SCL_SCLK and SDA_nCS		-	-	0.3 × V_{DDD33}	V
V_{HYS}	Hysteresis of Schmitt trigger inputs		0.05 × V_{DDD33}	-	-	V
V_{OL}	Low-level output voltage for SCL_SCLK and SDA_nCS	I_{OL} = 2mA	-	-	0.4	V
I_{IN}	Input leakage current per pin		[2]	-	[2]	µA

1. VOH is governed by the VPUP, the voltage rail to which the pull-up resistors are connected.
2. See CMOS GPI/GPIO Common Electrical Characteristics in Table 19.

2.21 SPI Slave Timing Diagrams

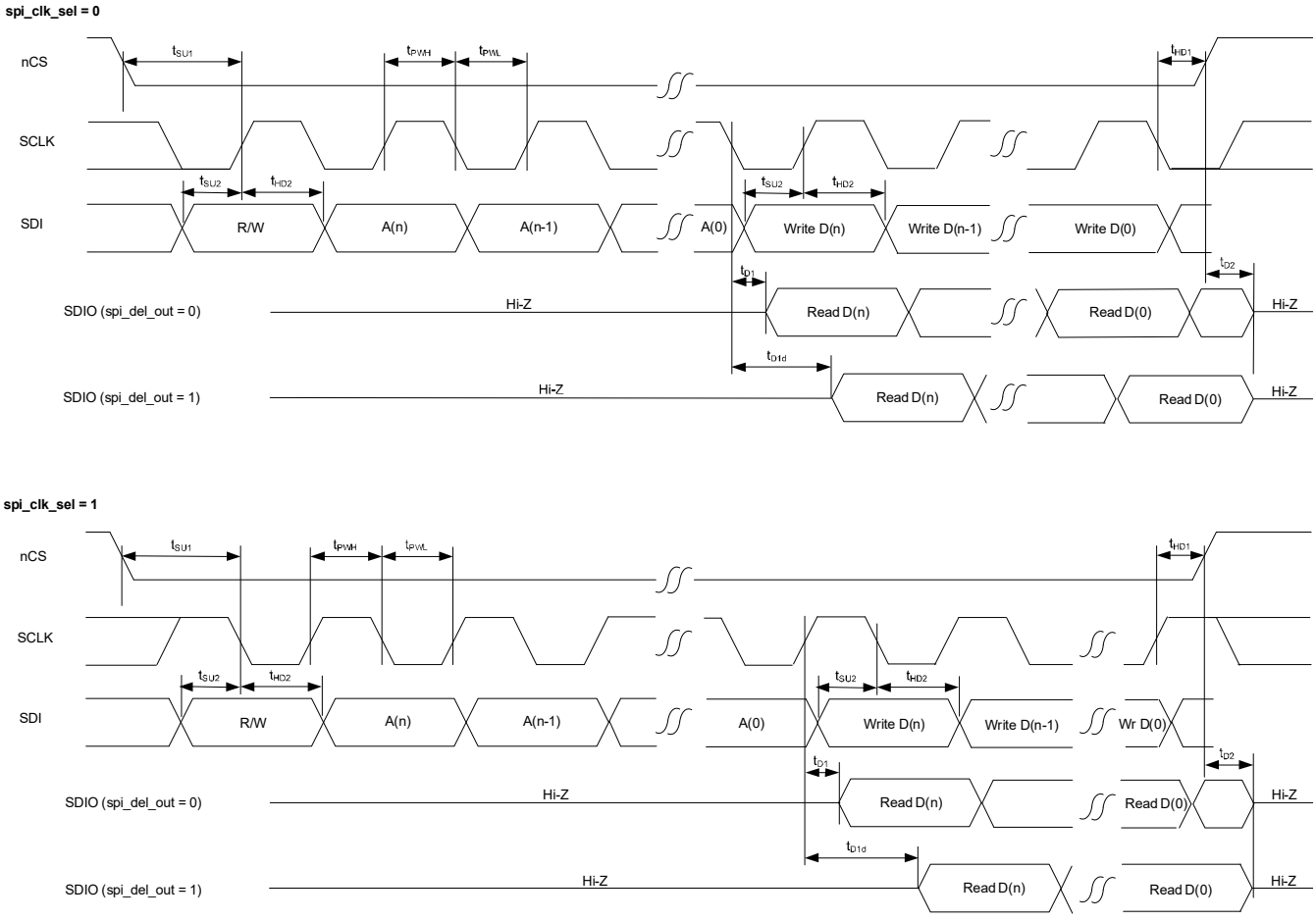


Figure 5. SPI Slave Timing Diagrams

2.22 SPI Slave Timing Characteristics

Table 22. SPI Slave Timing Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_{MAX}	Maximum operating frequency	0.1	-	20	MHz
t_{PWH}	SCLK pulse width high	-	50	-	ns
t_{PWL}	SCLK pulse width low	-	50	-	ns
t_{SU1}	nCS setup time to SCLK rising or falling edge	10	-	-	ns
t_{HD1}	nCS hold time from SCLK rising or falling edge	-	1	-	ns
t_{SU2}	SDIO setup time to SCLK rising or falling edge	-	4	-	ns
t_{HD2}	SDIO hold time from SCLK rising or falling edge	10	-	-	ns
t_{D1}	Read data valid time from SCLK rising or falling edge including half period of SCLK delay added to data timing	11	-	-	ns
t_{D1d}	Read data valid time from SCLK rising or falling edge including half period of SCLK delay added to data timing [1]	-	6 + half SCLK period	-	ns
t_{D2}	SDIO read data Hi-Z time from CS high [2]	-	10	-	ns

1. Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.
2. This is the time until the device releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

2.23 Thermal Resistance

Table 23. Thermal Resistance

Package	Symbol	Conditions [1]	Typical Value	Unit
NDG48	Θ_{JC}	Junction to case	17.5	°C/W
	Θ_{JB}	Junction to base	1.0	
	Θ_{JA0}	Junction to air, still air	20.0	
NDG64	Θ_{JC}	Junction to case	13.1	°C/W
	Θ_{JB}	Junction to base	1.0	
	Θ_{JA0}	Junction to air, still air	20.0	

1. ePad soldered to board.

3. Functional Description

3.1 Overview

The RC32312/RC32308 is an ultra-low phase noise jitter attenuator, multi-frequency synthesizer, synchronous Ethernet synchronizer, and digitally controlled oscillator (DCO). This flexible, low-power device outputs clocks with 50fs RMS (12kHz to 20MHz) jitter supporting SerDes operating at rates up to 112Gbps and 25fs RMS (12kHz to 20MHz with 4MHz high pass filter) supporting SerDes operating at 224Gbps.

The RC32312 has four differential clock inputs and 12 differential clock outputs, see Figure 2. The RC32308 has three differential clock inputs and eight differential clock outputs, see Figure 3. Both devices provide a digital PLL (DPLL) with an ultra-low phase noise analog PLL (APLL) based clock synthesizer and three fractional output divider (FOD) based clock synthesizers.

The differential clock inputs can each be configured as two single-ended inputs. The clock inputs can operate at frequencies up to 1GHz for differential and 250MHz for single-ended. The differential outputs can be configured as LVDS or HCSL. When configured for LVDS or HCSL, the differential outputs can operate at frequencies up to 1GHz. Each differential output can be configured as two LVCMOS outputs that can operate at frequencies up to 250MHz.

3.2 Frequency Reference

The device requires a frequency reference. The frequency reference can be implemented using an external crystal resonator connected between the XIN and XOUT pins and the device oscillator circuitry. Alternatively, an external oscillator can be connected to the XIN pin to overdrive the device oscillator circuitry. For the frequency ranges supported for crystal resonators and external oscillators, see Table 8.

The frequency reference must support the phase noise, frequency accuracy, and frequency stability requirements of the intended application. The phase noise of the frequency reference affects the phase noise of clocks output by the device. The accuracy of the frequency reference determines the frequency accuracy of the reference monitors and free-run clocks. The stability of the frequency reference determines the holdover stability of the DPLL and it affects the lowest filtering bandwidth the DPLL can support.

3.3 Analog PLL

The internal APLL locks to the device oscillator and synthesizes an ultra-low phase noise clock of virtually any frequency between 9.70GHz and 10.75GHz.

The APLL is the primary synthesizer for the DPLL and its fractional frequency offset (FFO) can be steered by the DPLL. When the DPLL is locked to a reference, the APLL output clock and its derivatives have the same long-term frequency accuracy as the reference.

The APLL output clock is pre-divided by 2 and is available to the integer output dividers (IOD). The pre-divided APLL clock is available directly to IOD[7:4]; it is also available via cross-connect to IOD[3:0] and IOD[11:8]. The undivided APLL clock is supplied to FOD[2:0].

3.4 Integer Output Dividers

Each IOD divides its input clock by a programmable 21-bit integer value.

3.5 Fractional Output Dividers

The FODs divide the APLL clock to synthesize low phase noise clocks with programmable frequencies from 120MHz to 700MHz. The FODs are capable of integer division, rational division (i.e., M/N), and fractional division with 1 part per trillion frequency resolution. The FOD output clocks are available, via cross-connect, to IOD[3:0] and IOD[11:8].

When configured for fractional division, the FODs can operate as DCOs with steering range of ±244PPM. The FODs can be configured to cancel frequency adjustments made by the DPLL to the APLL via the Combo Bus so that their output frequencies are virtually unaffected by the DPLL.

3.6 Divider Synchronization

The DPLL feedback divider is synchronized with the IODs. The rising edges of clocks from these dividers will be aligned for every Nth rising edge of the APLL clock, where N is the lowest common multiple of the accumulated divide ratios along the paths from the APLL to the divider outputs.

Consider the following example: The DPLL is locked to a 1kHz input reference and the APLL is operating at 10GHz. The pre-divider supplies a 5GHz clock to IOD1, IOD2 and the DPLL feedback divider. IOD1 uses a divide ratio of 40 to produce a 125MHz clock, IOD2 uses a divide ratio of 625,000 to produce an 8kHz clock, and the DPLL feedback divider uses a divide ratio of 5,000,000 to produce 1kHz at the DPLL phase detector. In this example, the lowest common multiple of the divisors along the three paths is 10,000,000. Therefore, the outputs of IOD1 and IOD2 will be aligned with the input reference once for every 10,000,000 edges of the 10GHz clock. In other words, the 1kHz reference, the 8kHz and the 125MHz clocks will be aligned for every edge of the 1kHz input reference (excluding the effects of reference noise and DPLL filtering).

3.7 Digital PLL

Up to four of the clock inputs can be selected as inputs for the reference monitors and the DPLL reference selection multiplexer. The DPLL can lock to reference frequencies between 1kHz and 33MHz; clock inputs with frequencies above 33MHz must be divided using the internal reference dividers. The DPLL steers the APLL using digital frequency control words via the Combo Bus. The DPLL supports programmable filtering bandwidths between 0.05Hz and 1kHz.

The DPLL operates in five states: Free-run, Acquire, Normal, Holdover, and Hitless Switch.

In DCO mode, the DPLL does not lock to an input reference and its frequency is steered by external software instead.

3.7.1 DPLL Free-run State

In the Free-run state, the DPLL does not generate frequency control words and the APLL synthesizes clocks based on the frequency reference.

3.7.2 DPLL Acquire State

In the Acquire state, the DPLL tracks the selected qualified reference with the acquisition bandwidth and damping factor settings until the DPLL declares lock. The acquisition bandwidth and damping factor can be configured to accelerate the locking process. When the DPLL achieves lock it automatically transitions to the Normal state.

3.7.3 DPLL Normal State

In the Normal state, the DPLL tracks the selected reference with the normal locking bandwidth and damping factor settings. The normal bandwidth and damping factor can be configured to meet the filtering requirements of the intended application. In the Normal state the long-term FFO of the APLL output clocks is the same as the long-term FFO of the reference and no phase slips will occur.

3.7.4 DPLL Holdover State

In the Holdover state, the DPLL outputs digital frequency control words based on data acquired while in the Normal state so that the APLL outputs an accurate frequency when a reference is not provided to the DPLL. While the DPLL is in the Holdover state, the APLL generates clocks based on the frequency reference and DPLL holdover data.

3.7.5 DPLL Hitless Switch State

In the Hitless Switch state, the DPLL enters Holdover and measures the phase offset between the selected reference and the DPLL feedback clock. The measured phase offset is stored by the DPLL and is used to minimize the phase transient at the output of the DPLL when it locks to the new reference.

3.8 DPLL External Feedback

In some applications it is useful to use an external feedback path from the APLL to the DPLL. The DPLL reference selection multiplexer can select one of the external references for use as the feedback clock for the DPLL. When external feedback is used, the feedback clock must have the same frequency as the selected DPLL reference.

3.9 DPLL Reference Switching

The active reference for the DPLL is determined by forced selection or by automatic selection based on user-programmed priorities, locking allowances, reference monitors, revertive and non-revertive settings, and GPIO LOS inputs.

The DPLL will act to close phase differences between the selected reference and the feedback clock. A step change in the phase difference can occur when a new reference is selected while the DPLL is in the Acquire state or the Normal state; or when the DPLL exits the Holdover state and enters the Acquire state. The resulting phase transient is filtered by the DPLL loop filter and the phase slope limiter; and there will not be any sudden phase steps or glitches on the device outputs.

3.9.1 Hitless Reference Switching

Hitless reference switching causes the DPLL to ignore the phase difference between the newly selected reference and the DPLL feedback clock; the DPLL will track the FFO of the newly selected reference.

When hitless reference switching is enabled – and the DPLL is the Acquire state or the Normal state, and the selected reference is changed – the DPLL enters the Holdover state and measures the phase offset between the newly selected reference and the DPLL feedback clock. The measured phase offset is stored and is subtracted from later phase offsets measured by the DPLL phase detector. The DPLL then enters the Acquire state.

When the DPLL is in the Holdover state due to a reference failure or any other reason, hitless reference switching can be used when entering the Acquire state.

3.9.2 Aligned Reference Switching

Hitless reference switching does not allow a deterministic phase relationship to exist between the DPLL reference and its output clocks. When a deterministic phase relationship is needed, hitless reference switching should not be enabled so that the DPLL can align its output clocks with the DPLL reference.

3.10 Reference Monitors

The references can be continually monitored for loss of signal and for frequency offset per user programmed thresholds.

3.11 Status and Control

All control and status registers are accessed through a 1MHz I^2C or 20MHz SPI slave microprocessor interface. The device can automatically load a configuration from internal one time programmable (OTP) memory. Alternatively, the I^2C master interface can automatically load a configuration from an external EEPROM after reset.

Note: For registers information, contact Renesas Technical Support.

4. Applications Information

4.1 Power Considerations

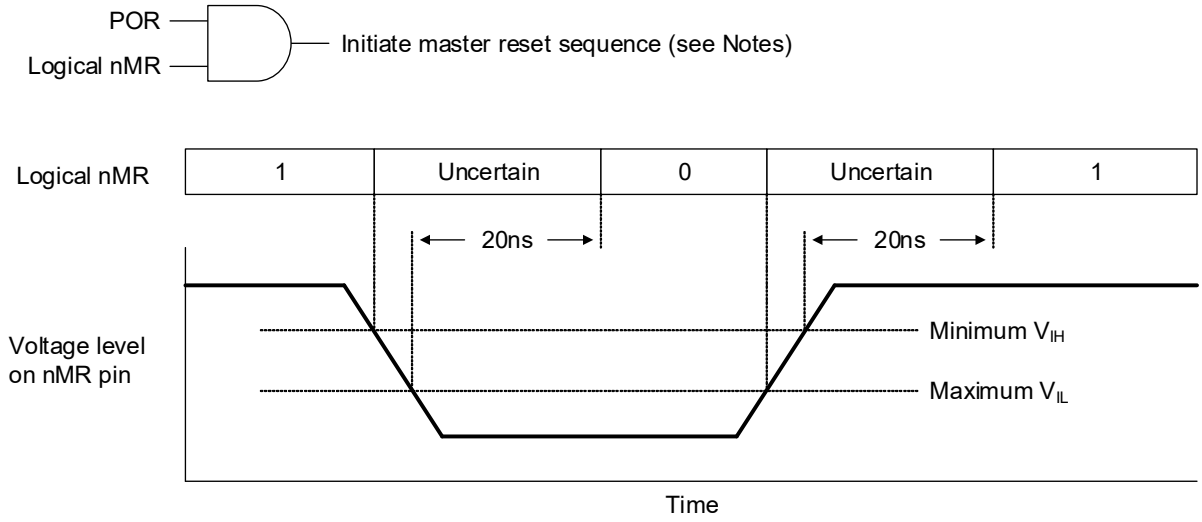
There are no power supply sequencing requirements; however, if V_{DDOx} or V_{DD_CLK} reach 90% of V_{DD} nominal after the later of V_{DD_VCO} or V_{DDD33_DIA} then a soft reset or a master reset must be initiated to ensure the input dividers and output dividers are synchronized.

For power and current consumption calculations, see the Renesas IC Toolbox (RICBox) software tool.

4.2 Power-On Reset and Reset Controller

Upon power-up, an internal power-on reset (POR) signal is asserted 5ms after both the V_{DDXO_DCD} and V_{DDD33_DIA} supplies reach 90% of V_{DD} nominal. The first master reset sequence is initiated when POR is asserted and the voltage level on the nMR pin is high.

After the first master reset sequence is initiated, another master reset sequence can be initiated by taking the voltage level on the nMR pin low and then high while POR remains asserted (see Figure 6). To ensure a master reset sequence is initiated, the voltage level on the nMR pin must be held low for at least 20ns before transitioning high. To ensure deterministic behavior, voltage level transitions on the nMR pin must be monotonic between minimum V_{IH} and maximum V_{IL} (see Table 18).



Notes:
- Requires 1 from logical nMR for the first master reset sequence
- Requires 0 to 1 transition from logical nMR after the first master reset sequence has been initiated

Figure 6. Master Reset Sequence Initiation

The nMR pin has an internal pull-up that can be left to float, or it can optionally be externally pulled high or low. If nMR is high when the internal POR is asserted, the reset controller will initiate a master reset sequence. If nMR is low when the internal POR is asserted, the reset controller will not initiate a master reset sequence until nMR is taken high.

During the master reset sequence, all clock outputs are optionally disabled depending on the value of the out_startup register field. Disabled outputs behave according to the associated out_dis_state register field.

The serial ports are accessible when the device_ready_sts register bit is set to 0x1. Any GPIO can be configured to indicate the state of the device_ready_sts register bit by setting the associated gpio_func register field to 0x18. When a reset sequence completes, the rst_done_sts register bit is set to 0x1.

When a configuration is loaded from EEPROM, the voltage level on the nMR pin must be held high from the time a master reset sequence is initiated until after the EEPROM transactions have completed, as indicated when the device_ready_sts register bit is set to 0x1.

4.3 Recommendations for Unused Input and Output Pins

4.3.1 CLKIN/nCLKIN Pins

Unused CLKIN/nCLKIN pins should be left to float. Renesas recommends that CLKIN/nCLKIN inputs that are connected but not used should not be driven with active signals.

4.3.2 LVCMOS Control Pins

LVCMOS control pins have internal pull-up resistors. Additional 1kΩ pull-up resistors can be added but are not required.

4.3.3 LVCMOS Output Pins

Unused LVCMOS outputs must be left to float; Renesas recommends that no trace should be attached. Unused LVCMOS outputs should be configured to a high-impedance state to prevent noise generation.

4.3.4 Differential Output Pins

Unused differential outputs must be left to float; Renesas recommends that no trace should be attached. Both sides of a differential output pair should be either left to float or terminated.

4.4 Overdriving the Crystal Interface

When overdriving the crystal interface, the XOUT pin is left to float and the XIN input is overdriven by an AC coupled LVCMOS driver, or by one side of an AC coupled differential driver. The XIN pin is internally biased to 0.6V. The voltage swing on XIN should be between 0.5V peak-to-peak and 1.2V peak-to-peak, and the slew rate should not be less than 0.6V/ns.

Figure 7 shows an LVCMOS driver overdriving the XIN pin. For this implementation, the voltage swing at XIN will equal $V_{DD} \times R_1 / (R_O + R_S + R_1)$. The values of V_{DD}, R_S, and R_1 should be selected so that the voltage swing at XIN is below 1.2V peak-to-peak.

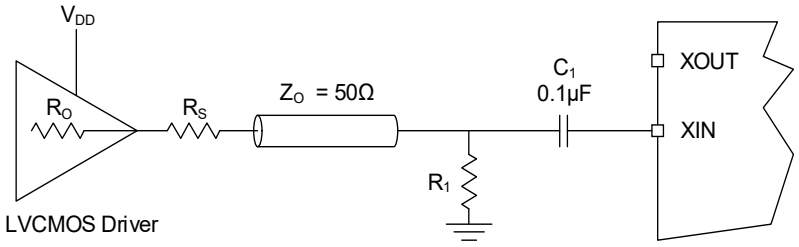


Figure 7. LVCMOS Driver to Crystal Input Interface

Figure 8 shows one side of an LVPECL driver overdriving the XIN pin.

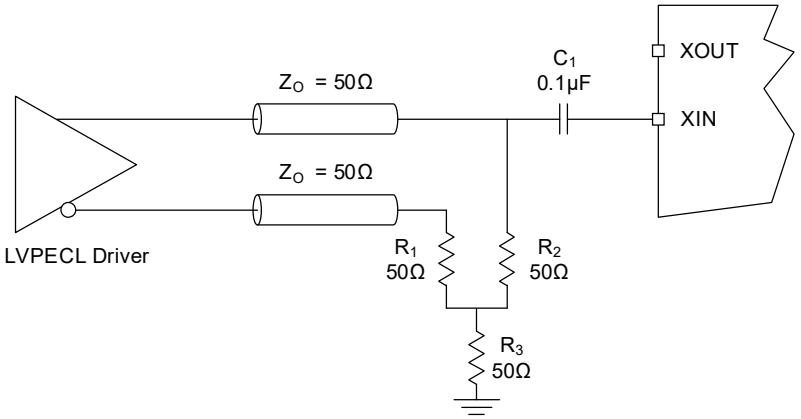


Figure 8. LVPECL Driver to Crystal Input Interface

4.5 Differential Output Termination

The RC32312, RC32308 programmable differential clock outputs support HCSL and LVDS. Receivers that support HCSL or LVDS can be direct-coupled with RC32312, RC32308 outputs. Differential receiver types other than HCSL or LVDS can be AC-coupled.

The RC32312, RC32308 HCSL clock outputs support selectable internal termination resistors as shown in Figure 9. The value of resistors $R_{O1\ and}$ R_{O2} is 50Ω.

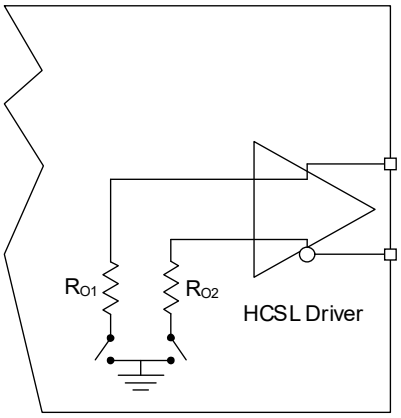


Figure 9. Internal Termination Resistors for Differential Drivers

Note: Some receivers are equipped with internal terminations that can include the following: trace termination, voltage biasing, and AC-coupling. Consult with the receiver specifications to determine if the termination components shown in this section are needed.

4.5.1 Direct-Coupled HCSL Terminations

For HCSL receivers, RC32312, RC32308 clock outputs should be configured for HCSL, and the devices should be direct-coupled. The RC32312, RC32308 supports a wide range of programmable HCSL voltage swing options.

Figure 10 shows an HCSL driver direct-coupled with an HCSL receiver and configured for internal termination. The RC32312, RC32308 supports source termination, with internal 50Ω resistors to ground at the transmitter. Resistor R_1 is optional and is used to improve impedance matching. If R_1 is used, it will reduce the amplitude at the receiver by 50% – this can be mitigated by adjusting the output amplitude of the driver.

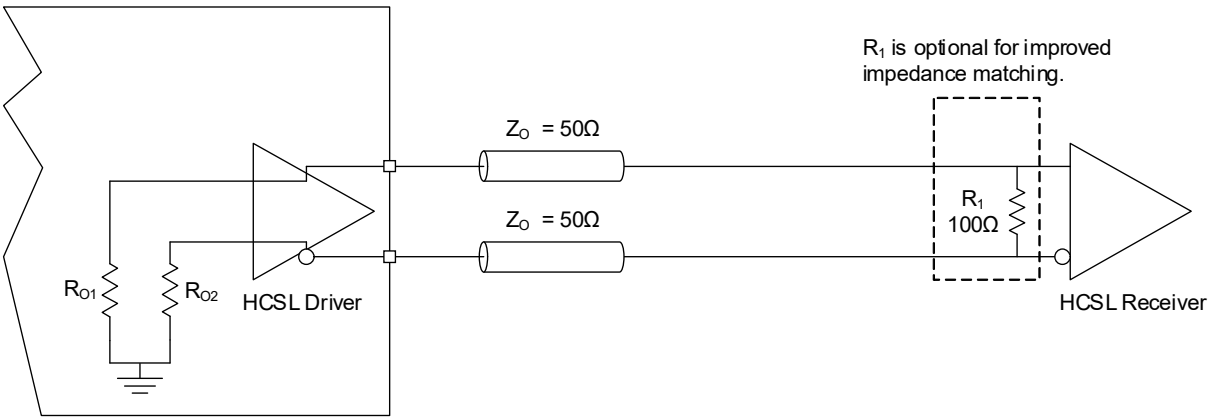


Figure 10. HCSL Internal Termination

Figure 11 shows an HCSL driver direct-coupled with an HCSL receiver and configured for external termination. If the HCSL receiver has an internal 100Ω termination resistor then it will reduce the signal amplitude at the receiver by 50% – this can be mitigated by adjusting the output amplitude of the driver.

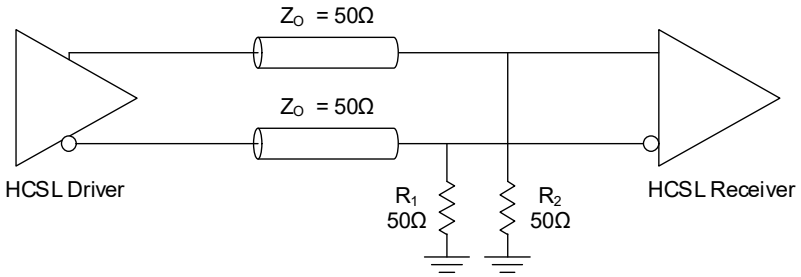


Figure 11. HCSL External Termination

For alternative termination schemes, see HCSL Terminations in *Quick Guide - Output Terminations* located on the RC32312/RC32308 product page, or contact Renesas for support.

4.5.2 Direct-Coupled LVDS Termination

For LVDS receivers, RC32312, RC32308 clock outputs should be configured for LVDS, and should be direct-coupled. The RC32312, RC32308 supports several programmable LVDS voltage swing and common mode options.

Figure 12 shows an LVDS driver direct-coupled with an LVDS receiver. The recommended value for the termination resistor (R_1) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of the transmission line. To avoid transmission-line reflection issues, R_1 should be surface-mounted and placed as close to the receiver as practical.

For alternative termination schemes, see LVDS Terminations in *Quick Guide - Output Terminations* located on the RC32312/RC32308 product page, or contact Renesas for support.

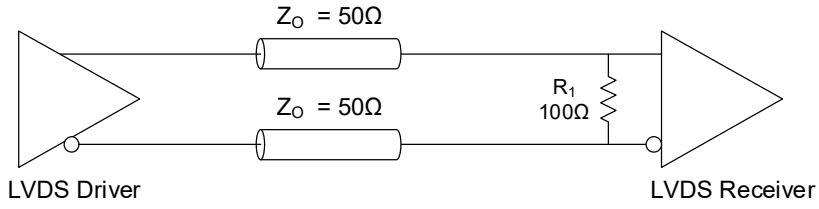


Figure 12. LVDS Termination

4.5.3 AC-Coupled Differential Termination

For differential receivers that do not support HCSL or LVDS, RC32312, RC32308 clock outputs should be configured for HCSL, and AC-coupling should be used. The HCSL driver should be configured with a voltage swing appropriate for the receiver. The RC32312, RC32308 supports a wide range of programmable HCSL voltage swing options.

Figure 13 shows an HCSL driver configured for internal termination and AC-coupled with a differential receiver. Resistors R_1, R_2, R_3, and R_4 should be selected to provide the appropriate bias voltage for the receiver (for more information, see the receiver specifications). An optional resistor (R_5) can be used to improve impedance matching. If R_5 is used, it will reduce the signal amplitude at the receiver by 50%; this can be mitigated by adjusting the output amplitude of the driver.

For alternative termination schemes, see HCSL Terminations in *Quick Guide - Output Terminations* located on the RC32312/RC32308 product page, or contact Renesas for support.

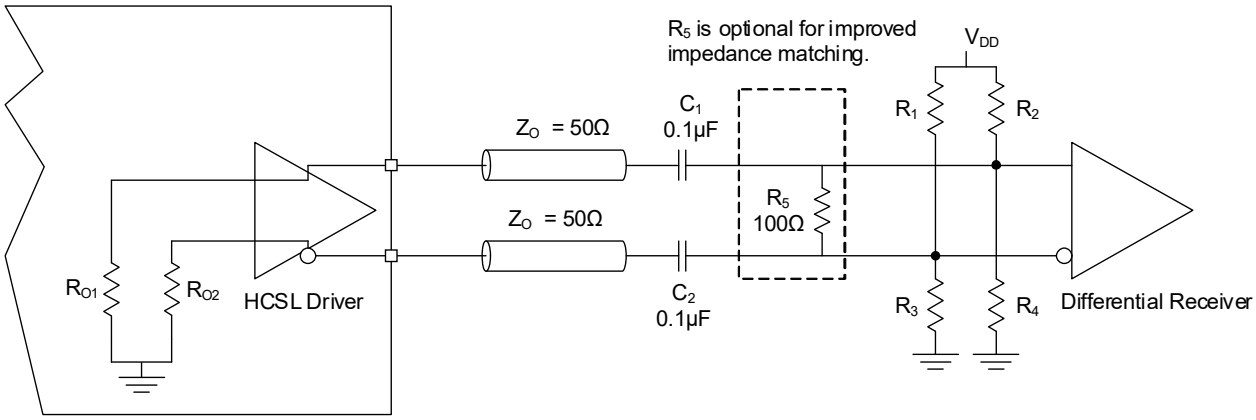


Figure 13. AC-Coupled Differential Termination

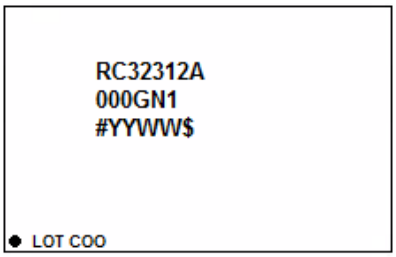
5. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

6. Device ID Register

Device	Device_ID (Base Address 0x02)
RC32308	0xC5C1
RC32312	0xC5C2

7. Marking Diagram



- Lines 1 and 2 are the part number.
- Line 3:
  - “#” denotes the stepping number.
  - “YYWW” denotes the last two digits of the year and the work week the part was assembled.
  - “$” denotes the mark code.

- Lines 1 and 2 are the part number.
- Line 3:
  - “#” denotes the stepping number.
  - “YYWW” denotes the last two digits of the year and the work week the part was assembled.
  - “$” denotes the mark code.

8. Ordering Information

Part Number [1]	Package Description	Carrier Type	Temperature Range
RC32308AxxxGNE#KB0	48-VFQFPN, 7 × 7 mm	Tape	-40 to +85°C
RC32308AxxxGNE#BB0	48-VFQFPN, 7 × 7 mm	Tray	
RC32312AxxxGN1#KB0	64-VFQFPN, 9 × 9 mm	Tape	-40 to +85°C
RC32312AxxxGN1#BB0	64-VFQFPN, 9 × 9 mm	Tray	

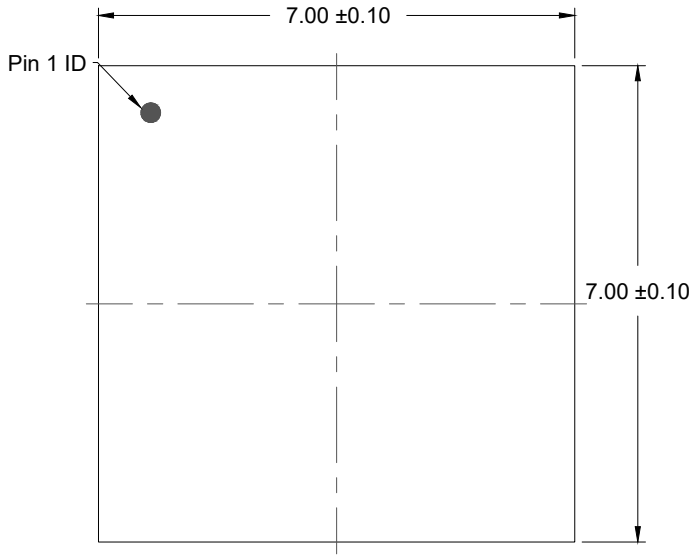
1. Replace “xxx” in the part number with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use “000” for unprogrammed parts.

9. Revision History

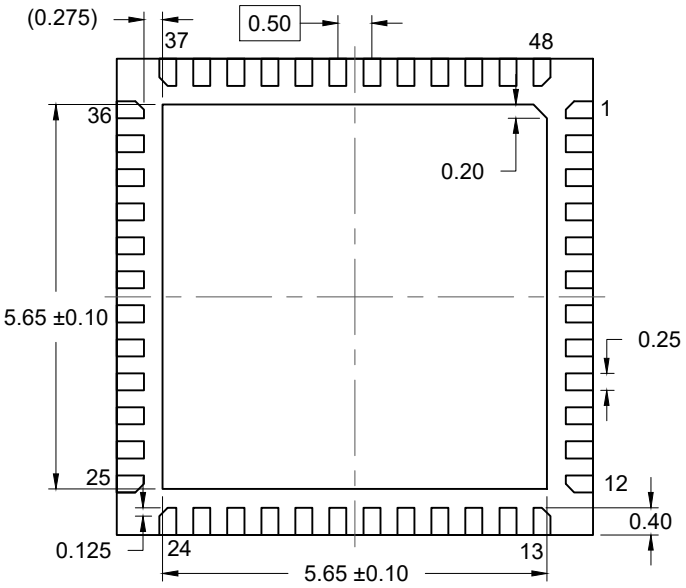
Revision	Date	Description
1.07	Apr 5, 2024	▪ Completed minor changes.
1.06	Mar 28, 2024	▪ Updated Figure 3 and Figure 5.
1.05	Mar 15, 2024	▪ Updated the nMR, nCS_A0, SCL_SCLK, SDA_SDIO and SDO_A1 pins in Table 1. ▪ Updated footnote 1 in Table 19. ▪ Updated Power-On Reset and Reset Controller section. ▪ Updated footnotes 3 and 4 and added footnote 5 in Table 17. ▪ Moved Soft Reset section to the *RC32312, RC32308 Programming Guide*. ▪ Completed other minor changes.
1.04	Feb 28, 2024	▪ Updated the description of the LOCK pin in Table 1 ▪ Updated the frequency tolerance values in Table 9. ▪ Updated footnotes 1 and 2 in Table 16. ▪ Updated Power Considerations. ▪ Added two new sections, Power-On Reset and Reset Controller and Soft Reset. ▪ Updated the slew rate in Overdriving the Crystal Interface.
1.03	Jan 22, 2024	▪ Updated Table 4 and Table 17. ▪ Updated the second paragraph of Overdriving the Crystal Interface.
1.02	Dec 6, 2023	▪ Updated Table 8 and Table 9. ▪ Updated the second paragraph of Overdriving the Crystal Interface.
1.01	Nov 21, 2023	▪ Updated the footnotes in Table 5. ▪ Reformatted Table 6 and updated its footnotes. ▪ Updated the footnotes in Table 7. ▪ Separated Table 8 into Table 8 and Table 9. ▪ Updated Table 10 and its footnotes. ▪ Updated the footnotes in Table 11 to Table 13. ▪ Updated Table 14 to Table 17 and their footnotes.
1.00	Oct 20, 2023	Initial release.

Package Outline Drawing

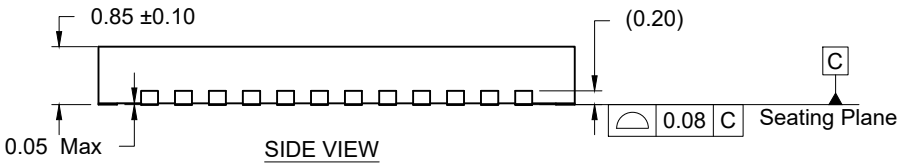
Package Code: NLG48P1
48-VFQFPN 7.0 x 7.0 x 0.85 mm Body, 0.5mm Pitch
PSC-4203-01, Revision: 03, Date Created: Apr 3, 2024



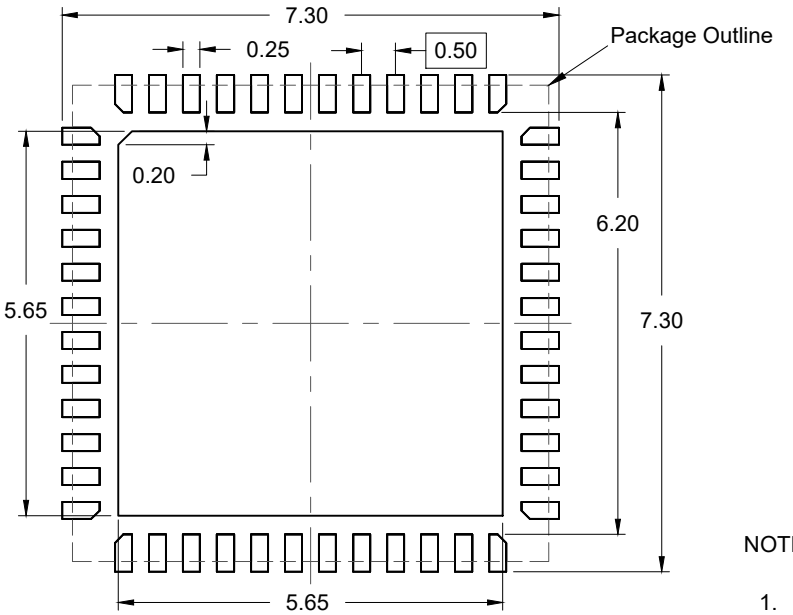
TOP VIEW



BOTTOM VIEW



SIDE VIEW



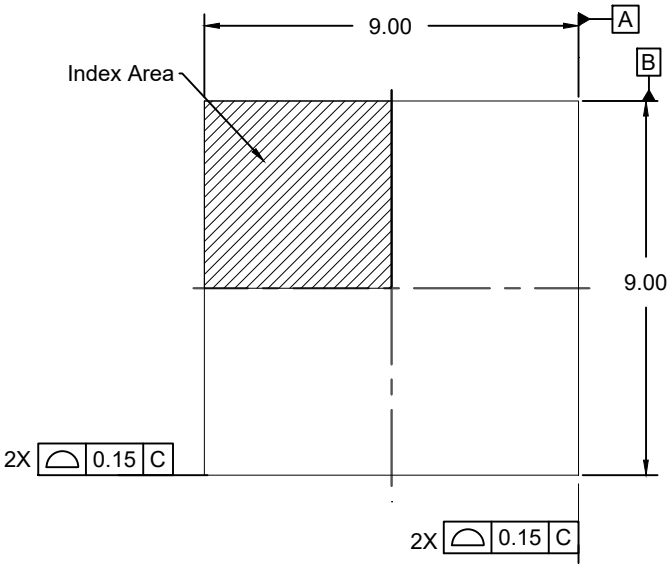
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

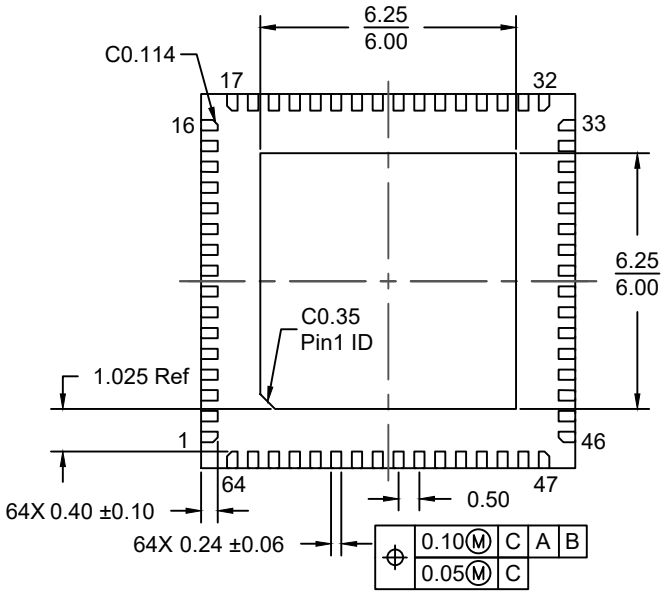
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

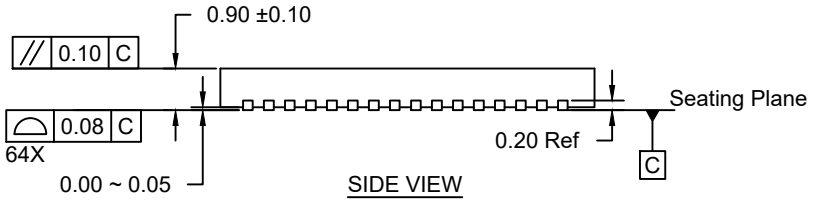
Package Code: NLG64P2
64-VFQFPN 9.0 x 9.0 x 0.9 mm Body, 0.50mm Pitch
PSC-4147-02, Revision: 03, Date Created: Jun 23, 2022



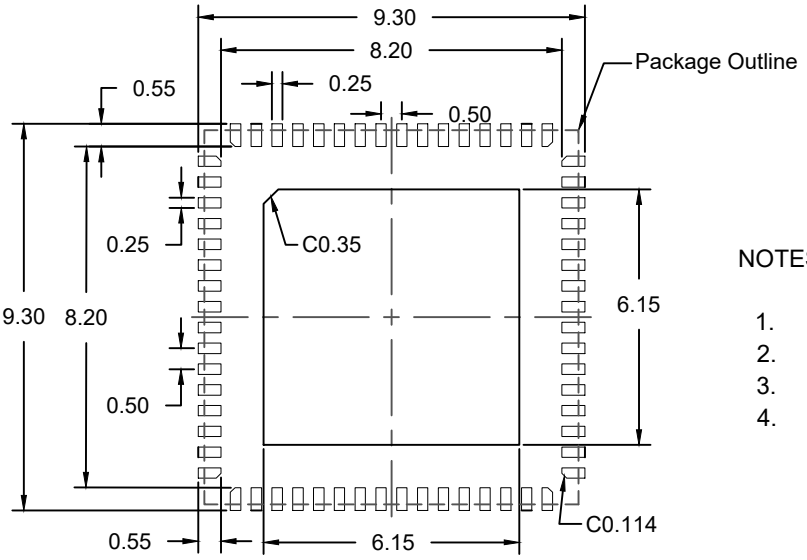
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
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