Data Sheet

AD7386-4/AD7387-4/AD7388-4

Single-Ended Input, Quad, Simultaneous Sampling, 16-Bit/14-Bit/12-Bit, SAR ADC

FEATURES

- 16-bit, 14-bit, and 12-bit ADC family
- Quad simultaneous sampling
- Single-ended analog inputs
- High throughput rate: 4 MSPS
- SNR (typical)
  - 84.7 dB (AD7386-4) at V_{REF} = 3.3 V
  - 82.4 dB (AD7387-4) at V_{REF} = 3.3 V
  - 73.7 dB (AD7388-4)
  - 92 dB with OSR = 8, V_{REF} = 3.3 V (AD7386-4)
- On-chip oversampling function
- 2-bit resolution boost
- Out of range indicator ($\overline{ALERT}$)
- INL (typical)
  - ±4 LSB (AD7386-4)
  - ±1 LSB (AD7387-4)
  - ±0.2 LSB (AD7388-4)
- High-speed serial interface
- Temperature range: −40°C to +125°C
- 2.5 V internal reference at 10 ppm/°C (maximum)
- 24-lead LFCSP

APPLICATIONS

- Motor control position feedback
- Motor control current sense
- Data acquisition systems
- Erbium doped fiber amplifier (EDFA) applications
- Traveling wave fault detection
- In-phase and quadrature demodulation

PRODUCT HIGHLIGHTS

1. Quad simultaneous sampling and conversion.
2. Pin-compatible product family.
3. High throughput rate, 4 MSPS at 16-bit, 14-bit, and 12-bit.
4. Space-saving, 24-lead LFCSP.
5. Integrated oversampling block to increase dynamic range, reduce noise, and reduce SCLK speed requirements.
6. Differential analog inputs with wide common-mode range.
7. Small sampling capacitor reduces amplifier drive burden.

FUNCTIONAL BLOCK DIAGRAM

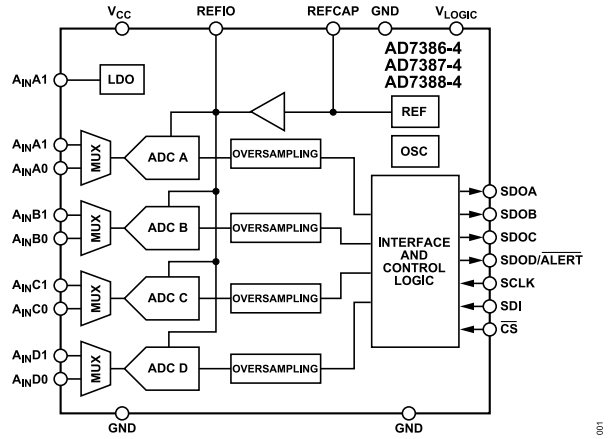

Figure 1.

GENERAL DESCRIPTION

The AD7386-4/AD7387-4/AD7388-4 are 16-bit, 14-bit, and 12-bit compatible, quad, simultaneous sampling, high-speed, successive approximation register (SAR), analog-to-digital converters (ADCs) operating from a 3.0 V to 3.3 V power supply with throughput rates up to 4 MSPS. The single-ended analog input accepts voltage from 0 V to V_{REF}, and is sampled and converted on the falling edge of $\overline{CS}$.

The AD7386-4/AD7387-4/AD7388-4 have on-chip oversampling blocks to improve dynamic range and reduce noise at lower bandwidths. The oversampling can boost up to two bits of added resolution. The REFIO pin can have a reference voltage (V_{REF}) of 2.5 V to 3.3 V.

The conversion process and data acquisition use standard control inputs, allowing easy interfacing to microprocessors or digital signal processors (DSPs). The conversion result can clock out simultaneously via 4-wire mode for faster throughput or via 1-wire serial mode when slower throughput is allowed. The device is compatible with 1.8 V, 2.5 V, and 3.3 V interfaces using the separate logic supply.

The AD7386-4/AD7387-4/AD7388-4 are available in a 24-lead lead frame chip scale package (LFCSP) and operate over a temperature range of −40°C to +125°C.

Rev. 0

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REVISION HISTORY

10/2023—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, external V_{REF} = 2.5 V to 3.3 V, f_{SAMPLE} = 4 MSPS, T_A = −40°C to +125°C, no oversampling enabled, unless otherwise noted.

Table 1. AD7386-4

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
THROUGHPUT					
Conversion Rate (f_{SAMPLE})					
Single-Channel Pair				4	MSPS
Alternating Channels	SEQ = 1			2	MSPS
DC ACCURACY					
No Missing Codes		16			Bits
Differential Nonlinearity (DNL) Error		−0.99	±0.6	+1.0	LSB
Integral Nonlinearity (INL) Error	External reference	−7.0	±4	+7.0	LSB
	Internal reference = 2.5 V		±3		LSB
Gain Error	External reference = 3.3 V	−0.08	±0.005	+0.08	% FS[1]
	Internal reference = 2.5 V		±0.015		% FS[1]
Gain Error Temperature Drift	External reference = 3.3 V	−5	±1	+5	ppm/°C
Gain Error Match			±0.01	+0.08	% FS
Offset Error	External reference = 3.3 V	−1	±0.07	+0.1	mV
	Internal reference		±0.055		mV
Offset Error Temperature Drift	External reference = 3.3 V	−8	±0.5	+8	µV/°C
Offset Error Match		−1.1	±0.2	+1.1	mV
AC ACCURACY	Input frequency (f_{IN}) = 1 kHz				
Dynamic Range	V_{REF} = 3.3 V		86		dB
	V_{REF} = 2.5 V		84.5		dB
Oversampled Dynamic Range	OSR = 4×, RES = 1 (decimal)		89		dB
Signal-to-Noise Ratio (SNR)	V_{REF} = 3.3 V, V_{CC} = 3.3 V	80.5	84.7		dB
	V_{REF} = 2.5 V (internal)		81.7		dB
	Rolling average OSR = 8×, RES = 1 (decimal)		92		dB
	f_{IN} = 100 kHz		83.5		dB
Spurious-Free Dynamic Range (SFDR)			−103		dB
Total Harmonic Distortion (THD)			−100		dB
	f_{IN} = 100 kHz		−89		dB
Signal-to-Noise-and-Distortion (SINAD) Ratio	V_{REF} = 3.3 V, V_{CC} = 3.3 V	80	84.5		dB
	V_{REF} = 2.5 V (internal)		81.3		dB
Channel to Channel Isolation			−120		dB
Channel to Channel Memory			−95		dB
POWER SUPPLIES					
I_{VCC}					
Normal Mode (Operational)			39	45	mA
Power Dissipation					
P_{TOTAL}			165	191	mW
P_{VCC} Normal Mode (Operational)			141	162	mW

[1] These specifications include full temperature range variation, but they do not include the error contribution from the external reference.

SPECIFICATIONS

Table 2. AD7387-4

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
THROUGHPUT					
Conversion Rate (f_{SAMPLE})					
Single-Channel Pair			4		MSPS
Alternating Channels	SEQ = 1		2		MSPS
DC ACCURACY					
No Missing Codes		14			Bits
DNL Error		−0.99	+0.4	+1	LSB
INL Error	External reference	−1.8	+1.0	+1.8	LSB
	Internal reference = 2.5 V		±0.75		LSB
Gain Error	External reference	−0.08	±0.005	+0.08	% FS[1]
	Internal reference		±0.015		% FS[1]
Gain Error Temperature Drift	External reference = 3.3 V	−5	±0.3	+5	ppm/°C
Gain Error Match			±0.01	+0.08	% FS
Offset Error	External reference = 3.3 V	−1	±0.1	+1	mV
	Internal reference = 2.5 V		±0.055		mV
Offset Error Temperature Drift	External reference = 3.3 V	−8	±1	+8	µV/°C
Offset Error Match			±0.2	+1.1	mV
AC ACCURACY	Input frequency (f_{IN}) = 1 kHz				
Dynamic Range	V_{REF} = 3.3 V		84		dB
	V_{REF} =2.5 V (internal)		83		dB
Oversampled Dynamic Range	OSR = 4×, RES = 1 (decimal)		87.2		dB
SNR	V_{REF} = 3.3 V, V_{CC} = 3.3 V	80	82.4		dB
	V_{REF} = 2.5 V (internal)		80.4		dB
	Rolling average OSR = 8×, RES = 1 (decimal)		90		dB
	f_{IN} = 100 kHz		81		dB
SFDR			−102		dB
THD			−100		dB
	f_{IN} = 100 kHz		−88		dB
SINAD Ratio	V_{REF} = 3.3 V, V_{CC} = 3.3 V	79.8	82.3		dB
	V_{REF} = 2.5 V (internal)		79.2		dB
Channel to Channel Isolation			−120		dB
Channel to Channel Memory			−95		dB
POWER SUPPLIES					
I_{VCC}					
Normal Mode (Operational)			39	45	mA
Power Dissipation					
P_{TOTAL}			165	191	mW
P_{VCC} Normal Mode (Operational)			141	162	mW

[1] These specifications include full temperature range variation, but they do not include the error contribution from the external reference.

Table 3. AD7388-4

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		12			Bits
THROUGHPUT					
Conversion Rate (f_{SAMPLE})					
Single-Channel Pair				4	MSPS
Alternating Channels	SEQ = 1			2	MSPS

SPECIFICATIONS

Table 3. AD7388-4 (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC ACCURACY					
No Missing Codes		12			Bits
DNL Error		−0.5	±0.25	+0.5	LSB
INL Error		−0.75	±0.2	+0.75	LSB
Gain Error		−0.08	±0.007	+0.08	% FS[1]
Gain Error Temperature Drift	External reference = 3.3 V	−6.5	±1	+6.5	ppm/°C
Gain Error Match			±0.018	+0.1	% FS
Offset Error		−2	±0.3	+2	mV
Offset Error Temperature Drift	External reference = 3.3 V	−12	±1	+12	µV/°C
Offset Error Match		−2	±0.35	+2	mV
AC ACCURACY	Input frequency (f_{IN}) = 1 kHz				
Dynamic Range	V_{REF} = 3.3 V, V_{CC} = 3.3 V		74		dB
					dB
Oversampled Dynamic Range	OSR = 4×, RES = 1 (decimal)		76.6		dB
SNR	V_{REF} = 3.3 V	73	73.7		dB
	V_{REF} = 2.5 V (internal)		73.3		dB
	Rolling average OSR = 8×, RES = 1 (decimal)		80		dB
	f_{IN} = 100 kHz		73		dB
SFDR			−100		dB
THD			−98		dB
	f_{IN} = 100 kHz		−90		dB
SINAD Ratio	V_{REF} = 3.3 V, V_{CC} = 3.3 V	73	73.7		dB
	V_{REF} = 2.5 V (internal)	71.8	73.1		dB
Channel to Channel Isolation			−120		dB
Channel to Channel Memory			−95		dB
POWER SUPPLIES					
I_{VCC}					
Normal Mode (Operational)			39	45	mA
Power Dissipation					
P_{TOTAL}			165	191	mW
P_{VCC} Normal Mode (Operational)			141	162	mW

[1] These specifications include full temperature range variation, but they do not include the error contribution from the external reference.

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, V_{REF} = 2.5 V to 3.3 V, T_A = −40°C to +125°C, no oversampling enabled, unless otherwise noted.

Table 4. All Devices

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT					
Voltage Range		0		+V_{REF}	V
DC Leakage Current			0.1	1	µA
Input Capacitance	Track mode		18		pF
	Hold mode		5		pF
SAMPLING DYNAMICS					
Input Bandwidth	At −0.1 dB		6		MHz
	At −3 dB		24		MHz
Aperture Delay			2		ns
Aperture Delay Match			310		ps
Aperture Jitter			20		ps

SPECIFICATIONS

Table 4. All Devices (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE INPUT					
V_{REF} Input Voltage Range	External reference	2.49		3.4	V
V_{REF} Input Current	External reference		0.9	1.2	mA
V_{REF} Output Voltage	At 25°C	2.495	2.5	2.505	V
V_{REF} Temperature Coefficient			2	10	ppm/°C
V_{REF} Regulation					
Line			−40		ppm/V
Load			−34		ppm/mA
V_{REF} Noise			7		μVrms
DIGITAL INPUTS (SCLK, SDI, $\overline{CS}$)					
Logic Levels					
Input Voltage Low (V_{IL})	V_{LOGIC} < 2.3 V			0.45	V
	V_{LOGIC} ≥ 2.3 V			0.7	V
Input Voltage High (V_{IH})	V_{LOGIC} < 2.3 V	V_{LOGIC} − 0.45 V			V
	V_{LOGIC} ≥ 2.3 V	0.8 × V_{LOGIC}			V
Input Current Low (I_{IL})		−1		+1	μA
Input Current High (I_{IH})		−1		+1	μA
DIGITAL OUTPUTS (SDOA, SDOB, SDOC, SDOD/$\overline{ALERT}$)					
Output Coding			Straight binary		Bits
Output Voltage Low (V_{OL})	Current sink (I_{SINK}) = 300 μA			0.4	V
Output Voltage High (V_{OH})	Current source (I_{SOURCE}) = −300 μA	V_{LOGIC} − 0.3			V
Floating State Leakage Current				±1	μA
Floating State Output Capacitance			10		pF
POWER SUPPLIES					
V_{CC}		3.0	3.3	3.6	V
	External reference = 3.3 V	3.3		3.6	V
V_{LOGIC}		1.65		3.6	V
V_{CC} Supply Current (I_{VCC})					
Normal Mode (Static)			2.6	3.3	mA
Shutdown Mode			98	200	μA
V_{LOGIC} Current (I_{VLOGIC})	Analog inputs at positive full scale				
Normal Mode (Static)			146	400	nA
Normal Mode (Operational)			6.6	8	mA
Shutdown Mode			47	400	nA
Power Dissipation					
V_{CC} Power (P_{VCC})					
Normal Mode (Static)			9.3	11.5	mW
Shutdown Mode			375	720	μW
V_{LOGIC} Power (P_{VLOGIC})	Analog inputs at positive full scale				
Normal Mode (Static)			0.53	1.5	μW
Normal Mode (Operational)			24	29	mW
Shutdown Mode			0.17	1.5	μW

SPECIFICATIONS

TIMING SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, V_{REF} = 2.5 V to 3.3 V, T_A = −40°C to +125°C, unless otherwise noted. When referencing a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed such as $\overline{ALERT}$. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

Table 5.

Parameter	Min	Typ	Max	Unit	Description
t_{CYC}					Time between conversions
	250			ns	4 MSPS
	500			ns	Alternating conversion channels
t_{SCLKED}	0.5			ns	$\overline{CS}$ falling edge to first serial clock (SCLK) falling edge
t_{SCLK}	12.5			ns	SCLK period
t_{SCLKH}	5.5			ns	SCLK high time
t_{SCLKL}	5.5			ns	SCLK low time
t_{CSH}	20			ns	$\overline{CS}$ pulse width
t_{QUIET}	20			ns	Interface quiet time prior to conversion
t_{SDOEN}					$\overline{CS}$ low to SDOA, SDOB, SDOC, and SDOD enabled
			5.58	ns	V_{LOGIC} > 2.25 V
			8	ns	1.65 V < V_{LOGIC} < 2.25 V
t_{SDOH}	3			ns	SCLK rising edge to SDOA, SDOB, SDOC, and SDOD hold time
t_{SDOS}					SCLK rising edge to SDOA, SDOB, SDOC, and SDOD setup time
			6	ns	V_{LOGIC} > 2.25 V
			8	ns	1.65 V < V_{LOGIC} < 2.25 V
t_{SDOT}			8	ns	$\overline{CS}$ rising edge to SDOA, SDOB, SDOC, and SDOD high impedance
t_{SDIS}	4			ns	SDI setup time prior to SCLK falling edge
t_{SDIH}	4			ns	SDI hold time after SCLK falling edge
t_{SCLKCS}	0			ns	SCLK rising edge to $\overline{CS}$ rising edge
$t_{CONVERT}$			190	ns	Conversion time
$t_{ACQUIRE}$	110			ns	Acquire time
t_{RESET}		250		ns	Valid time to start conversion after soft reset
		800		ns	Valid time to start conversion after hard reset
$t_{POWERUP}$					Supply active to conversion
			5	ms	First conversion allowed
			11	ms	Settled to within 1% with internal reference
			5	ms	Settled to within 1% with external reference
$t_{REGWRITE}$			5	ms	Supply active to register read write access allowed
$t_{STARTUP}$					Exiting shutdown mode to conversion
			10	µs	Settled to within 1% with external reference
$t_{CONVERT0}$	6	8	10	ns	Conversion time for first sample in oversampling (OS) normal mode
$t_{CONVERTx}$					Conversion time for x^{th} sample in OS normal mode, 4 MSPS, 16-bit devices
	$t_{CONVERT0}$ + (320 × (x – 1))			ns	For AD7386-4, at 3 MSPS
	$t_{CONVERT0}$ + (250 × (x – 1))			ns	For AD7387-4 and AD7388-4, at 4 MSPS
t_{ALERTS}			220	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ indication
t_{ALERTC}			10	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ clear
t_{ALERTS_NOS}			20	ns	Time from internal conversion with exceeded threshold to $\overline{ALERT}$ indication

SPECIFICATIONS

Timing Diagrams

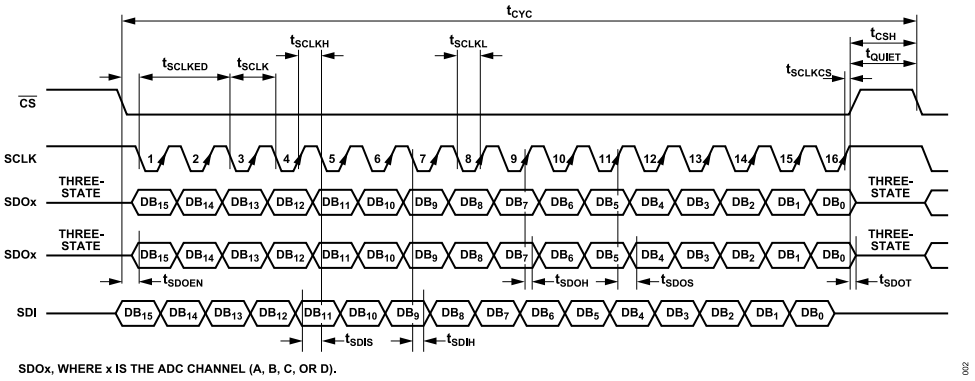


Figure 2. Serial Interface Timing Diagram

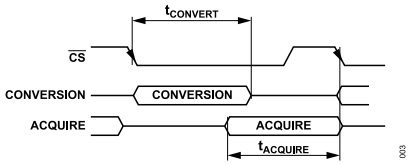


Figure 3. Internal Conversion Acquire Timing

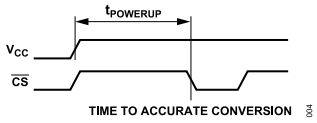


Figure 4. Power-Up Time to Conversion

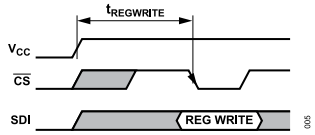


Figure 5. Power-Up Time to Register Read Write Access

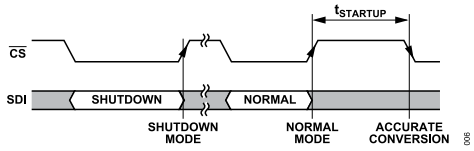


Figure 6. Shutdown Mode to Normal Mode Timing

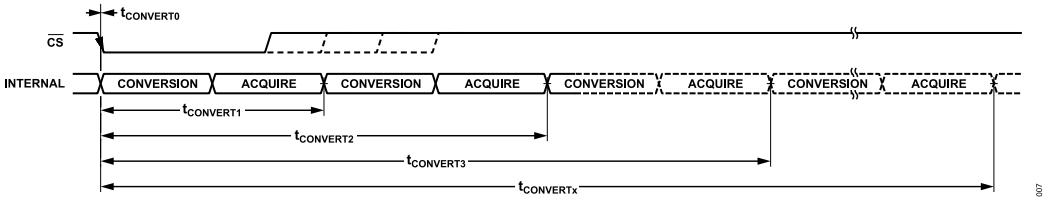


Figure 7. Conversion Timing During OS Normal Mode

SPECIFICATIONS

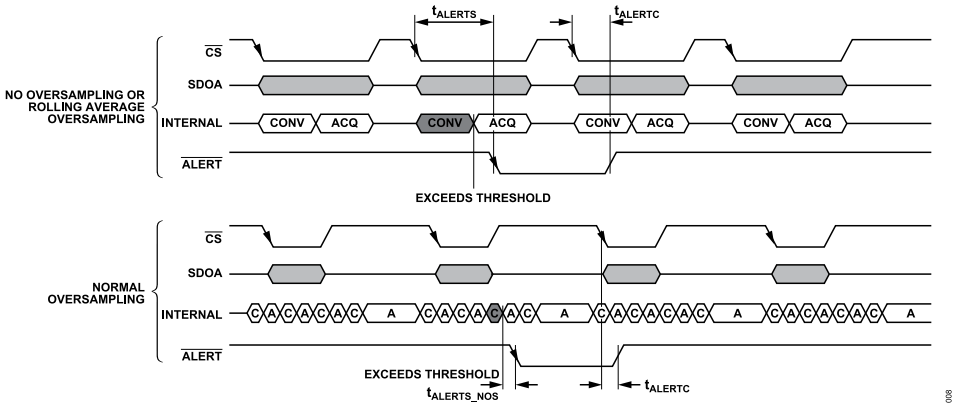


Figure 8. $\overline{\text{ALERT}}$ Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
V_{CC} to GND	−0.3 V to +4 V
V_{LOGIC} to GND	−0.3 V to +4 V
Analog Input Voltage to GND	−0.3 V to V_{REF} + 0.3 V, or V_{CC} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
REFIO Input to GND	−0.3 V to V_{CC} + 0.3 V
Input Current to any Pin Except Supplies	±10 mA
Temperature	
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_{JMAX})	150°C
Pb-Free Soldering Reflow Temperature	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-25[1]	48.4	0.43[1]	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESDS1.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charge device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD7386-4, AD7387-4, and AD7388-4

Table 8. AD7386-4/AD7387-4/AD7388-4, 24-lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

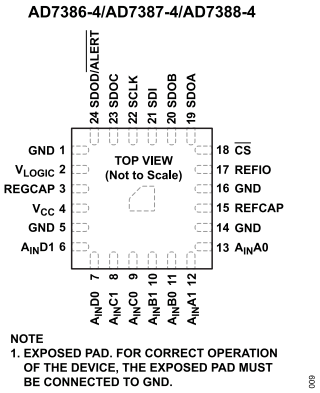


Figure 9. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 14, 16	GND	Ground Reference Point. These pins are the ground reference points for all circuitry on the device.
2	V_{LOGIC}	Logic Interface Supply Voltage, 1.65 V to 3.6 V. Decouple this pin to GND with a 1 µF capacitor.
3	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this pin to GND with a 1 µF capacitor. The voltage at this pin is 1.9 V typical.
4	V_{CC}	Power Supply Input Voltage, 3.0 V to 3.6 V. Decouple this pin to GND using a 1 µF capacitor.
6, 7	$A_{IN}D1$, $A_{IN}D0$	Analog Inputs of ADC D. These are 2-channel multiplexed single-ended inputs.
8, 9	$A_{IN}C1$, $A_{IN}C0$	Analog Inputs of ADC C. These are 2-channel multiplexed single-ended inputs.
10, 11	$A_{IN}B1$, $A_{IN}B0$	Analog Inputs of ADC B. These are 2-channel multiplexed single-ended inputs.
12, 13	$A_{IN}A1$, $A_{IN}A0$	Analog Inputs of ADC A. These are 2-channel multiplexed single-ended inputs.
15	REFCAP	Decoupling Capacitor Pin for Band Gap Reference. Decouple REFCAP to GND with a 0.1 µF capacitor. The voltage at REFCAP is 2.5 V typical.
17	REFIO	Reference Input and Output. The on-chip reference of 2.5 V is available as an output on REFIO for external use if the device is configured accordingly. Alternatively, an external reference of 2.5 V to 3.3 V can be connected to the REFIO pin as input. Set the REFSEL bit in the Configuration 1 register to 1 when using the external reference and apply the REFSEL bit after V_{CC} and V_{LOGIC}. Decoupling is required on REFIO for both the internal and external reference options. Apply a 1 µF capacitor from REFIO to GND.
18	$\overline{CS}$	Chip Select Input. Active low logic input. This input provides the dual function of initiating conversions on the AD7386-4/AD7387-4/AD7388-4 and framing the serial data transfer.
19	SDOA	Serial Data Output A. This pin functions as a serial data output pin to access the conversion results and register contents.
20	SDOB	Serial Data Output B. This pin functions as a serial data output pin to access the conversion results.
21	SDI	Serial Data Input. This input provides the data written to the on-chip control registers.
22	SCLK	Serial Clock Input. This SCLK input is for data transfers to and from the ADC.
23	SDOC	Serial Data Output C. This pin functions as a serial data output pin to access the conversion results and register contents.
24	SDOD/$\overline{ALERT}$	Serial Data Output D/Alert Indication Output. This pin can operate as a serial data output pin or alert indication output.
		SDOD. This pin functions as a serial data output pin to access the conversion results.
		$\overline{ALERT}$. This pin operates as an alert pin going low to indicate that a conversion result has exceeded a configured threshold.
	EPAD	Exposed Pad. For correct operation of the device, the exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = V_{LOGIC} = 3.3 V, throughput rate = 4 MSPS, external V_{REF} = 2.5 V and 3.3 V, external SCLK = 80 MHz, unless otherwise noted.

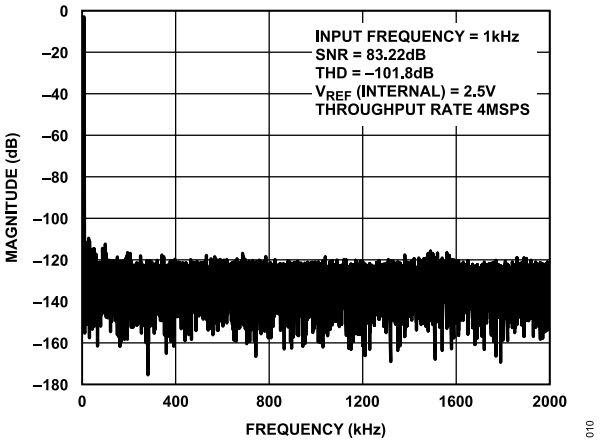


Figure 10. Fast Fourier Transform (FFT), AD7386-4 Internal V_{REF} = 2.5 V

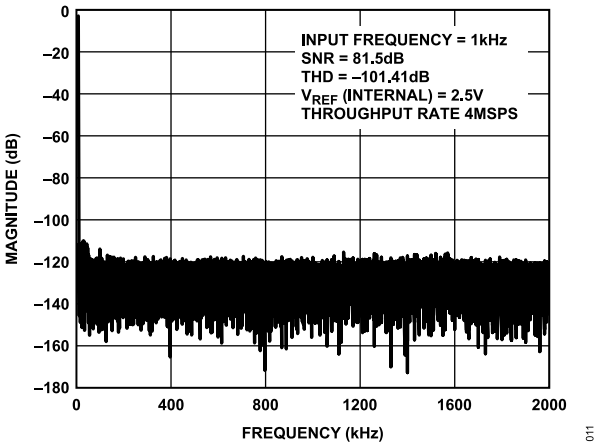


Figure 11. FFT, AD7387-4 Internal V_{REF} = 2.5 V

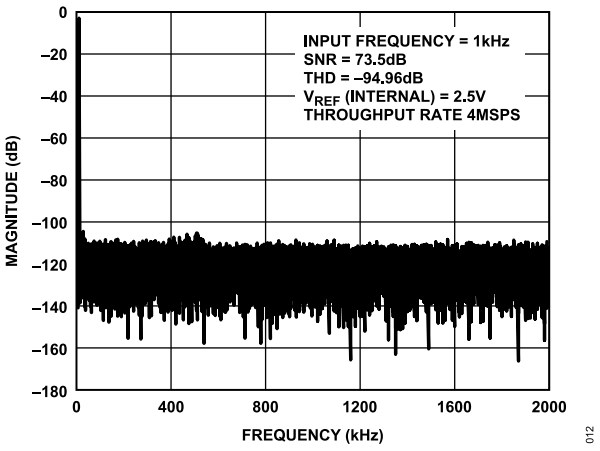


Figure 12. FFT, AD7388-4 Internal V_{REF} = 2.5 V

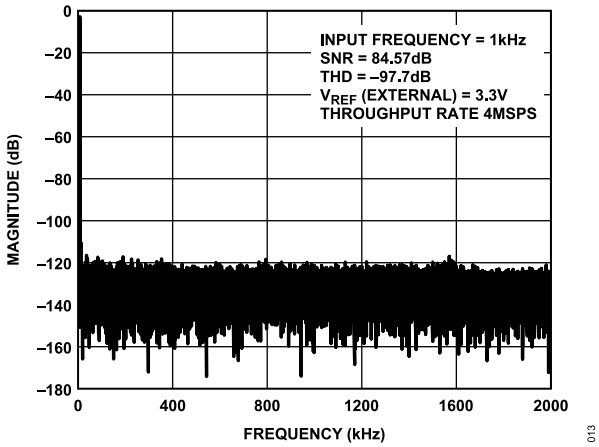


Figure 13. FFT, AD7386-4 External V_{REF} = 3.3 V

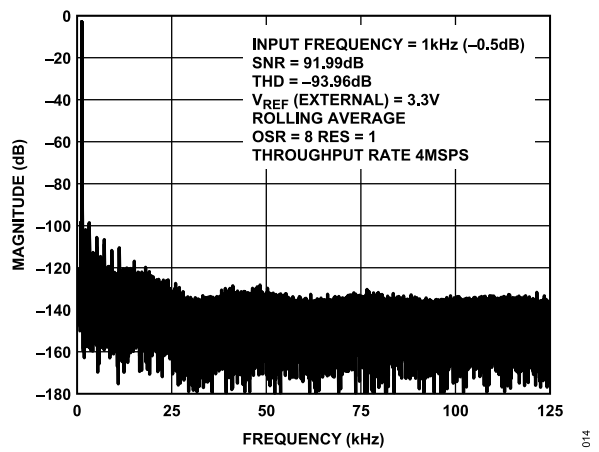


Figure 14. FFT, AD7386-4 Oversampling, External V_{REF} = 3.3 V

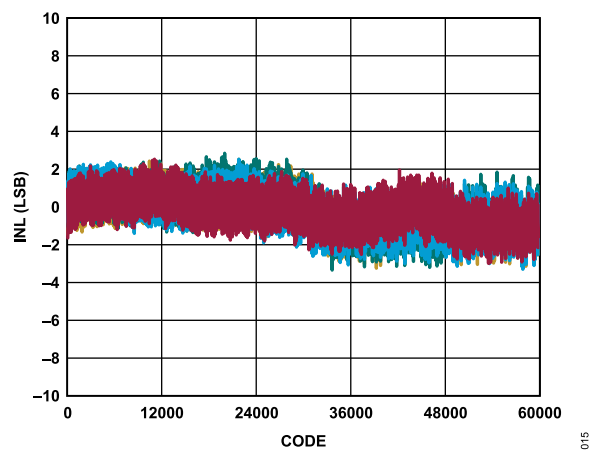


Figure 15. INL vs. Code

TYPICAL PERFORMANCE CHARACTERISTICS

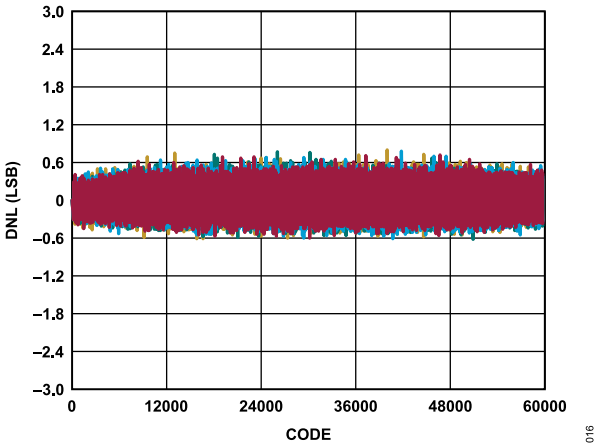


Figure 16. DNL vs. Code

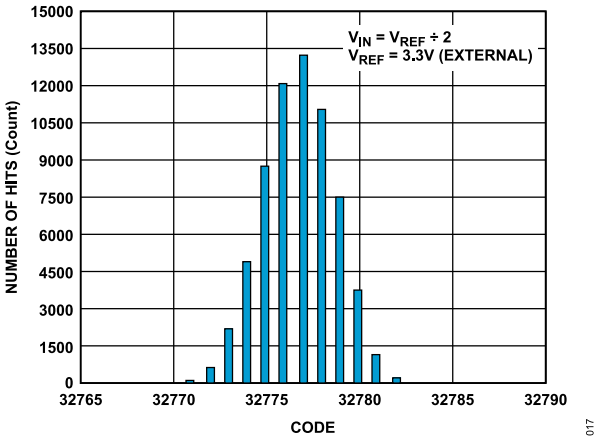


Figure 17. DC Histogram

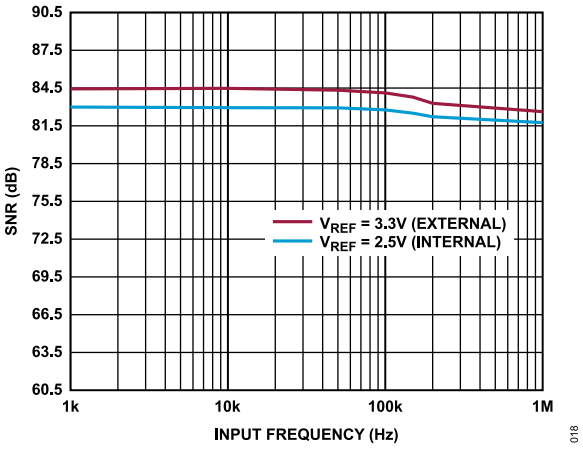


Figure 18. SNR vs. Input Frequency (AD7386-4)

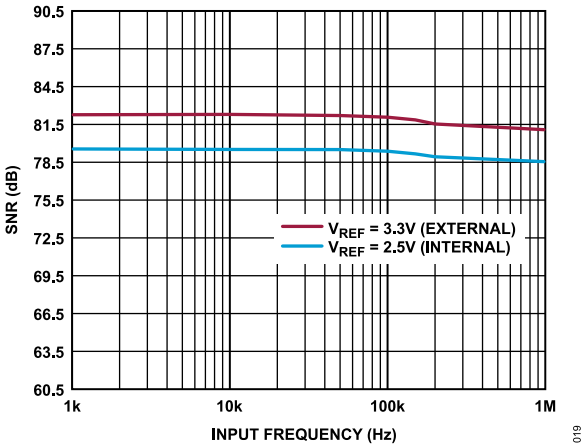


Figure 19. SNR vs. Input Frequency (AD7387-4)

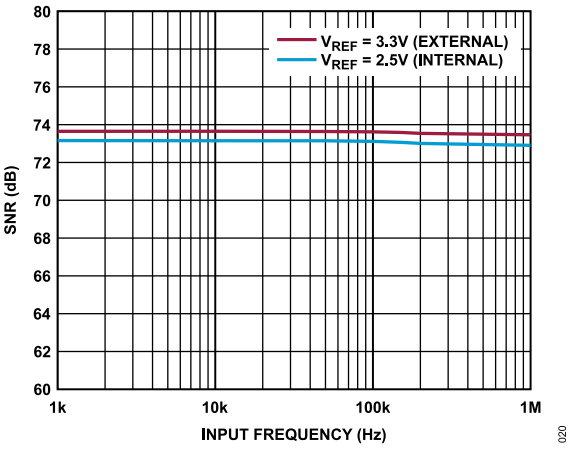


Figure 20. SNR vs. Input Frequency (AD7388-4)

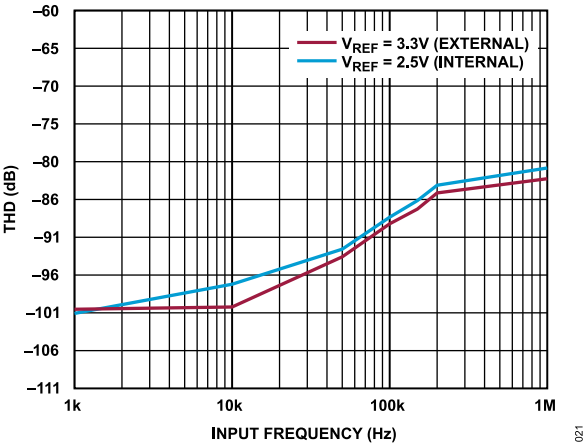


Figure 21. THD vs. Input Frequency (AD7386-4)

TYPICAL PERFORMANCE CHARACTERISTICS

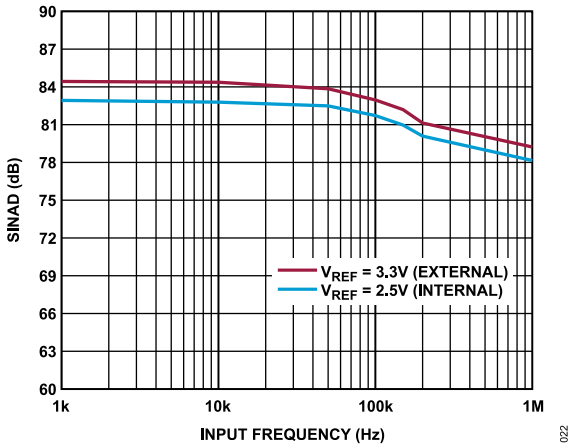


Figure 22. SINAD vs. Input Frequency (AD7386-4)

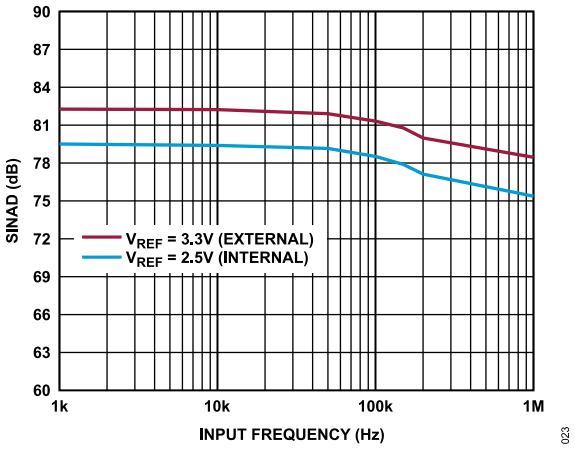


Figure 23. SINAD vs. Input Frequency (AD7387-4)

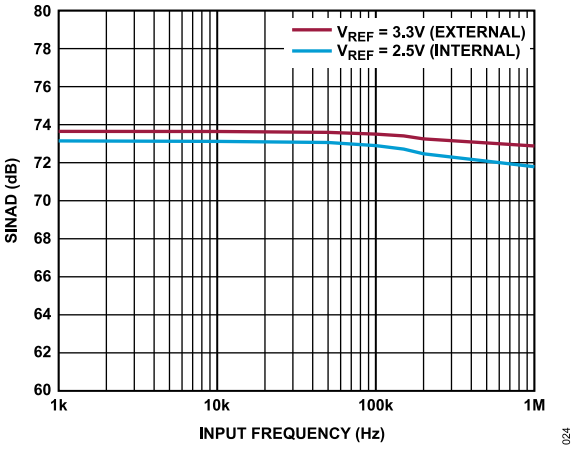


Figure 24. SINAD vs. Input Frequency (AD7388-4)

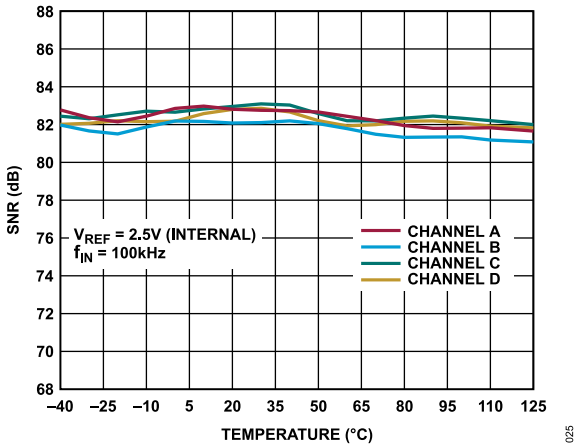


Figure 25. SNR vs. Temperature

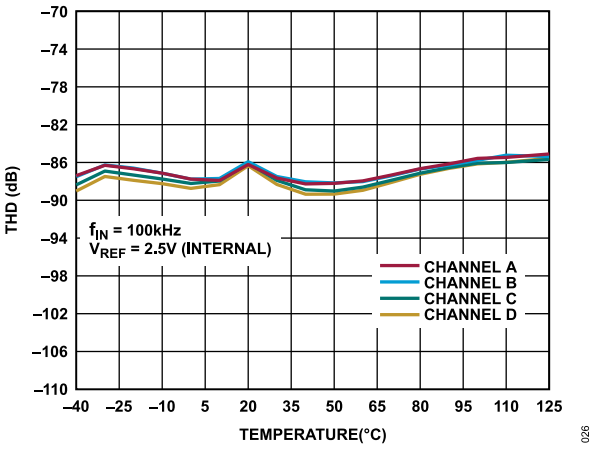


Figure 26. THD vs. Temperature

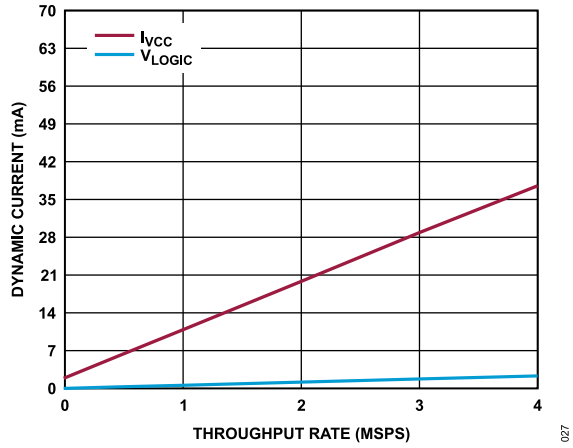


Figure 27. Dynamic Current vs. Throughput Rate

TYPICAL PERFORMANCE CHARACTERISTICS

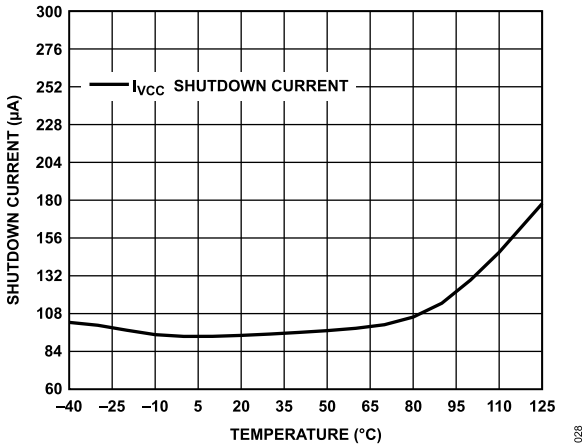


Figure 28. Shutdown Current vs. Temperature

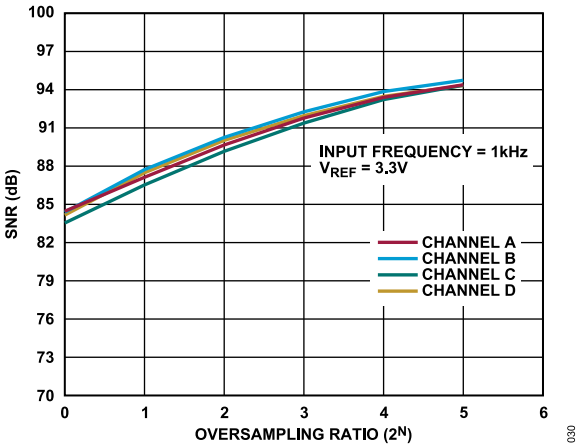


Figure 30. Normal Averaging Oversampling

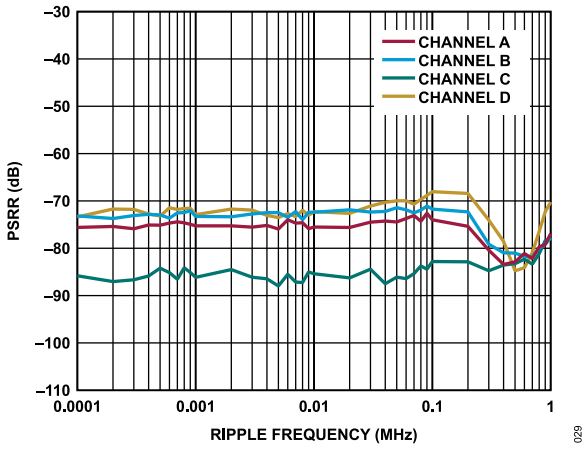


Figure 29. PSRR vs. Ripple Frequency

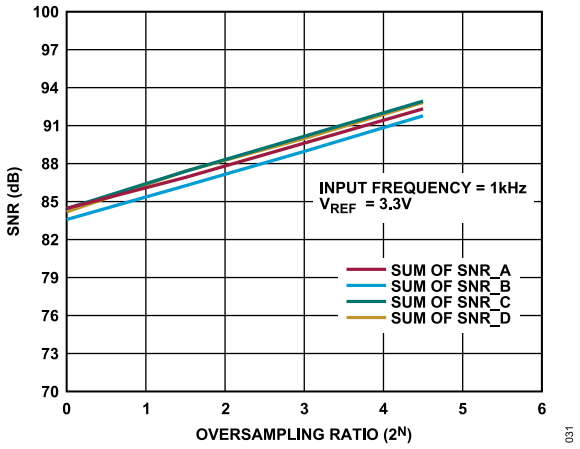


Figure 31. Rolling Average Oversampling

TERMINOLOGY

Differential Nonlinearity (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs at a level ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Gain Error

The first transition (from 100 … 000 to 100 … 001) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage at a level 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Temperature Drift

Gain error temperature drift is the gain error change due to a temperature change of 1°C.

Gain Error Match

Gain error match is the difference in negative full-scale error between the input channels and the difference in positive full-scale error between the input channels.

Offset Error

The first transition must occur at a level ½ LSB above analog ground. Offset error is the deviation of the actual transition from that analog ground point.

Offset Error Temperature Drift

Offset error temperature drift is the offset error change due to a temperature change of 1°C.

Offset Error Match

Offset error match is the difference in offset error between the input channels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the RMS amplitude of the input signal and the peak spurious signal.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first five harmonic components to the RMS value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD)

SINAD is the ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding DC. The value for SINAD is expressed in decibels.

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in the full-scale transition point due to the change in the power supply voltage from the nominal value. PSRR is the ratio of power in the ADC output at full-scale frequency, f, to the power of a 100 mVp-p sine wave applied to the V_{CC} supply of the ADC of ripple frequency, fr.

$$PSRR\ (\text{dB}) = 10\log(Pf/Pfr) \quad (1)$$

where:
Pf is equal to the power at *f* in the ADC output.
Pfr is equal to the power at *fr* coupled into the V_{CC} supply.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the $\overline{CS}$ input and when the input signal is held for a conversion.

Aperture Jitter

Aperture jitter is the variation in aperture delay.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7386-4/AD7387-4/AD7388-4 are high-speed, quad, single-ended 16-bit, 14-bit, and 12-bit SAR ADCs. These devices operate from a 3.0 V to 3.6 V power supply and features throughput rates up to 4 MSPS.

The AD7386-4/AD7387-4/AD7388-4 contain four successive approximation ADCs and a serial interface with four separate data output pins. These devices are housed in a 24-lead LFCSP, offering the user considerable space-saving advantages over alternative solutions.

Data is accessed from the device via the serial interface. The interface can be operated with two, four, or one serial output. The AD7386-4/AD7387-4/AD7388-4 have an on-chip, 2.5 V internal reference. If an external reference is desired, the internal reference can be disabled and an external V_{REF} value ranging from 2.5 V to 3.3 V can be applied. The analog input range for the AD7386-4/AD7387-4/AD7388-4 is 0 V to V_{REF}.

The AD7386-4/AD7387-4/AD7388-4 feature on-chip oversampling blocks to improve performance. Normal averaging and rolling average OS modes are available. Power-down options to allow power saving between conversions are available. Configuration of the device is implemented via the standard serial interface, as described in the Interface section.

CONVERTER OPERATION

The AD7386-4/AD7387-4/AD7388-4 have four successive approximation ADCs, each based around two capacitive DACs. Figure 32 and Figure 33 show simplified schematics of one of these ADCs in acquisition and conversion phases, respectively. The ADC comprises control logic, an SAR, and two capacitive DACs. In Figure 32 (the acquisition phase), SW2 is closed, SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor (C_S) arrays can acquire the signal on the input.

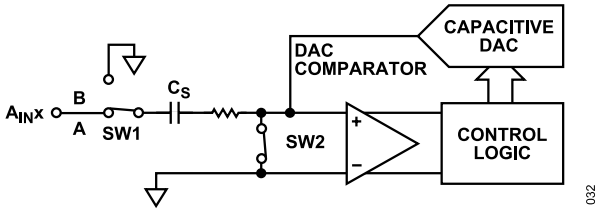


Figure 32. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 33), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. Input is disconnected when the conversion begins. The control logic and charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

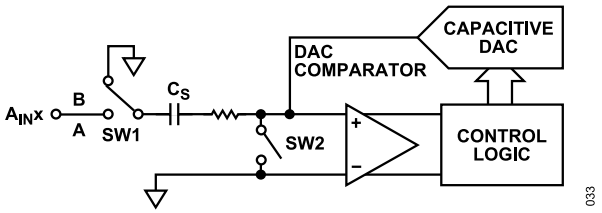


Figure 33. ADC Conversion Phase

ANALOG INPUT STRUCTURE

Figure 34 shows the equivalent circuit of the analog input structure of the AD7386-4/AD7387-4/AD7388-4. The two diodes provide ESD protection for the analog inputs, $A_{IN}x$. Ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the device.

The C1 capacitors in Figure 34 are typically 3 pF and can primarily be attributed to pin capacitance. The R1 resistors are combined components made up of the on resistance of the switches. The value of these resistors is typically about 200 Ω. The C2 capacitors are the ADC sampling capacitors with a typical capacitance of 15 pF.

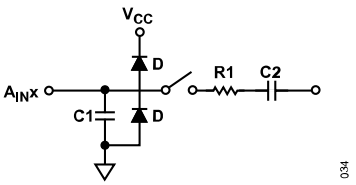


Figure 34. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

ADC TRANSFER FUNCTION

The AD7386-4/AD7387-4/AD7388-4 use a 2.5 V to 3.3 V reference. The AD7386-4/AD7387-4/AD7388-4 convert the voltage of the analog inputs ($A_{IN}x0$ and $A_{IN}x1$) into a digital output, where x are ADC Channel A, Channel B, Channel C, and Channel D.

The conversion result is MSB first, straight binary. The LSB size is $(V_{REF})/2^N$, where N is the ADC resolution. The ADC resolution is determined by the resolution of the device chosen and if resolution boost mode is enabled. Table 10 outlines the LSB size expressed in microvolts for different resolutions and V_{REF} options.

The ideal transfer characteristic of the AD7386-4/AD7387-4/AD7388-4 is shown in Figure 35.

THEORY OF OPERATION

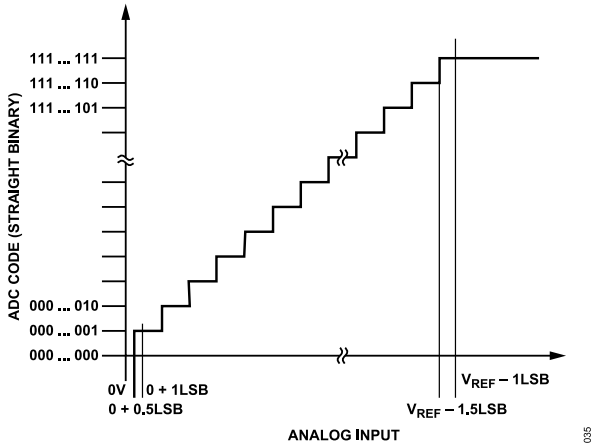


Figure 35. ADC Ideal Transfer Function (FSR = Full-Scale Range)

Table 10. LSB Size

Resolution (Bits)	2.5 V Reference (µV)	3.3 V Reference (µV)
12	610.3	805.7
14	152.6	201.4
16	38.1	50.4
18	9.5	12.6

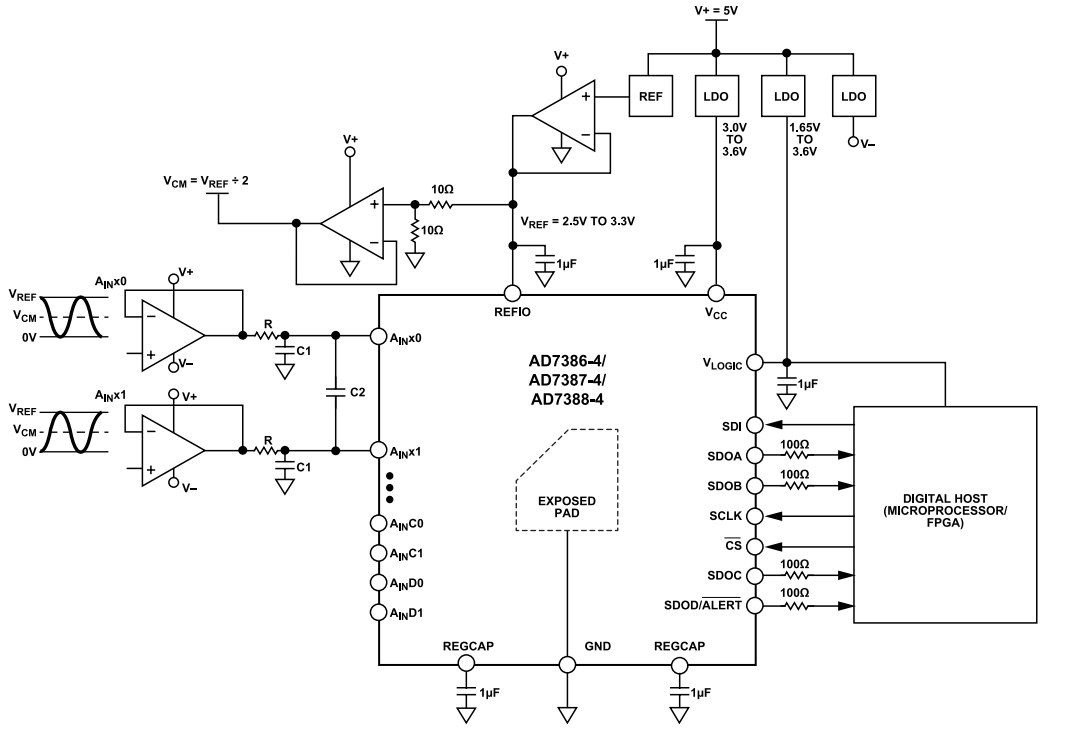


Figure 36. Typical Application Circuit

APPLICATIONS INFORMATION

Figure 36 shows an example of a typical application circuit for the AD7386-4/AD7387-4/AD7388-4. Decouple the V_{CC} pin, the V_{LOGIC} pin, the REGCAP pin, the REFCAP pin, and the REFIO pin with suitable decoupling capacitors as shown in Figure 36. The exposed pad is a ground reference point for circuitry on the device and must be connected to the board ground.

An RC filter must be placed on the analog inputs to ensure optimal performance is achieved. In a typical application, R = 33 Ω and C1 = 330 pF are recommended. These RC combinations must be the same for all channels of the AD7386-4/AD7387-4/AD7388-4.

The eight single-ended channels (4:2) of the AD7386-4/AD7387-4/AD7388-4 can accept an input voltage range from 0 V to V_{REF} and convert digitally. These analog input pins ($A_{IN}x$) can easily be driven with an amplifier. See Table 11 for the recommended driver amplifiers that can best fit and add value to the application.

The performance of the AD7386-4/AD7387-4/AD7388-4 can be impacted by noise on the digital interface. This impact is dependent on board layout and design. Keep a minimal distance of the digital line to the digital interface or place a 100 Ω resistor in series with and close to the SDOA pin, the SDOB pin, the SDOC pin, and the SDOD/$\overline{\text{ALERT}}$ pin to reduce noise from the digital interface coupling of the AD7386-4/AD7387-4/AD7388-4.

The V_{REF} of the AD7386-4/AD7387-4/AD7388-4 ranges from 2.5 V to 3.3 V. The ADR4533 or the ADR4525 is an ultra-low noise, high accuracy voltage reference recommended to drive the AD7386-4/AD7387-4/AD7388-4 REFIO pin. A 1 µF reservoir capacitor is recommended to be connected between the REFIO pin and the ground. When using this external V_{REF} in another circuit within the application, for example, as a common-mode voltage for the driver amplifier, it is recommended to use a buffer amplifier like the ADA4807-2 for a stable reference.

POWER SUPPLY

For a typical application, the AD7386-4/AD7387-4/AD7388-4 circuitry shown in Figure 36 can be driven from a 5 V (V+) supply to power the system. The 5 V (V+) can be supplied from the ADP7104. The ADC driver can be supplied by a +5 V (V+) and a −2.5 V (V−) source derived from the inverting charge pump, the ADP5600, that converts +5 V to −5 V, then to the ADP7182 for the low noise voltage regulator to output −2.5 V. Two independent power supply sources are derived from a low dropout (LDO) regulator to power the V_{CC} supply for the analog circuitry and the V_{LOGIC} supply for the digital interface of the AD7386-4/AD7387-4/AD7388-4. A very low quiescent current LDO regulator like the ADP166 is a suitable supply with a fixed output voltage range from 1.2 V to 3.3 V for typical V_{CC} and V_{LOGIC} levels. The V_{CC} supply and the V_{LOGIC} supply must be decoupled separately with a 1 µF capacitor, placed close to the AD7386-4/AD7387-4/AD7388-4 and connected using short and wide traces, to provide low impedance paths and reduce the glitches in the power supply lines. Additionally, an internal LDO regulator supplies the AD7386-4/AD7387-4/AD7388-4. The on-chip regulator provides a 1.9 V supply only for internal use on the device. Decouple the REGCAP pin with a 1 µF capacitor to GND with short and wide traces and place the capacitor close to the AD7386-4/AD7387-4/AD7388-4 REGCAP pin and the GND pin.

Power-Up

The AD7386-4/AD7387-4/AD7388-4 are not easily damaged by power supply sequencing. V_{CC} and V_{LOGIC} can be applied in any sequence. The external reference must be applied after V_{CC} and V_{LOGIC} are applied. Analog and digital signals must be applied after the external reference is applied.

The AD7386-4/AD7387-4/AD7388-4 require $t_{POWERUP}$ from applying V_{CC} and V_{LOGIC} until the ADC conversion results are stable. Figure 4 shows the recommended power-up timing and condition with $\overline{\text{CS}}$ held high. It is highly recommended to issue a software reset after power-up (see the Software Reset section for details). However, conversion results are not guaranteed to meet data sheet specifications at this time.

Table 11. Signal Chain Components

Companion Devices	Part Name	Description	Typical Application
ADC Driver	ADA4896-2	1 nV/√Hz, rail-to-rail output amplifier	Precision, low noise, high frequency
	ADA4940-2	Ultra-low power, full differential, low distortion amplifier	Precision, low density, low power
	ADA4807-2	1 mA, rail-to-rail output amplifier	Precision, low power, high frequency
	LTC6227	1 nV/√Hz, 420 MHz low distortion rail-to rail-output amplifier	Precision, low noise, high frequency
External Reference	ADR4525	Ultra-low noise, high accuracy voltage reference	2.5 V V_{REF}
	ADR4533	Ultra-low noise, high accuracy voltage reference	3.3 V V_{REF}
Reference Buffer	ADA4807-2	1 mA, rail-to-rail output amplifier	Precision, low power, high frequency
LDO Regulator	ADP166	Very low quiescent, 150 mA LDO regulator	3.0 V to 3.6 V supply for V_{CC} and V_{LOGIC}
	ADP7104	500 mA low noise, CMOS LDO regulator	5 V supply
	ADP7182	Low noise line regulator	−2.5 V supply for ADC driver amplifier
	ADP5600	Interleaved inverting charge pump with negative LDO	Voltage inverter for negative supply

MODES OF OPERATION

The AD7386-4/AD7387-4/AD7388-4 have several on-chip configuration registers for controlling the operational mode of the device.

CHANNEL SELECTION

The ADC channel pairs for conversion ($A_{IN}A0/A_{IN}B0$, $A_{IN}C0/A_{IN}D0$, $A_{IN}A1/A_{IN}B1$, and $A_{IN}C1/A_{IN}D1$) are selected by setting the CH bit in the Configuration 1 register. If the CH bit is set to 0, the $A_{IN}A0$ channel, the $A_{IN}B0/A_{IN}C0$ channel, and the $A_{IN}D0$ channel simultaneously convert. Alternatively, if the CH bit is set to 1, the $A_{IN}A1$ channel, the $A_{IN}B1$ channel, the $A_{IN}C1$ channel, and $A_{IN}D1$ channel are selected for simultaneous conversion.

If the channel to convert is changing, the ADC requires additional settling time. The maximum throughput rate when changing between the $A_{IN}x0$ channel and the $A_{IN}x1$ channel is 2 MSPS.

SEQUENCER

The AD7386-4/AD7387-4/AD7388-4 can be configured to automatically cycle through the $A_{IN}x0$ channel and the $A_{IN}x1$ channel using the on-chip sequencer. The sequencer is controlled via the SEQ bit in the Configuration 1 register. If the SEQ bit is set to 0, the sequencer is disabled. If SEQ is set to 1, the sequencer is enabled. The CH bit is not queried for the sequencer mode. The sequencer always starts at the $A_{IN}x0$ channel and then moves to the $A_{IN}x1$ channel. After converting the $A_{IN}x1$ channel, the sequencer loops back to the $A_{IN}x0$ channel and the sequence restarts.

In sequencer mode (SEQ = 1), the channel to convert is automatically changing, and the ADC requires additional settling time. The maximum throughput rate when changing between the $A_{IN}x0$ channel and the $A_{IN}x1$ channel is 2 MSPS.

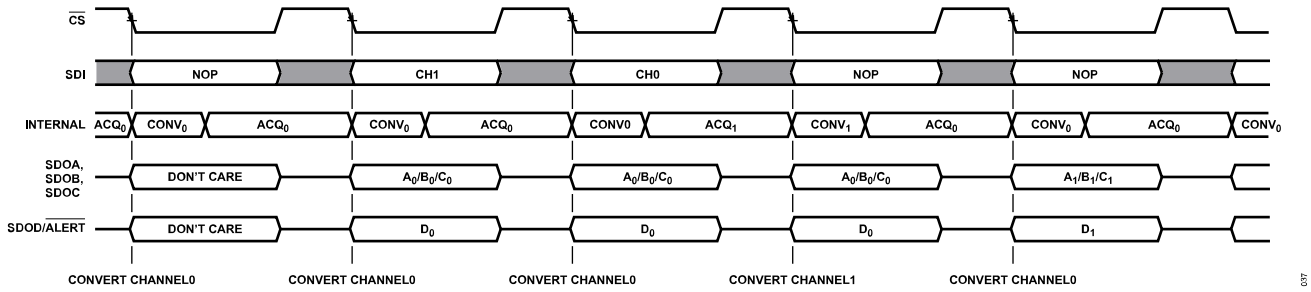


Figure 37. Manual Channel Selection Setup

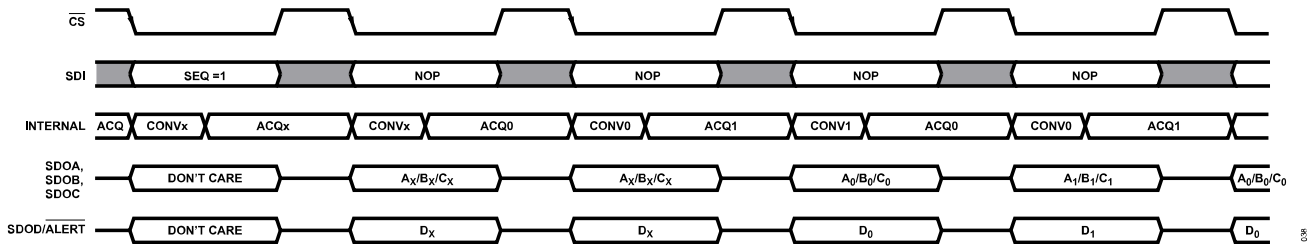


Figure 38. Channel Sequencer Setup

MODES OF OPERATION

OVERSAMPLING

Oversampling is a common method used in analog electronics to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from quantization noise and thermal noise (kTC noise) of the ADC. The AD7386-4/AD7387-4/AD7388-4 offer an oversampling function on chip. The AD7386-4/AD7387-4/AD7388-4 have two user configurable OS modes: normal averaging and rolling average.

The oversampling functionality is configured by programming the OS_MODE bit and the OSR bits in the Configuration 1 register.

Normal Averaging Oversampling

The normal averaging OS mode can be used in applications where slower output data rates are allowed and where higher SNR or dynamic range is desirable. Normal averaging involves taking a number of samples, adding them together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is cleared when the process completes.

The normal averaging OS mode is configured by setting the OS_MODE bit to Logic 0 and having a valid nonzero value in the OSR bits. The OS ratio of the digital filter is controlled using the oversampling bits, OSR (see Table 12).

Table 12 provides the oversampling bit decoding to select the different OS rates. The output result is decimated to 16-bit resolution. If required, additional resolution can be achieved by configuring the resolution boost bit (RES) in the Configuration 1 register. See the Resolution Boost section for further details.

The number of samples (n), defined by the OSR bits, are taken and added together, and the result is divided by n. The initial ADC conversion is initiated by the falling edge of $\overline{CS}$ and the AD7386-4/AD7387-4/AD7388-4 control all subsequent samples in the oversampling sequence internally. The sampling rate of the additional n at the device maximum sampling rate is 3 MSPS for AD7386-4, and 4 MSPS for AD7387-4 and AD7388-4. The data is ready for readback on the next serial interface access. After the averaging technique is applied, the sample data used in the calculation is discarded. This process is repeated every time the application needs a new conversion result and is initiated by the next falling edge of $\overline{CS}$.

As the output data rate is reduced by the OS ratio, the serial peripheral interface (SPI) frequency required to transmit the data is reduced accordingly.

Table 12. Normal Averaging Oversampling Overview

		SNR (dB Typical)				
		2.5 V External Reference		3.3 V External Reference		Data Output Rate (kSPS Maximum)
OSR, Bits[2:0]	OS Ratio	RES = 0	RES = 1	RES = 0	RES = 1	
000	No OS	83.15	83.25	84.5	84.5	4000
001	2	86.15	86.36	87.12	87.46	1500
010	4	88.8	89.35	89.66	90.32	750
011	8	91.05	92.05	91.77	92.81	375
100	16	92.7	94.18	93.4	95.03	187.5
101	32	93.8	95.91	94.74	96.35	93.75
110	Invalid	N/A[1]	N/A[1]	N/A[1]	N/A[1]	N/A[1]
111	Invalid	N/A[1]	N/A[1]	N/A[1]	N/A[1]	N/A[1]

[1] N/A means not applicable.

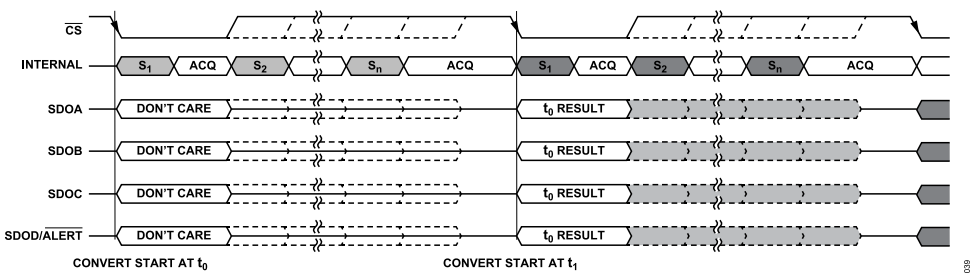


Figure 39. Normal Averaging Oversampling Operation

MODES OF OPERATION

Rolling Average Oversampling

The rolling average OS mode can be used in applications where higher output data rates are required and where a higher SNR or dynamic range is desirable. Rolling averaging involves taking a number of samples, adding them together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is not cleared when the process completes. The rolling average OS mode uses a first in, first out (FIFO) buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same.

The rolling average OS mode is configured by setting the OS_MODE bit to Logic 1 and having a valid nonzero value in the OSR bits. The OS ratio of the digital filter is controlled using the oversampling bits, OSR (see Table 13).

Table 13 provides the oversampling bit decoding to select the different OS rates. The output result is decimated to 16-bit resolution for the AD7386-4/AD7387-4/AD7388-4. If required, additional resolution can be achieved by configuring the resolution boost bit in the Configuration 1 register. See the Resolution Boost section for further details.

In the rolling average OS mode, all ADC conversions are controlled and initiated by the falling edge of $\overline{CS}$. When a conversion is complete, the result is loaded into the FIFO. The FIFO length is 8, regardless of the OS ratio set. The FIFO is filled on the first conversion after a power-on reset (POR) and on the first conversion after a software controlled hard or soft reset. A new conversion result is shifted into the FIFO on completion of every ADC conversion regardless of the status of the OSR bits and the OS_MODE bit. This conversion allows a seamless transition from no OS to rolling average OS, or different rolling average OS ratios without waiting for the FIFO to fill.

The number of samples, n, defined by the OSR bits are taken from the FIFO, added together, and the result is divided by n.

Table 13. Rolling Average Oversampling Overview

		SNR (dB Typical)				
		2.5 V External Reference		3.3 V External Reference		Data Output Rate
OSR, Bits[2:0]	OS Ratio	RES = 0	RES = 1	RES = 0	RES = 1	(kSPS Maximum)
000	No OS	83.17	83.25	84.51	84.5	4000
001	2	85.77	85.97	86.61	86.9	4000
010	4	88.31	88.77	89.02	89.61	4000
011	8	90.74	91.68	91.42	92.32	4000
110	Invalid	N/A[1]	N/A[1]	N/A[1]	N/A[1]	N/A[1]
111	Invalid	N/A[1]	N/A[1]	N/A[1]	N/A[1]	N/A[1]

[1] N/A means not applicable.

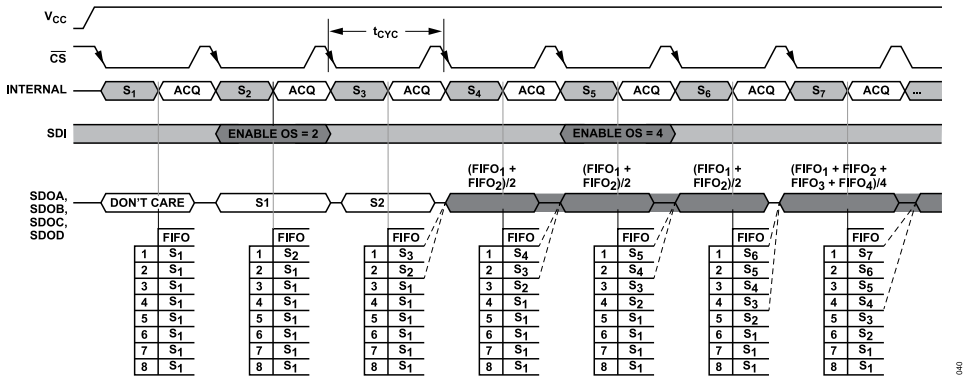


Figure 40. Rolling Average OS Mode Configuration

MODES OF OPERATION

RESOLUTION BOOST

The default resolution and output data size are 16 bits for the AD7386-4, 14 bits for the AD7387-4, and 12 bits for the AD7388-4. When the on-chip oversampling function is enabled, the performance of the ADC can exceed the default resolution. To accommodate the performance boost achievable, it is possible to enable an additional two bits of resolution. If the RES bit in the Configuration 1 register is set to Logic 1 and the AD7386-4/AD7387-4/AD7388-4 are in a valid OS mode, the conversion result size is 18 bits for the AD7386-4, 16 bits for the AD7387-4, and 14 bits for the AD7388-4. In this mode, 18 SCLK cycles are required to propagate the data for the AD7386-4, 16 SCLK cycles are required for the AD7387-4, and 14 SCLK cycles are required for the AD7388-4.

ALERT

The alert functionality is an out of range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the value in the conversion result register exceeds the alert high limit value in the alert high threshold register or falls below the alert low limit value in the alert low threshold register. The alert high threshold register and the alert low threshold register are common to all ADCs. When setting the threshold limits, the alert high threshold must always be greater than the alert low threshold. Detailed alert information is accessible in the Alert Indication Register section.

The register contains two status bits per ADC, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all ADCs creates a common alert value. This value can be configured to drive out on the $\overline{\text{ALERT}}$ function of the SDOD/$\overline{\text{ALERT}}$ pin. The SDOD/$\overline{\text{ALERT}}$ pin is configured as $\overline{\text{ALERT}}$ by configuring the following bits in the Configuration 1 and Configuration 2 registers:

1. Set the SDO bits to any value other than 0b10.
2. Set the ALERT_EN bit to 1.
3. Set a valid value in the alert high threshold register and the alert low threshold register.

The alert indication function is available in oversampling (rolling averaging, normal averaging, and non-OS modes).

The alert function of the SDOD/$\overline{\text{ALERT}}$ pin updates at the end of conversion. The alert indication status bits in the $\overline{\text{ALERT}}$ register are updated as well and must be read before the end of the next conversion.

Bits[7:0] in the alert indication register are cleared by reading the alert indication register contents. The alert function of the SDOD/$\overline{\text{ALERT}}$ pin is cleared with a falling edge of $\overline{\text{CS}}$. Issuing a software reset also clears the alert status in the alert indication register.

See Figure 8 for the $\overline{\text{ALERT}}$ timing diagram.

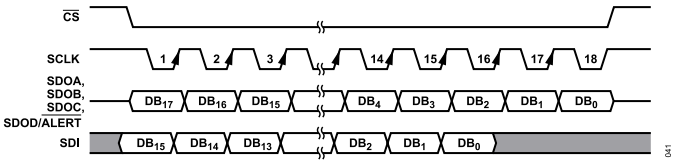


Figure 41. Resolution Boost

MODES OF OPERATION

POWER MODES

The AD7386-4/AD7387-4/AD7388-4 have two power modes that can be set in the Configuration 1 register: normal mode and shutdown mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the Configuration 1 register to configure the power modes in the AD7386-4/AD7387-4/AD7388-4. Set PMODE to Logic 0 for normal mode and Logic 1 for shutdown mode.

Normal Mode

Keep the AD7386-4/AD7387-4/AD7388-4 in normal mode to achieve the fastest throughput rate. All blocks within the AD7386-4/AD7387-4/AD7388-4 always remain fully powered and an ADC conversion can be initiated by a falling edge of $\overline{CS}$ when required. When the AD7386-4/AD7387-4/AD7388-4 are not converting, these devices are in static mode, and power consumption is automatically reduced. Additional current is required to perform a conversion. Therefore, power consumption of the AD7386-4/AD7387-4/AD7388-4 scales with throughput.

Shutdown Mode

When slower throughput rates and lower power consumption are required, use shutdown mode by either powering down the ADC between each conversion, or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the AD7386-4/AD7387-4/AD7388-4 are in shutdown mode, all analog circuitry powers down. The serial interface remains active during shutdown mode to allow the AD7386-4/AD7387-4/AD7388-4 to exit shutdown mode.

To enter shutdown mode, write to the power mode configuration bit, PMODE, in the Configuration 1 register. The AD7386-4/AD7387-4/AD7388-4 shut down, and current consumption reduces. To exit shutdown mode and return to normal mode, set the PMODE bit in the Configuration 1 register to Logic 0. All register configuration settings remain unchanged entering or leaving shutdown mode. After exiting shutdown mode, allow sufficient time for the circuitry to turn on before starting a conversion. If the internal reference is enabled, the reference must be allowed to settle for accurate conversions to happen. $t_{STARTUP}$ time required to settle for both internal and external reference is shown in Table 5.

INTERNAL AND EXTERNAL REFERENCE

The AD7386-4/AD7387-4/AD7388-4 have a 2.5 V internal reference. Alternatively, if a more accurate reference or higher dynamic range is required, an external reference can be supplied. An externally supplied reference can be in the range of 2.5 V to 3.3 V. The recommended external voltage reference is the ADR4525 for 2.5 V and the ADR4533 for 3.3 V. When using the external reference, the core refers to the voltage in the REFIO pin during ADC conversion. The V_{REF} voltage of the AD7386-4/AD7387-4/AD7388-4 is driven through the REFIO pin. This pin can be supplied with a voltage ranging from 2.5 V to 3.3 V. The external V_{REF} requires enough current to drive the AD7386-4/AD7387-4/AD7388-4, which is a maximum of 1.2 mA. Connecting a 1 µF capacitor to the REFIO pin is recommended.

Reference selection, internal and external, is configured by the REFSEL bit in the Configuration 1 register. If the REFSEL bit is set to 0, the internal reference buffer is enabled. If an external reference is preferred, the REFSEL bit must be set to 1, and an external reference must be supplied to the REFIO pin.

SOFTWARE RESET

The AD7386-4/AD7387-4/AD7388-4 have two reset modes: a soft reset and a hard reset. A reset is initiated by writing to the reset bits in the Configuration 2 register.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The alert indication register is cleared. The reference and LDO regulator remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to the default status, and resets the internal oscillator block. It is recommended to perform a hard reset after power-up.

DIAGNOSTIC SELF TEST

The AD7386-4/AD7387-4/AD7388-4 run a diagnostic self test after a POR or after a software hard reset to ensure that the correct configuration is loaded into the device.

The result of the self test is displayed in the SETUP_F bit in the alert indication register. If the SETUP_F bit is set to Logic 1, the diagnostic self test has failed. If the test fails, perform a software hard reset to reset the AD7386-4/AD7387-4/AD7388-4 registers to the default status.

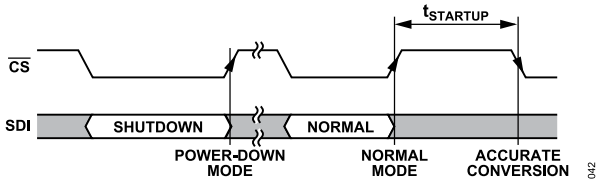


Figure 42. Shutdown Mode Operation

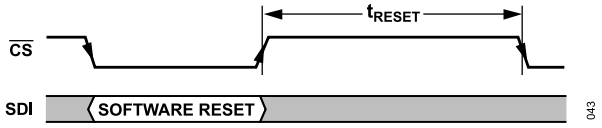


Figure 43. Software Reset Operation

INTERFACE

The interface to the AD7386-4/AD7387-4/AD7388-4 is via a serial interface. The interface consists of $\overline{CS}$, SCLK, SDOA, SDOB, SDOC, SDOD, and SDI. When referencing a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed such as SDOD. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

The $\overline{CS}$ signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled and the bus is taken out of three-state. The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The SCLK signal synchronizes data in and out of the device via the SDOA, SDOB, SDOC, SDOD, and SDI signals. A minimum of 16 SCLK cycles are required for a write to or read from a register. The minimum numbers of SCLKs for a conversion read is dependent on the resolution of the device and the configuration settings (see Table 14).

The AD7386-4/AD7387-4/AD7388-4 have four serial output signals: SDOA, SDOB, SDOC, and SDOD. Programming the SDO bits in the Configuration 2 register configures 2-wire mode, 1-wire mode, or 4-wire mode. To achieve the highest throughput of the device, it is required to use either the 2-wire mode or 4-wire mode to read the conversion results. If a reduced throughput is required or oversampling is used, it is possible to use 1-wire mode, SDOA signal only, for reading conversion results.

Configuring cyclic redundancy check (CRC) operation for SPI reads, SPI writes, and OS mode with resolution boost mode enabled can alter the operation of the interface. Refer to the CRC section to ensure correct operation.

READING CONVERSION RESULTS

The $\overline{CS}$ signal initiates the conversion process. A high to low transition on the $\overline{CS}$ signal initiates a simultaneous conversion of the four ADCs, ADC A, ADC B, ADC C, and ADC D. The AD7386-4/AD7387-4/AD7388-4 have a one cycle readback latency. Therefore, the conversion results are available on the next SPI access. Then, take the $\overline{CS}$ signal low, and the conversion result clocks out on the serial data output pins. The next conversion is also initiated at this point.

The conversion result is shifted out of the device as a 16-bit result for the AD7386-4/AD7387-4/AD7388-4. The MSB of the conversion result is shifted out on the $\overline{CS}$ falling edge. The remaining data is shifted out of the device under the control of the SCLK input. The data is shifted out on the rising edge of SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take $\overline{CS}$ high again to return the serial data output pins to a high impedance state.

The number of SCLK cycles to propagate the conversion results on the serial data output pins is dependent on the serial mode of operation configured and if resolution boost mode is enabled (see Figure 44 and Table 14 for details). If CRC reading is enabled, additional SCLK pulses are required to propagate the CRC information. See the CRC section for more details.

Because the $\overline{CS}$ signal initiates a conversion as well as framing the data, any data access must be completed within a single frame.

Table 14. Number of SCLK Cycles (n) Required for Reading Conversion Results

Interface Configuration	Resolution Boost Mode	CRC Read	Number of SCLK Cycles
4-Wire	Disabled	Disabled	16
		Enabled	24
	Enabled	Disabled	18
		Enabled	26
2-Wire	Disabled	Disabled	32
		Enabled	40
	Enabled	Disabled	36
		Enabled	44
1-Wire	Disabled	Disabled	64
		Enabled	72
	Enabled	Disabled	72
		Enabled	80

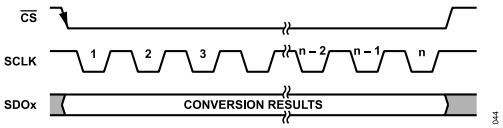


Figure 44. Reading Conversion Results (Consult Table 14 for Values for n, the Number of SCLK Pulses Required)

INTERFACE

Serial 4-Wire Mode

Configure 4-wire mode by setting the SDO bits to 0b10 in the Configuration 2 register. In 4-wire mode, the conversion result for ADC A is output on SDOA, ADC B on SDOB, ADC C on SDOC, and ADC D on SDOD.

Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO bits to 0b00 in the Configuration 2 register. In 2-wire mode, the conversion results for ADC A and ADC C are output on SDOA. The conversion results for ADC B and ADC D are output on SDOB.

Serial 1-Wire Mode

In applications where slower throughput rates are allowed or normal averaging OS is used, the serial interface can be configured to operate in 1-wire mode. In 1-wire mode, the conversion results from ADC A, ADC B, ADC C, and ADC D are output on SDOA. Additional SCLK cycles are required to propagate all data. ADC A data is output first followed by the ADC B, ADC C, and ADC D conversion results.

LOW LATENCY READBACK

The interface on the AD7386-4/AD7387-4/AD7388-4 have a one cycle latency as shown in Figure 46. For applications that operate at lower throughput rates, the latency of reading the conversion result can be reduced. After the conversion time ($t_{CONVERT}$) elapses, a second $\overline{CS}$ pulse after the initial $\overline{CS}$ pulse that initiated the conversion can be used to read back the conversion result. This operation is shown in Figure 48.

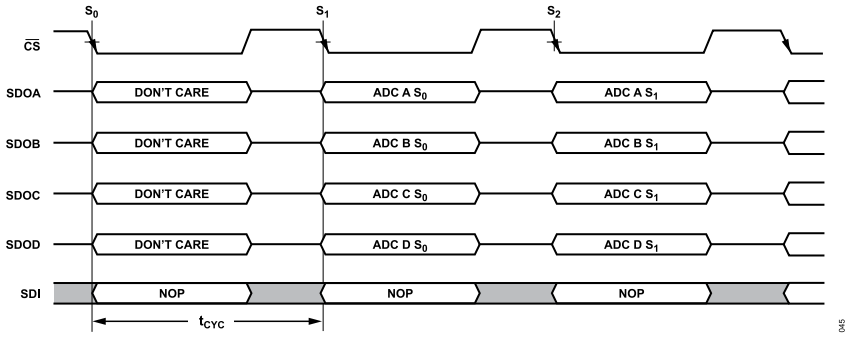


Figure 45. Read Conversion Results, 4-Wire Mode

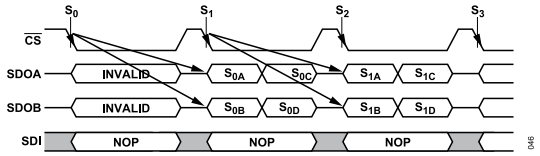


Figure 46. Read Conversion Results, 2-Wire Mode

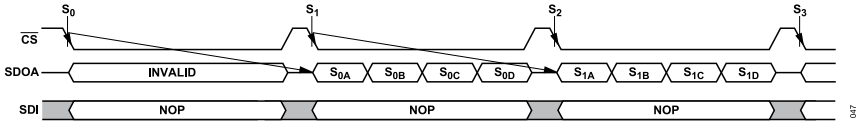


Figure 47. Reading Conversion Results, 1-Wire Mode

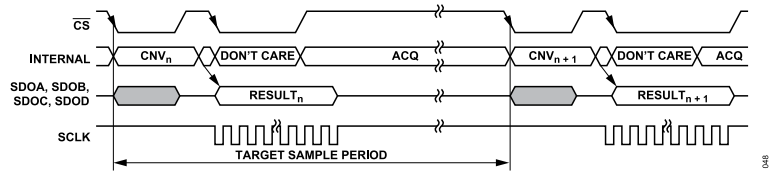


Figure 48. Low Throughput Low Latency

INTERFACE

READING FROM DEVICE REGISTERS

All registers in the device can be read over the serial interface. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or no operation command (NOP). The format for a read command is shown in Table 17. Bit D15 must be set to 0 to select a read command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], are ignored.

WRITING TO DEVICE REGISTERS

All the read/write registers in the AD7386-4/AD7387-4/AD7388-4 can be written to over the serial interface. The length of an SPI write access is determined by the CRC write function. An SPI access is 16 bits if CRC write is disabled and 24 bits when CRC write is enabled. The format for a write command is shown in Table 17. Bit D15 must be set to 1 to select a write command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], contain the data to be written to the selected register.

CRC

The AD7386-4/AD7387-4/AD7388-4 have CRC checksum modes that can be used to improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for SPI interface reads and writes. For example, enable the CRC function for SPI writes to prevent unexpected changes to the device configuration but do not enable the CRC function on SPI reads to maintain a higher throughput rate. The CRC feature is controlled by programming the CRC_W bit and CRC_R bit in the Configuration 1 register.

CRC Read

If enabled, a CRC consisting of an 8-bit word is appended to the conversion result or register reads. The CRC is calculated on the conversion result for ADC A, ADC B, ADC C, and ADC D, and is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 2-wire SPI mode, 1-wire SPI mode, 4-wire SPI mode, and resolution boost mode.

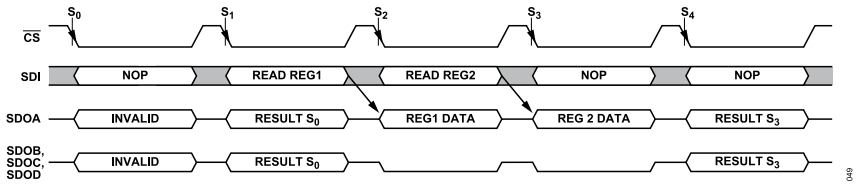


Figure 49. Register Read

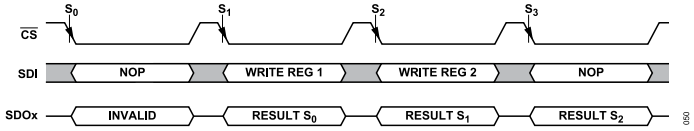


Figure 50. Register Write

INTERFACE

CRC Write

To enable the CRC write function, the CRC_W bit in the Configuration 1 register must be set to 1. To set the CRC_W bit to 1 to enable the CRC feature, a valid CRC must be appended to the request frame.

After the CRC feature is enabled, all register write requests are ignored unless they are accompanied by a valid CRC command. A valid CRC is required to both enable and disable the CRC write feature.

CRC Polynomial

For CRC checksum calculations, this polynomial is always used: $x^8 + x^2 + x + 1$.

To generate the checksum, the 16-bit data conversion results of the four channels are combined to produce a 64-bit data stream. The eight MSBs of the 64-bit data are inverted and the data is appended by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum.

For example, the AD7386-4/AD7387-4/AD7388-4 polynomial is 100000111. Let the original data of four channels be 0xAAAA, 0x5555, 0xAAAA, and 0x5555. The eight MSBs of the data are inverted. The data is then appended to include eight 0s on the right. In the final XOR operation, the reduced data is less than the polynomial. Therefore, the remainder is the CRC for the assumed data.

Table 15. Example CRC Calculation for 4-Channel, 16-Bit Data

Data	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**X[1]**	**X[1]**	**X[1]**	**X[1]**	**X[1]**	**X[1]**	**X[1]**	**X[1]**
Process Data	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
		1	0	0	0	0	0	1	1	1																														
				1	0	1	0	0	0	1	1	0																												
				1	0	0	0	0	0	1	1	1																												
						1	0	0	0	0	0	0	1	1	1	0																									
						1	0	0	0	0	0	0	1	1	1	1																									
													1	1	0	0	0	1	0	0	1	0	1	0	1														
														1	0	0	0	1	0	0	1	1	0	1	1														
															1	0	0	1	0	0	0	1	1	0	1														
																1	0	1	0	0	0	0	1	1	0	0													
																	1	1	0	0	0	0	0	1	1	0	0												
																		1	1	0	0	0	0	0	1	1	0	0											
																			1	1	0	0	0	0	0	1	1	0	0										
																				1	1	0	0	0	0	0	1	1	0	0									
																					1	1	0	0	0	0	0	1	1	0	0								
																						1	1	0	0	0	0	0	1	1	0	0							
																							1	1	0	0	0	0	0	1	1	0	0						
																								1	1	0	0	0	0	0	1	1	0	0					
																									1	1	0	0	0	0	0	1	1	0	0				
																										1	1	0	0	0	0	0	1	1	0	0				
																											1	1	0	0	0	0	0	1	1	0	0			
																												1	1	0	0	0	0	0	1	1	0	0		
																													1	1	0	0	0	0	0	1	1	0	0	
CRC																															1	0	0	1	1	1	0	0		

[1] X means don't care.

INTERFACE

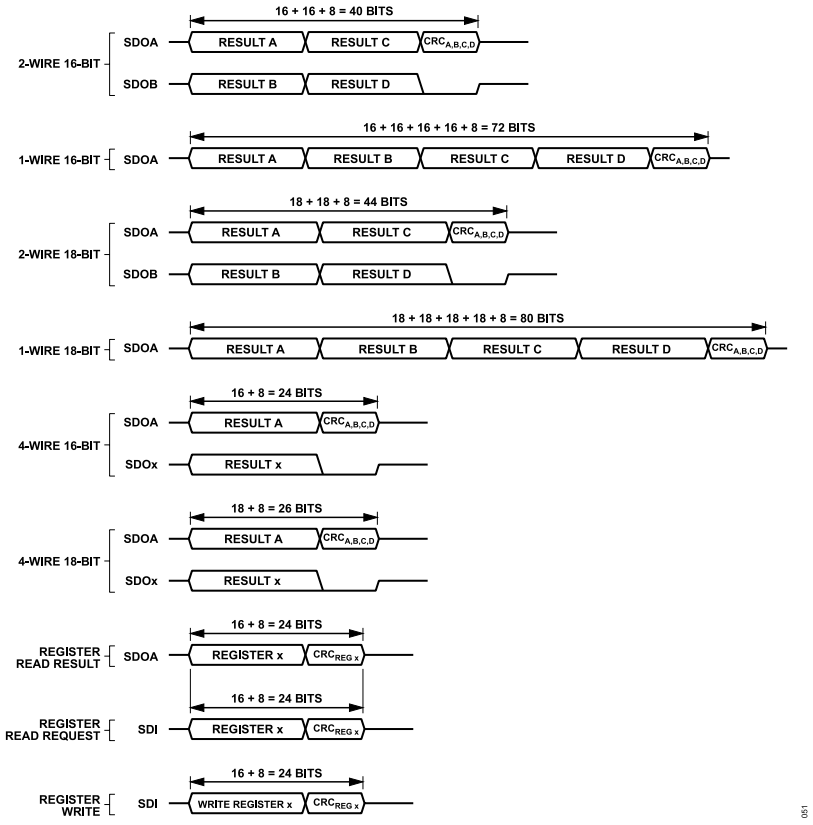


Figure 51. CRC Operation

REGISTERS

The AD7386-4/AD7387-4/AD7388-4 have user-programmable on-chip registers for configuring the device. Table 16 shows a complete overview of the registers available on the AD7386-4/AD7387-4/AD7388-4.

The registers are either read/write (R/W) or read only (R). Any read request to a write only register is ignored. Any write to a read only register is ignored. Writes to the NOP registers and the reserved register are ignored. Any read request to the NOP registers or reserved registers is considered a no operation and the data transmitted in the next SPI frame are the conversion results.

Table 16. Register Description

Reg	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	R/W
0x1	Configuration 1	[15:8]	WR	ADDRESSING			CH	SEQ	OS_MODE	OSR, Bit 2	0x0000	R/W
		[7:0]	OSR, Bits[1:0]		CRC_W	CRC_R	ALERTEN	RES	REFSEL	PMODE		
0x2	Configuration 2	[15:8]	WR	ADDRESSING			RESERVED		SDO, Bits[1:0]		0x0000	R/W
		[7:0]	RESET, Bits[7:0]									
0x3	Alert	[15:8]	WR	ADDRESSING			RESERVED		CRCW_F	SETUP_F	0x0000	R
		[7:0]	AI_D_HIGH	AI_D_LOW	AI_C_HIGH	AI_C_LOW	AI_B_HIGH	AI_B_LOW	AI_A_HIGH	AI_A_LOW		
0x4	Alert low threshold	[15:8]	WR	ADDRESSING			ALERT_LOW, Bits[11:8]				0x0800	R
		[7:0]	ALERT_LOW, Bits[7:0]									
0x5	Alert high threshold	[15:8]	WR	ADDRESSING			ALERT_HIGH, Bits[11:8]				0x07FF	R/W
		[7:0]	ALERT_HIGH, Bits[7:0]									

ADDRESSING REGISTERS

A serial register transfer on the AD7386-4/AD7387-4/AD7388-4 consists of 16 SCLK cycles. The four MSBs written to the device are decoded to determine which register is addressed. The four MSBs consist of the register address (REGADDR), Bits[2:0], and the read/write bit (WR). The register address bits determine which on-chip register is selected. If the addressed register is a valid write register, the WR bit determines whether the remaining 12 bits of data on the SDI input are loaded into the addressed register. If the WR bit is 1, the bits load into the register addressed by the register select bits. If the WR bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

Table 17. Addressing Register Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WR	REGADDR, Bits[2:0]			Data, Bits[11:0]											

Table 18. Bit Descriptions for Addressing Registers

Bit	Mnemonic	Description
D15	WR	When a 1 is written to this bit, Bits[11:0] of this register are written to the register specified by REGADDR if it is a valid address. Alternatively, when a 0 is written, the next data sent out on the SDOA pin is a read from the designated register if it is a valid address.
D14 to D12	REGADDR	When WR = 1, the contents of REGADDR determine the register for selection as outlined in Table 16. When WR = 0 and the REGADDR bits contain a valid register address, the contents on the requested register are output on the SDOA pin during the next interface access. When WR = 0 and the REGADDR bits contain 0x0, 0x6, or 0x7, the contents on the SDI line are ignored. The next interface access results in the conversion results being read back.
D11 to D0	Data	These bits are written into the corresponding register specified by the REGADDR bits when the WR bit = 1 and the REGADDR bits contain a valid address.

REGISTERS

CONFIGURATION 1 REGISTER

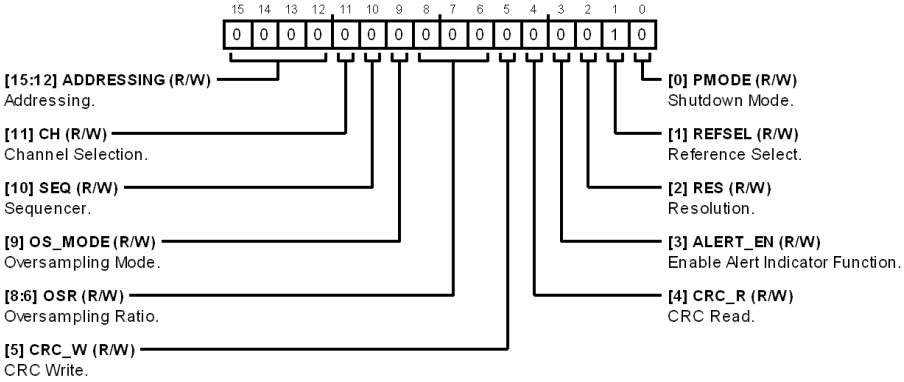


Table 19. Bit Descriptions for Configuration 1 Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
11	CH	Channel Selection. Selects the channel to converted. 0: Channel 0s. Selects Channel 0s of the ADC, $A_{IN}A0$, $A_{IN}B0$, $A_{IN}C0$, and $A_{IN}D0$. 1: Channel 1s. Selects Channel 0s of the ADC, $A_{IN}A1$, $A_{IN}B1$, $A_{IN}C1$, and $A_{IN}D1$.	0x0	R/W
10	SEQ	Sequencer. Cycles through the $A_{IN}X0$ and $A_{IN}X1$ Channels of the ADC for conversion. 0: Sequencer disabled. 1: Sequencer enabled.	0x0	R/W
9	OS_MODE	Oversampling Mode. Sets the oversampling mode of the ADC. 0: normal averaging. 1: rolling average.	0x0	R/W
[8:6]	OSR	Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the relevant mode. Normal averaging mode supports oversampling ratios of 2×, 4×, 8×, 16×, and 32×. Rolling average mode supports oversampling ratios of 2×, 4×, and 8×. 000: disabled. 001: 2×. 010: 4×. 011: 8×. 100: 16×. 101: 32×. 110: disabled. 111: disabled.	0x0	R/W
5	CRC_W	CRC Write. Controls the CRC functionality for the SDI interface. When setting this bit from a 0 to a 1, the command must be followed by a valid CRC to set this configuration bit. If a valid CRC is not received, the entire frame is ignored. If the bit is set to 1, it requires a CRC to clear it to 0. 0: no CRC function. 1: CRC function.	0x0	R/W
4	CRC_R	CRC Read. Controls the CRC functionality for the SDOx interface. 0: no CRC function. 1: CRC function.	0x0	R/W
3	ALERT_EN	Enable Alert Indicator Function. This bit functions when the SDO bits = 01. Otherwise, the ALERT_EN bit is ignored. 0: SDOB. 1: $\overline{\text{ALERT}}$.	0x0	R/W
2	RES	Resolution. Sets the size of the conversion result data. If OSR = 0, these bits are ignored and the resolution is set to default resolution.	0x0	R/W

REGISTERS

Table 19. Bit Descriptions for Configuration 1 Register (Continued)

Bits	Bit Name	Description	Reset	Access
		0: normal resolution. 1: 2-bit higher resolution.		
1	REFSEL	Reference Select. Selects the ADC reference source. 0: selects internal 2.5 V reference. 1: selects external reference source via REFIO pin.	0x0	R/W
0	PMODE	Power-Down Mode. Sets the power modes. 0: normal mode. 1: shutdown mode.	0x0	R/W

CONFIGURATION 2 REGISTER

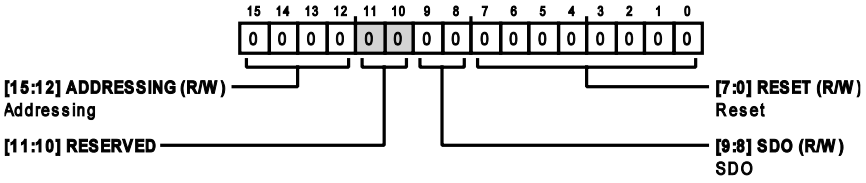
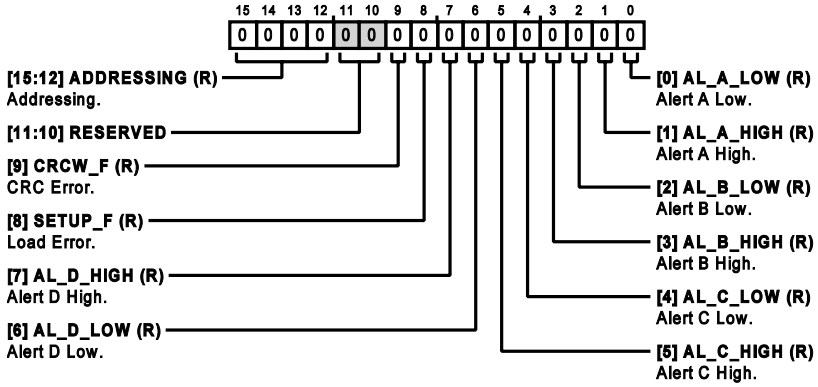


Table 20. Bit Descriptions for Configuration 2 Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing Bits. These bits define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R
[9:8]	SDO	SDO. Conversion Results Serial Data Output. 00: 2-wire output. Conversion data are output on both SDOA and SDOB. 01: 1-wire output. Conversion data are output on SDOA only. 10: 4-wire. Conversion data are output on SDOA, SDOB, SDOC, and SDOD/$\overline{\text{ALERT}}$. 11: 1-wire. Conversion data are output on SDOA, only.	0x0	R/W
[7:0]	RESET	Reset. 0x3C: performs a soft reset. Refreshes some blocks, register contents remain unchanged. Clears alert indication register and flushes any oversampling stored variables or active state machine. 0xFF: performs a hard reset. Resets all possible blocks in the device. Registers contents are set to defaults. All other values are ignored.	0x0	R/W

ALERT INDICATION REGISTER



REGISTERS

Table 21. Bit Descriptions for Alert Indication Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R
[11:10]	RESERVED	Reserved.	0x0	R
9	CRCW_F	CRC Error. Indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read. 0: no CRC error. 1: CRC error.	0x0	R
8	SETUP_F	Load Error. The SETUP_F indicates that the device configuration data did not load correctly on startup. This bit does not clear on an alert indication register read. A hard reset via the Configuration 2 register is required to clear this bit and restart the device setup. 0: no setup error. 1: setup error.	0x0	R
7	AL_D_HIGH	Alert D High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
6	AL_D_LOW	Alert D Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R
5	AL_C_HIGH	Alert C High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
4	AL_C_LOW	Alert C Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
3	AL_B_HIGH	Alert B High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
2	AL_B_LOW	Alert B Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
1	AL_A_HIGH	Alert A High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R
0	AL_A_LOW	Alert A Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R

REGISTERS

ALERT LOW THRESHOLD REGISTER

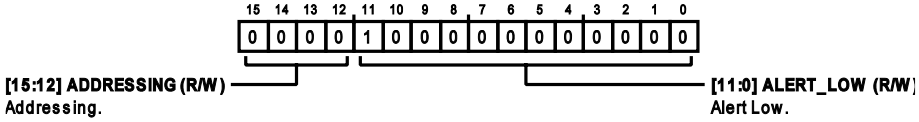


Table 22. Bit Descriptions for Alert Low Threshold Register

Bits	Bit Name	Descriptions	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:0]	ALERT_LOW	Alert Low. Bits[11:0] from ALERT_LOW move to the MSBs of the internal alert low register, D[15:4]. The remaining bits, D[3:0] of the internal register are fixed at 0x0. Sets an alert when the converter result is below the value in the alert low threshold register, and the alert is disabled when it is above the value in the alert low threshold register.	0x800	R/W

ALERT HIGH THRESHOLD REGISTER

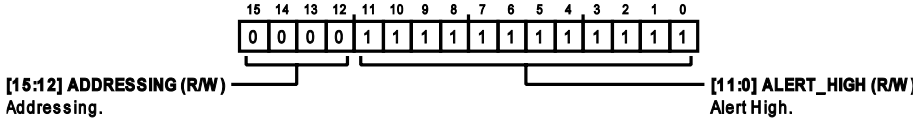


Table 23. Bit Descriptions for Alert High Threshold Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits [15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:0]	ALERT_HIGH	Alert High. Bits D[11:0] from ALERT_HIGH move to the MSBs of the internal alert high register, D[15:4]. The remaining bits, D[3:0] of the internal are fixed at 0xF. Sets an alert when the converter result is above the value in the alert high threshold register, and the alert is disabled when it is below the value in the alert high threshold register.	0xFFF	R/W

RELATED DEVICES

Table 24. Related Devices

No. of Channels	Input Type	16 Bits	14 Bits	12 Bits
4	Differential	AD7380-4 AD7389-4	AD7381-4	
	Pseudo-differential	AD7383-4 AD7380	AD7384-4 AD7381	
2	Differential	AD4680 AD4681		
	Pseudo-differential	AD7383 AD4682 AD4683	AD7384	
	Single-ended	AD7386 AD4684 AD4685	AD7387	AD7388

OUTLINE DIMENSIONS

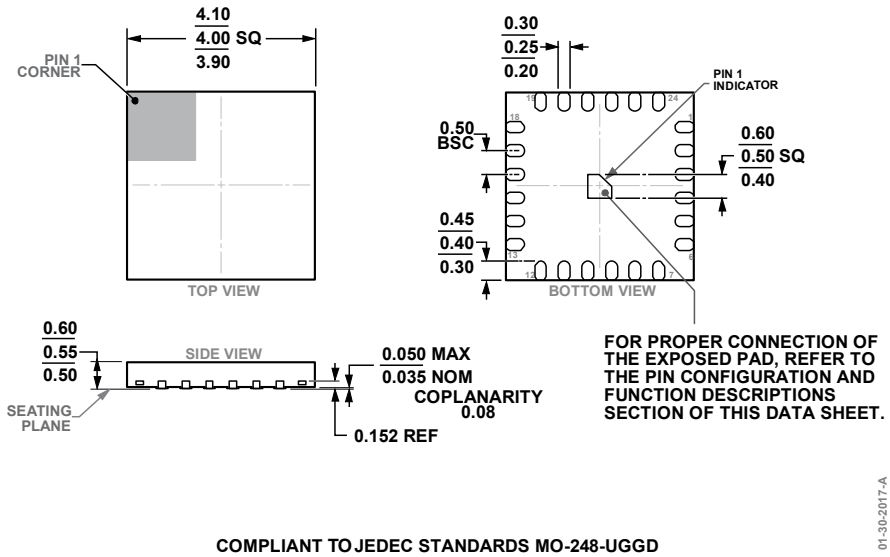


Figure 52. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.55 mm Package Height
(CP-24-25)
Dimensions shown in millimeters

Updated: October 18, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
AD7386-4BCPZ	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE		CP-24-25	
AD7386-4BCPZ-RL	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE	Reel, 5000	CP-24-25	
AD7386-4BCPZ-RL7	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE	Reel, 1000	CP-24-25	
AD7387-4BCPZ	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE		CP-24-25	CA7
AD7387-4BCPZ-RL	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE	Reel, 5000	CP-24-25	CA7
AD7387-4BCPZ-RL7	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE	Reel, 1000	CP-24-25	CA7
AD7388-4BCPZ	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE		CP-24-25	
AD7388-4BCPZ-RL	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE	Reel, 5000	CP-24-25	
AD7388-4BCPZ-RL7	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE	Reel, 1000	CP-24-25	

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-AD7386-4FMCZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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Analog Devices Inc.:

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