DS2401
Silicon Serial Number

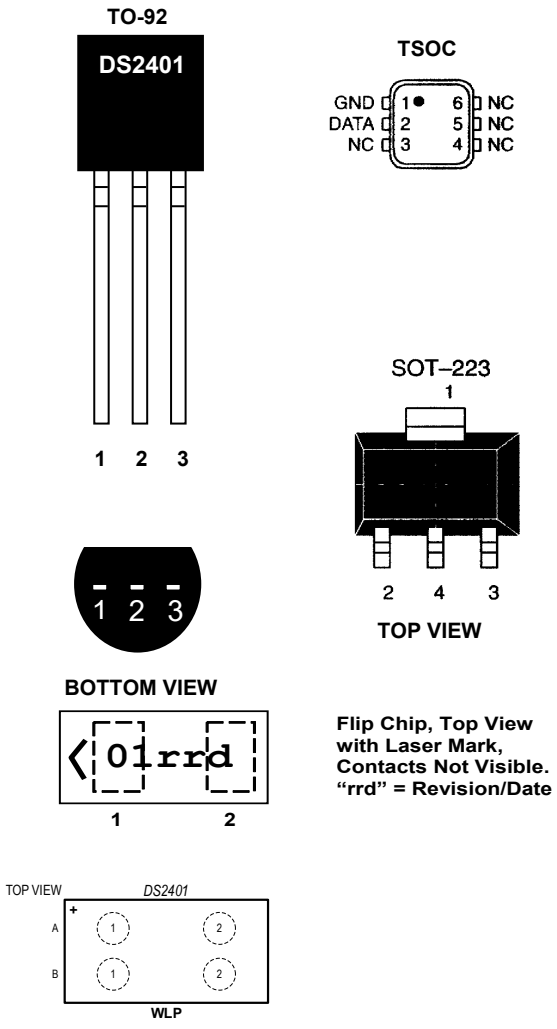
Benefits and Features

- Guaranteed Unique 64-Bit ROM ID Chip for Absolute Traceability
  - Unique, 64-Bit Registration Number (8-Bit Family Code + 48-Bit Serial Number + 8-Bit CRC Tester)
  - 8-Bit Family Code Specifies DS2401 Communications Requirements to Reader
- Minimalist 1-Wire® Interface Lowers Cost and Interface Complexity
  - Multiple DS2401 Devices Can Reside on a Common 1-Wire Net
  - Built-In Multidrop Controller Ensures Compatibility with Other 1-Wire Net Products
  - Reduces Control, Address, Data, and Power to a Single Pin and Communicates at up to 16.3kbps
  - Presence Pulse Acknowledges When the Reader First Applies Voltage
  - Low-Cost TO-92, SOT-223, and TSOC Surface-Mount Packages
  - TO-92 Tape-and-Reel Version with Leads Bent to 100-mil Spacing (Default) or with Straight Leads (DS2401-SL)
- Wide Voltage and Temperature Operating Ranges Enables Robust System Performance
  - Extended 2.8V to 6.0V Range (DS2401)
  - Zero Standby Power Required
  - -40°C to +85°C Industrial Temperature Range

Applications

- PCB Identification
- Network Node ID
- Equipment Registration

Pin Configurations



Pin Descriptions

NAME	PIN				
	TO-92	SOT-223	TSOC	FLIP CHIP	WLP
DATA (DQ)	2	2	2	1	A1, B1
GROUND	1	1, 4	1	2	A2, B2
N.C. (No Connect)	3	3	3–6	—	—

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19-5860; Rev 12/23

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS2401+	-40°C to +85°C	3 TO-92
DS2401A+	-40°C to +85°C	3 TO-92
DS2401+T&R	-40°C to +85°C	3 TO-92 (formed leads)
DS2401A+T&R	-40°C to +85°C	3 TO-92 (formed leads)
DS2401-SL+T&R	-40°C to +85°C	3 TO-92 (straight leads)
DS2401A-SL+T&R	-40°C to +85°C	3 TO-92 (straight leads)
DS2401P+	-40°C to +85°C	6 TSOC
DS2401AP+	-40°C to +85°C	6 TSOC
DS2401P+T&R	-40°C to +85°C	6 TSOC
DS2401AP+T&R	-40°C to +85°C	6 TSOC
DS2401Z+	-40°C to +85°C	4 SOT-223
DS2401AZ+	-40°C to +85°C	4 SOT-223
DS2401Z+T&R	-40°C to +85°C	4 SOT-223
DS2401AZ+T&R	-40°C to +85°C	4 SOT-223
DS2401X1-S#T	-40°C to +85°C	2 Flip Chip (2.5k pieces)
DS2401X-S+T	-40°C to +85°C	4 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R/T = Tape and reel.
SL = Straight leads.
#Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements.

Description

The DS2401 enhanced silicon serial number is a low-cost, electronic registration number that provides an absolutely unique identity which can be determined with a minimal electronic interface (typically, a single port pin of a microcontroller). The DS2401 consists of a 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol that requires only a single data lead and a ground return. Power for reading and writing the device is derived from the data line itself with no need for an external power source. The DS2401 is an upgrade to the DS2400. The DS2401 is fully reverse-compatible with the DS2400 but provides the additional multi-drop capability that enables many devices to reside on a single data line. The familiar TO-92, SOT-223, or TSOC package provides a compact enclosure that allows standard assembly equipment to handle the device easily.

Operation

The DS2401's internal ROM is accessed via a single data line. The 48-bit serial number, 8-bit family code and 8-bit CRC are retrieved using the 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus controller. All data is read and written least significant bit first.

1-Wire Bus System

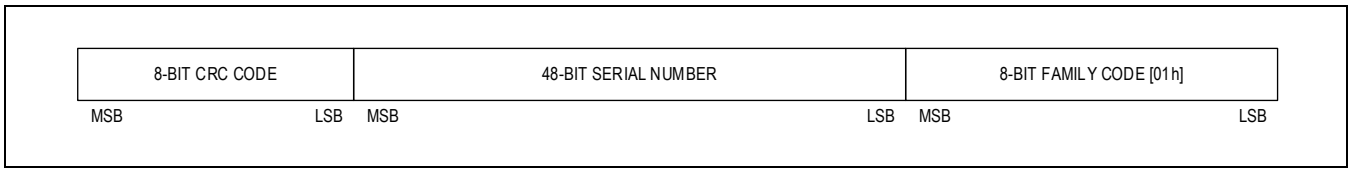
The 1-Wire bus is a system which has a single bus controller system and one or more peripherals. In all instances, the DS2401 is a peripheral device. The bus controller is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing).

Hardware Configuration

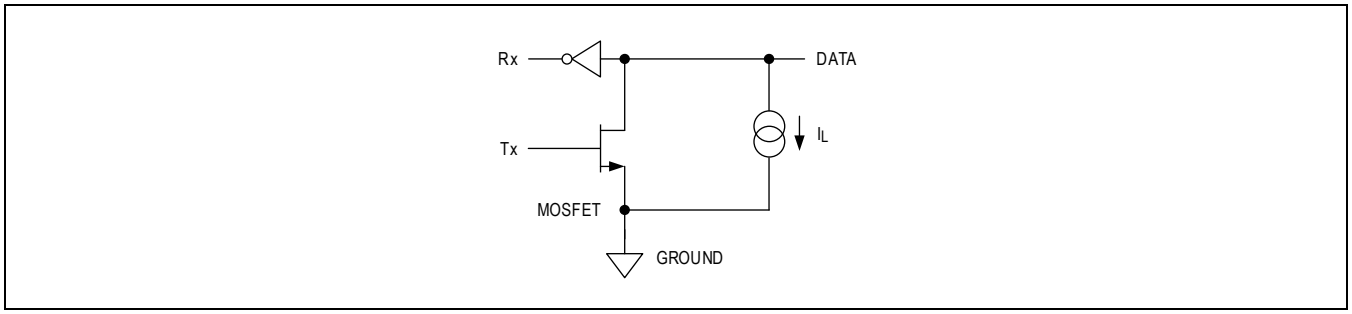
The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an

open-drain connection or 3-state outputs. The DS2401 is an open-drain part with an internal circuit equivalent to that shown in Figure 2. The bus controller can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus controller requires a pullup resistor at the controller end of the bus, with the bus controller circuit equivalent to the one shown in Figure 3. The value of the pullup resistor should be approximately 5kΩ (DS2401) or 2.2kΩ (DS2401A) for short line lengths. A multidrop bus consists of a 1-Wire bus with multiple peripherals attached. The 1-Wire bus has a maximum data rate of 16.3kbits per second.
The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more of the devices on the bus may be reset.

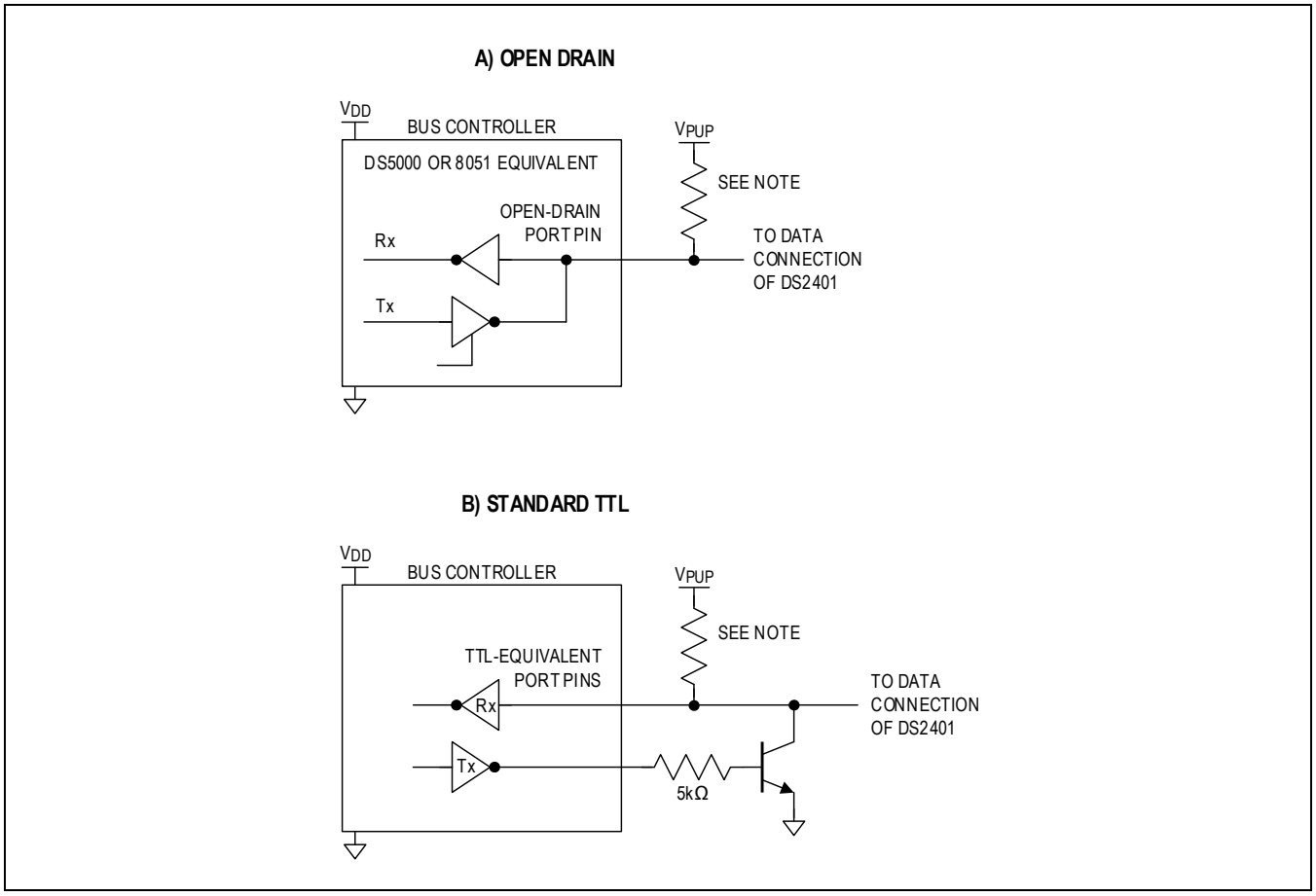
DS2401 Memory Map Figure 1



DS2401 Equivalent Circuit Figure 2



Bus Controller Circuit Figure 3



Note:
Depending on the 1-Wire communication speed and the bus load characteristics, the optimal pullup resistor (R_{PU}) value for the DS2401 will be in the 1.5kΩ to 5kΩ range. For the DS2401A, R_{PU} should range from 300Ω to 2.2kΩ.

Transaction Sequence

The sequence for accessing the DS2401 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus controller followed by a Presence Pulse(s) transmitted by the peripheral(s).

The Presence Pulse lets the bus controller know that the DS2401 is on the bus and is ready to operate. For more details, see the 1-Wire Signaling section.

ROM Function Commands

Once the bus controller has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 4).

Read ROM [33h]

This command allows the bus controller to read the DS2401's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2401 on the bus. If more than one peripheral is present on the bus, a data collision will occur when all peripherals try to transmit at the same time (open drain will produce a wired-AND result).

Legacy Read ROM [0Fh] (Not Supported by DS2401A)

In addition to command byte 33h, the DS2401 Read ROM function will also occur with a command byte of 0Fh in order to ensure compatibility with the DS2400, which will only respond to a 0Fh command word with its 64-bit ROM data. This legacy command byte is not supported by the DS2401A.

Match ROM [55h]/Skip ROM [CCh]

The complete 1-Wire protocol for all iButton® devices contains a Match ROM and a Skip ROM command. Since the DS2401 contains only the 64-bit ROM with no additional data fields, the Match ROM and Skip ROM are not applicable and will cause no further activity on the 1-Wire bus if executed. The DS2401 does not interfere with other 1-Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM (for example, a DS2401 and DS1994 on the same bus). However, the DS2401A will return a response after a Match ROM or Skip ROM command. If a multidrop configuration exists in the application, responses from connected DS2401A devices should be taken into account.

Search ROM [F0h]

When a system is initially brought up, the bus controller might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus controller to use a process of elimination to identify the 64-bit ROM codes of all peripheral devices on the bus. The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus controller performs this simple 3-step routine on each bit of the ROM. After one complete pass, the bus controller knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. Refer to Application Note 187: 1-Wire Search Algorithm for a comprehensive discussion of a ROM search, including an actual example.

1-Wire Signaling

The DS2401 requires a strict protocol to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1, and read data. All these signals except Presence Pulse are initiated by the bus controller.

The initialization sequence required to begin any communication with the DS2401 is shown in Figure 5. A reset pulse followed by a Presence Pulse indicates the DS2401 is ready to send or receive data given the correct ROM command.

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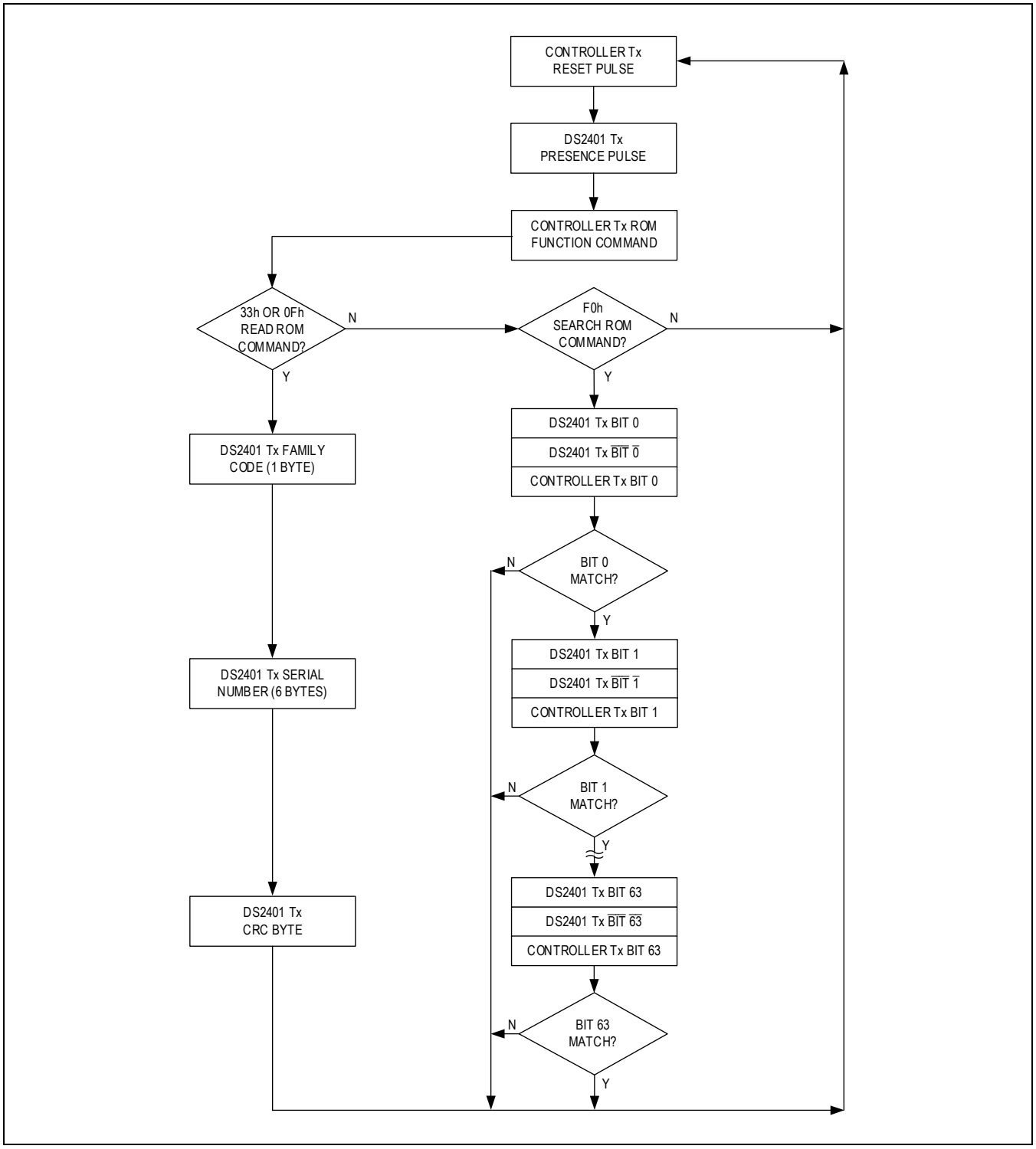
The bus controller transmits (Tx) a reset pulse (t_{RSTL}, minimum 480µs). The bus controller then releases the line and goes into receive mode (Rx). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS2401 waits (t_{PDH}, 15-60µs) and then transmits the Presence Pulse (t_{PDL}, 60-240µs). The 1-Wire bus requires a pullup resistance in the range specified by R_{PU}, depending on bus load characteristics.

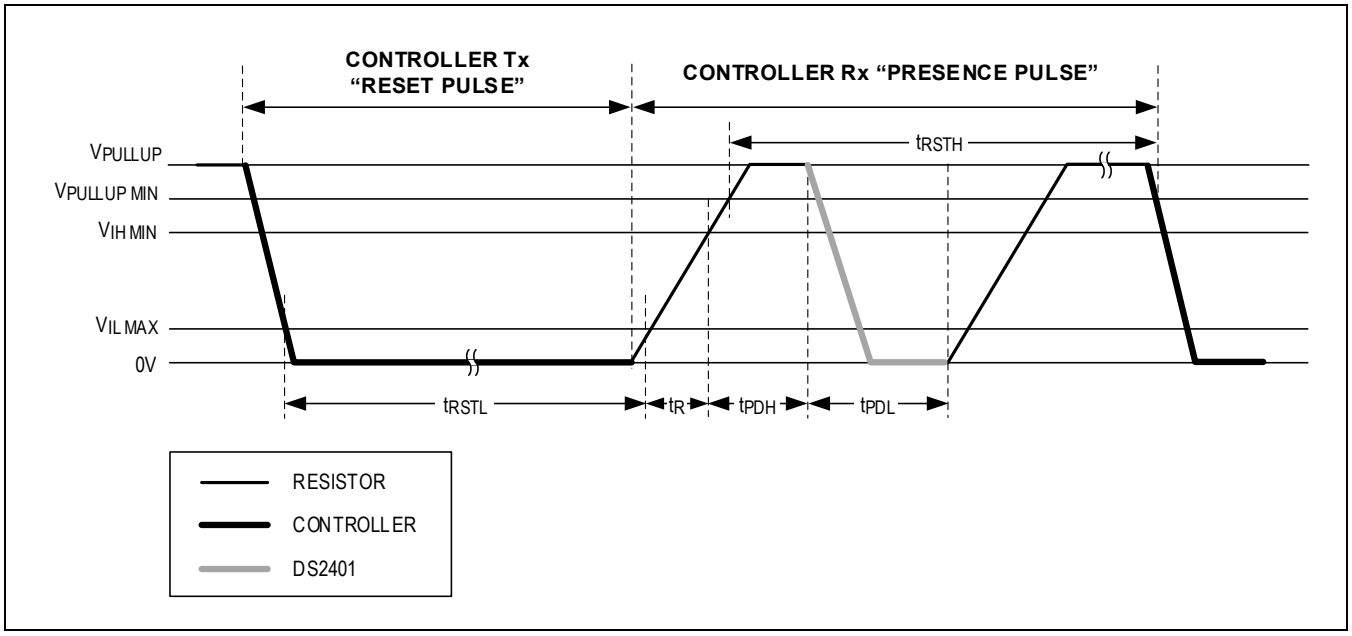
Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the controller driving the data line low. The falling edge of the data line synchronizes the DS2401 to the controller by triggering a delay circuit in the DS2401. During write time slots, the delay circuit determines when the DS2401 will sample the data line. For a read data time slot, if a “0” is to be transmitted, the delay circuit determines how long the DS2401 will hold the data line low overriding the “1” generated by the controller. If the data bit is a 1, the DS2401 will leave the read data time slot unchanged.

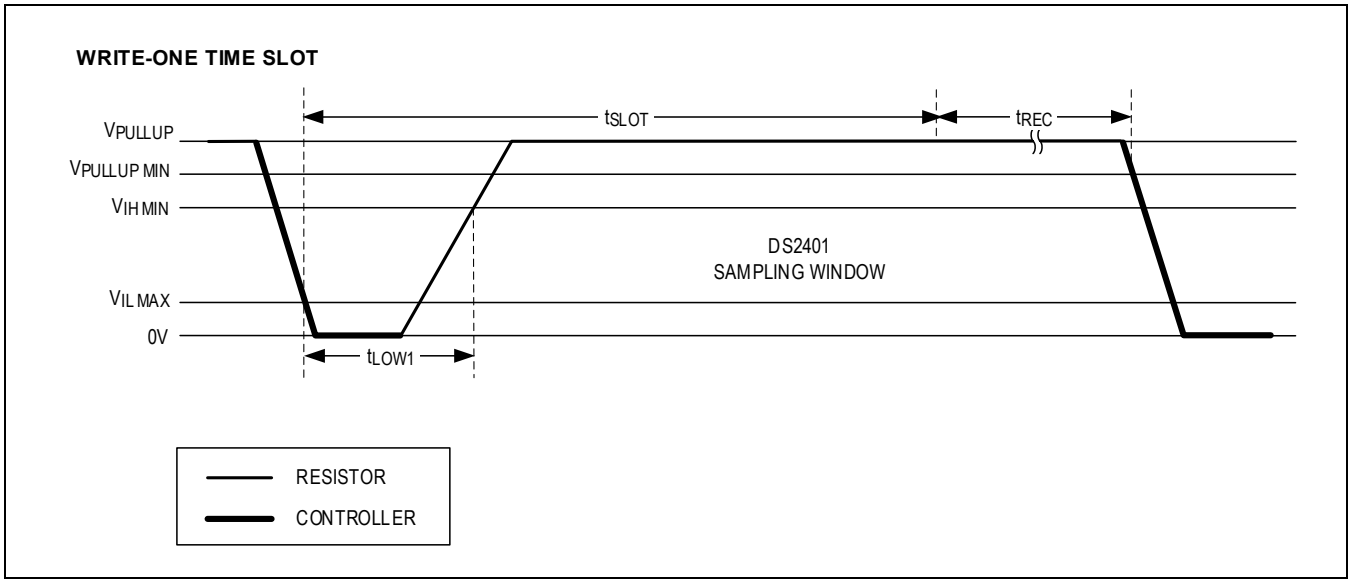
ROM Functions Flow Chart Figure 4



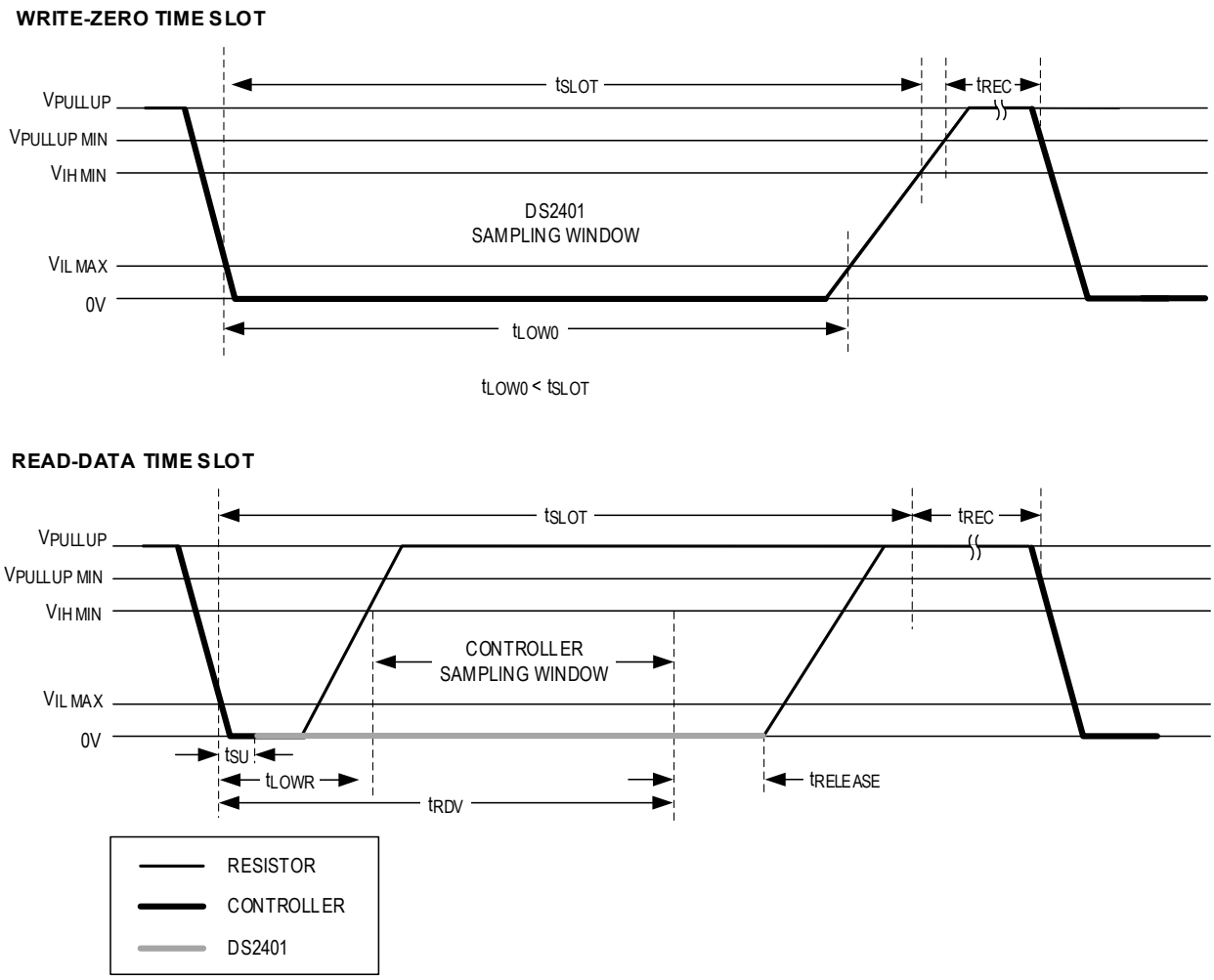
Initialization Procedure "Reset and Presence Pulses" Figure 5



Read/Write Timing Diagram Figure 6



Read/Write Timing Diagram (cont'd) Figure 6



CRC Generation

To validate the data transmitted from the DS2401, the bus controller may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last 8 bits of the DS2401. If the two CRC values match, the transmission is error-free.

The equivalent polynomial function of this CRC is: CRC = x8 + x5 + x4 + 1. Additional information about the 1-Wire CRC is available in the *Understanding and Using Cyclic Redundancy Checks with Maxim 1-Wire and iButton Products* application note.

Custom DS2401

Customization of a portion of the unique 48-bit serial number by the customer is available. Analog Devices will register and assign a specific customer ID in the 12 most significant bits of the 48-bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non-selectable and will be automatically incremented by one. Certain quantities and conditions apply for these custom parts. Contact your Analog Devices sales representative for more information.

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground
- DS2401 ..... -0.5V to +7.0V
- DS2401A ..... -0.5V to +6.0V

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (TO-92, TSOC, SOT-223 only; soldering, 10s) ..... +300°C
Soldering Temperature (reflow)
- TO-92 ..... +250°C
- TSOC, SOT-223, WLP ..... +260°C
- Flip Chip ..... +240°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Pullup Voltage (Note 2)	V_{PUP}	DS2401	2.8		6	V
		DS2401A	3		5.25	
Pullup Resistance (Note 1)	R_{PUP}	DS2401	1500		5000	Ω
		DS2401A	300		2000	
Logic 1 (Notes 6, 11)	V_{IH}	DS2401	2.2			V
		DS2401A		0.75 x V_{PUP}		
Logic 0	V_{IL}		-0.3		0.3	V
Output Logic-Low	V_{OL}				0.4	V
Input Load Current (Note 3)	IL			5		µA
Input Capacitance (Notes 7, 11)	CIO	DS2401			800	pF
		DS2401A		1000		
AC ELECTRICAL CHARACTERISTICS						
Time Slot	t_{SLOT}		60		120	µs
Write 1 Low Time (Note 10)	t_{LOW1}		1		15	µs
Write 0 Low Time	t_{LOW0}		60		120	µs
Read Data Valid (Note 9)	t_{RDV}			15		µs
Release Time	$t_{RELEASE}$		0	15	45	µs
Read Data Setup (Note 5)	t_{SU}				1	µs
Recovery Time	t_{REC}		1			µs
		DS2401A, R_{PUP} = 2200Ω (Notes 1, 12)	5			
Reset Time High (Note 4)	t_{RSTH}		480			µs
Reset Time Low	t_{RSTL}	DS2401 (Note 8)	480		960	µs
		DS2401A	480		640	
Presence Detect High	t_{PDH}		15		60	µs
Presence Detect Low	t_{PDL}		60		240	µs

Note 1: System requirement.

Note 2: V_{PUP} = external pullup voltage.

Note 3: Input load is to ground.

Note 4: An additional reset or communication sequence cannot begin until the reset high time has expired.

Note 5: Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within t_{SU} of this falling edge.

Note 6: V_{IH} is a function of the external pullup resistor and V_{PUP}.

Note 7: Specified value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.

Note 8: The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs to allow interrupt signaling, otherwise it could mask or conceal interrupt pulses if this device is used in parallel with a DS2404 or DS1994.

Note 9: The optimal sampling point for the controller is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV}. For the case of a Read-One Time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a Read-Zero Time slot, it ensures that a read will occur before the fastest 1-Wire device(s) releases the line.

Note 10: The duration of the low pulse sent by the controller should be a minimum of 1µs with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time, or before the controller samples in the case of a Read-One Time.

Note 11: Guaranteed by design and/or characterization only. Not production tested

Note 12: Applies to a single device attached to a 1-Wire line.

Package Information

For the latest package outline information and land patterns (footprints), go to the **Package Index** on the Analog Devices website. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
3 TO-92 (straight leads)	Q3+1	21-0248	—
3 TO-92 (formed leads)	Q3+4	21-0250	—
6 TSOC	D6+1	21-0382	90-0321
4 SOT-223	K3+1	21-0264	—
2 Flip Chip	BF211#1	21-0378	21-0378
4 WLP	N40B1+1	21-0605	Refer to Application Note 1891

Revision History

REVISION DATE	DESCRIPTION	PAGES CHANGED
040601	Changed MicroLAN to 1-Wire Net; updated ordering information for tape and reel	1
	Changed soldering temperature from 260°C for 10 seconds to See J-STD-020A Specification	9
022202	Below Figure 3, added a note on the optimal R_{PUP} range; added a similar note before the *Read/Write Time Slots* section	3, 6
	Added notes 11 to 13 to the EC table	9, 10
122106	Added flip chip package; added lead-free ordering information	1, 2
	References to the *Book of iButton Standards* replaced with references to corresponding application notes	Various
	V_{ILMAX} changed from 0.8V to 0.3V, EC table note 11 deleted	9, 10
5/11	Deleted standard (Pb) parts from ordering information; changed flip chip part number from DS2401X1 to DS2401X1-S#T	2
	Deleted V_{OH} from the EC table; moved V_{PUP} from the EC table header into the EC table; changed soldering temperature from J-STD-020A reference to explicit package specific numbers	9
	Added *Package Information* and *Revision History* sections	10, 11
3/15	Revised *Benefits and Features* section	1
12/16	Added WLP package to *Pin Configurations*, *Pin Descriptions*, *Ordering Information*, *Absolute Maximum Ratings*, and *Package Information* sections	1, 2, 9, 10
11/21	Added DS2401 content: updated *Benefits and Features*, *Ordering Information* table, *Description section*, *Hardware Configuration* section, Figure 2, *ROM Function Commands* section, *1-Wire Signaling* section, Figures 5 and 6, *Absolute Maximum Ratings*, and *Electrical Characteristics* table	1–6, 8–11
12/23	Changed WLP package drawing; updated outline and land pattern drawing hyperlinks	1, 11

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