*Click **here** to ask an associate for production status of specific part numbers.*

MAX25206/MAX25207/ MAX25208

Versatile Automotive 60V/70V 2.2MHz Buck Controller with 7µA I_Q and Optional Bypass Mode

General Description

The MAX25206/MAX25207/MAX25208 are automotive 2.2MHz synchronous step-down controllers with 7µA I_Q. These devices operate with an input voltage supply from 3.5V to 60V (MAX25206/MAX25207) and 70V (MAX25208). They can operate in drop-out condition by running at 99% (typ) duty cycle. These controllers are intended for applications with mid- to high-power requirements that operate at a wide input voltage range such as during automotive cold-crank or engine stop-start conditions. The MAX25207 has an optional bypass mode, which allows 100% high-side switch on until step-down function is needed during automotive transients.

The MAX25206/MAX25207/MAX25208 step-down controllers operate at a frequency up to 2.2MHz to allow small external components, reduced output ripple, and to eliminate AM band interference. The switching frequency is resistor adjustable (220kHz to 2200kHz). SYNC input programmability enables three frequency modes for optimized performance: forced fixed-frequency operation (FPWM), skip mode with ultra-low quiescent current, and synchronization to an external clock. The IC also provides SYNCOUT output to enable two controllers to operate in parallel. The MAX25206/MAX25207/MAX25208 have a pin-selectable spread-spectrum option for frequency modulation to minimize EMI.

The MAX25206/MAX25207/MAX25208 feature a PGOOD monitor and undervoltage lockout. Protection features include cycle-by-cycle current limit and thermal shutdown. These controllers are specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- Infotainment Systems
- 48V Systems
- General Purpose Point of Load (POL)

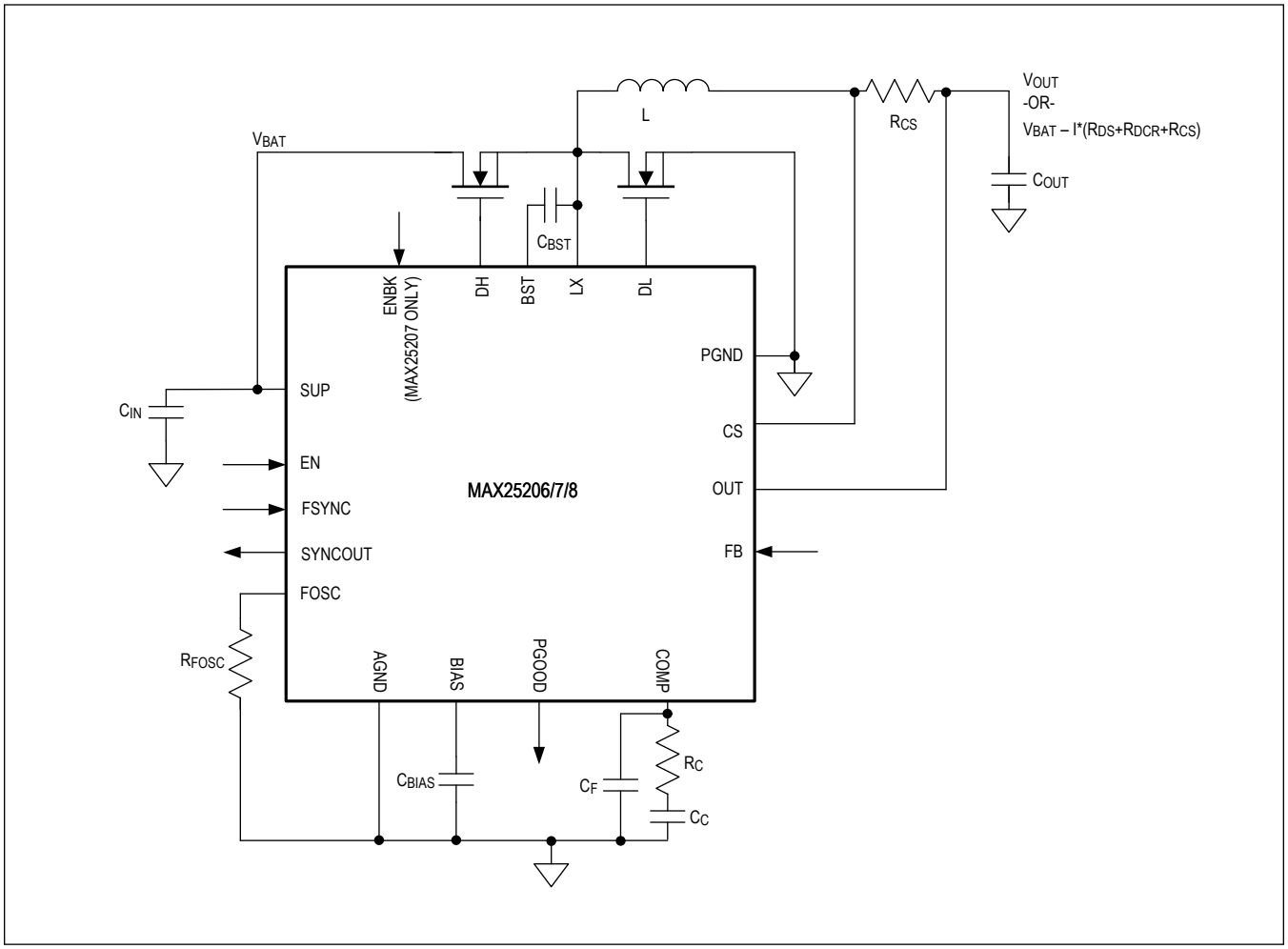
Benefits and Features

- Meets Stringent Automotive OEM Module Power Consumption and Performance Specifications
  - 7µA Quiescent Current in Skip Mode
  - Fixed 5.0V/3.3V or Adjustable 0.7V to 20V Output
  - ±1.5% Output-Voltage Accuracy for 5V Fixed Setting
- Enables Crank-Ready Designs
  - Wide Input Supply Range from 3.5V to 60V/70V
- EMI Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - 50ns (typ) Minimum On-Time Allows Skip-Free Operation for 3.3V Output from Car Battery at 2.2MHz
  - Spread-Spectrum Option
  - Frequency-Synchronization Input
  - Resistor-Programmable Frequency Between 220kHz and 2.2MHz
- Integration and Thermally Enhanced Packages Save Board Space and Cost
  - 2.2MHz Step-Down Controller
  - 180 Degrees Out-of-Phase SYNCOUT Output for Synchronization
  - Current-Mode Controller with Forced-Continuous and Skip Modes
  - Thermally Enhanced 20-Pin Side-Wettable (SW) 4mm x 4mm TQFN-EP Package
- Protection Features Improve System Reliability
  - Supply Undervoltage Lockout
  - Output Overvoltage and Undervoltage Monitoring
  - Overtemperature and Short-Circuit Protection
  - -40°C to +125°C Grade 1 Automotive Temperature Range

Ordering Information appears at end of data sheet.

19-100800; Rev 2; 1/22

Simplified Block Diagram



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LIST OF FIGURES

Absolute Maximum Ratings

SUP, EN, LX to PGND (MAX25206, MAX25207) .... -0.3V to 65V
SUP, EN, LX to PGND (MAX25208) ..... -0.3V to 75V
OUT to AGND..... -0.3V to 22V
CS to OUT ..... -0.3V to 0.3V
SYNCOUT, SPS, FOSC, COMP, FB, ENBK to AGND ....-0.3V to BIAS + 0.3V
BIAS to AGND ..... -0.3V to 6V
PGOOD, FSYNC to AGND..... -0.3V to 6V
DL to PGND ..... -.0.3V to BIAS + 0.3V
BST to LX ..... -0.3V to 6V
DH to LX ..... -0.3V to BST+0.3V
PGND to AGND ..... -0.3V to 0.3V
Package Thermal Characteristics
T2044Y+6C
Continuous Power Dissipation
TQFN (derate 28mW/°C above +70°C) 2260mW
Operating Junction Temperature .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....+260°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: During initial startup, V_{SUP}, rising must cross 6V. The normal operating range is then valid.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to +125	ºC

Note: These limits are not guaranteed.

Package Information

20 SW TQFN

Package Code	T2044Y+6C
Outline Number	21-100388
Land Pattern Number	90-100132
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35.4 ºC/W
Junction to Case (θ_{JC})	4 ºC/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{SUP} = 24V (MAX25206, MAX25207)/48V (MAX25208), V_{EN} = V_{SUP}, C_{SUP} = 4.7µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 2* and *Note 5*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS STEP DOWN CONVERTER						
Supply Voltage Range	V_{SUP}	Normal Operation (MAX25206 and MAX25207) (Note 3)	3.5		60	V
		Normal Operation (MAX25208) (Note 3)	3.5		70	
Output Overvoltage Threshold		Detected with respect to V_{FB} Rising		107		%
		Detected with respect to V_{FB} Falling		105		

Electrical Characteristics (continued)

(V_{SUP} = 24V (MAX25206, MAX25207)/48V (MAX25208), V_{EN} = V_{SUP}, C_{SUP} = 4.7µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 2* and *Note 5*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{SUP}	V_{EN} = 0V		1	6	µA
		V_{EN} = V_{SUP}, V_{OUT} = 5V, No Switching, MAX25206/8		7	11	
		V_{EN} = V_{SUP} = 14V, MAX25207 in bypass mode		3		mA
Buck Fixed Output Voltage	V_{OUT}	V_{FB} = V_{BIAS}, V_{OUT} = 5V, PWM mode (T_J = -40ºC to +125ºC)	4.925	5	5.075	V
		V_{FB} = V_{BIAS}, V_{OUT} = 5V, PWM mode	4.915	5	5.075	
		V_{FB} = V_{BIAS}, V_{OUT} = 5V, skip mode	4.9	5	5.1	
		V_{FB} = V_{BIAS}, V_{OUT} = 3.3V, PWM mode	3.234	3.3	3.366	
		V_{FB} = V_{BIAS}, V_{OUT} = 3.3V, skip mode	3.234	3.3	3.366	
Output Voltage Adjustable Range		Buck	0.7		20	V
Regulated Feedback Voltage	V_{FB}		0.689	0.7	0.715	V
Feedback Leakage Current	I_{FB}	T_A = +25°C		0.01	1	µA
Feedback Line Regulation Error		V_{SUP} = 3.5V to 60V, V_{FB} = 0.7V		0.01		%/V
Transconductance (from FB to COMP)	$g_{m, EA}$	V_{FB} = 0.7V, V_{BIAS} = 5V	220	450	650	µS
Dead Time		DL low to DH Rising		15		ns
		DH low to DL Rising		15		
Max Duty Cycle		Buck	97			%
Minimum On-Time	$t_{ON,MIN}$	Buck		50		ns
PWM Switching Frequency Range	f_{SW}	Programmable	0.22		2.2	MHz
Switching Frequency Accuracy		R_{FOSC} = 12kΩ, V_{BIAS} = 5V, 3.3V	2	2.2	2.4	MHz
CS Current-Limit Voltage Threshold	V_{LIMIT}	V_{CS} – V_{OUT}; V_{BIAS} = 5V, V_{OUT} ≥ 2.5V	71	80	90.5	mV
Soft-Start Ramp Time	$t_{SOFT-START}$	Buck, fixed soft-start time regardless of frequency.		3.7		ms
LX Leakage Current		V_{SUP} = 6V, V_{LX} = V_{PGND} or V_{SUP}, T_A = 25°C		0.01		µA
DH Pullup Resistance		V_{BIAS} = 5V, I_{DH} = -100mA		2.7		Ω
DH Pulldown Resistance		V_{BIAS} = 5V, I_{DH} = 100mA		1		Ω
DL Pullup Resistance		V_{BIAS} = 5V, I_{DL} = -100mA		2.2		Ω
DL Pulldown Resistance		V_{BIAS} = 5V, I_{DL} = 100mA		1		Ω
PGOOD UV Threshold	P_{GOOD_H}	% of target V_{OUT}, Rising		95		%
	P_{GOOD_F}	% of target V_{OUT}, Falling	90.5	93	95.5	

Electrical Characteristics (continued)

(V_{SUP} = 24V (MAX25206, MAX25207)/48V (MAX25208), V_{EN} = V_{SUP}, C_{SUP} = 4.7µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 2* and *Note 5*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Leakage Current		V_{PGOOD} = 5V, T_A = 25°C		0.01	1	µA
PGOOD Output Low Voltage		I_{SINK} = 1mA			0.2	V
PGOOD Debounce Time		OV/UV Fault Detection, Rising and Falling		32		µs
PGOOD Timeout		OTP Option (default 0ms) rising	0.5			ms
Bypass Mode						
Bypass Mode Threshold	V_{BYP}	Rising threshold where buck starts (14V to 18V, 0.5V Steps) MAX25207	-3		3	%
Hysteresis				0.7		V
ENBK Threshold, High	V_{IH}		1.4			V
ENBK Threshold, Low	V_{IL}				0.4	V
ENBK Internal Pulldown				620		kΩ
FSYNC INPUT						
FSYNC Frequency Range		f_{OSC} = 2.2MHz, minimum sync pulse > ($1/f_{SYNC}$ - $1/f_{OSC}$)	1.8		2.6	MHz
		f_{OSC} = 400kHz, minimum sync pulse > ($1/f_{SYNC}$ - $1/f_{OSC}$)	320		480	kHz
		Minimum sync-in pulse	100			ns
FSYNC Switching Thresholds		High Threshold	1.4			V
		Low Threshold			0.4	V
INTERNAL LDO BIAS						
Internal BIAS Voltage		V_{SUP} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} Rising		3.1	3.5	V
		V_{BIAS} Falling	2.6	2.8		
THERMAL OVERLOAD						
Thermal Shutdown Temperature		T_J rising (Note 4)		165		°C
Thermal Shutdown Hysteresis		(Note 4)		20		°C
Logic Levels						
EN High Threshold		EN	1.4			V
EN Low Threshold		EN			0.4	V
EN Input Bias Current		EN logic input only, T_A = 25°C		0.01	1	µA
SPS Threshold, High	$V_{IH,SPS}$		1.4			V
SPS Threshold, Low	$V_{IL,SPS}$				0.4	V
SPS Internal Pulldown				620		kΩ
SYNCOUT and Spread Spectrum Logic						
SYNCOUT Low Voltage		I_{SINK} = 5mA			0.4	V

Electrical Characteristics (continued)

(V_{SUP} = 24V (MAX25206, MAX25207)/48V (MAX25208), V_{EN} = V_{SUP}, C_{SUP} = 4.7µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 2* and *Note 5*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCOUT Leakage Current		T_A = 25°C			1	µA
Spread Spectrum				±6		% of f_{OSC}

Note 2: Limits are 100% production tested at T_A = +25ºC. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization.

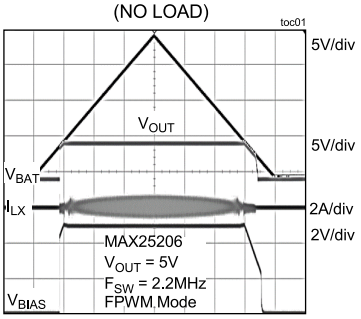
Note 3: During initial startup, V_{SUP}, rising must cross 6V. The normal operating range is then valid.

Note 4: Guaranteed by design; not production tested.

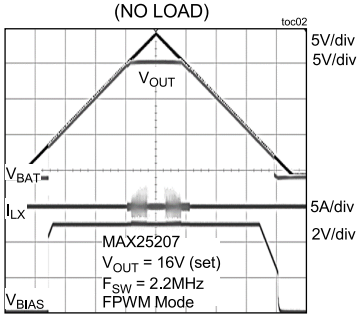
Note 5: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Typical Operating Characteristics

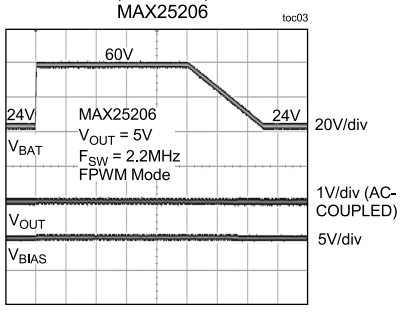
SLOW VIN RAMP
(NO LOAD)



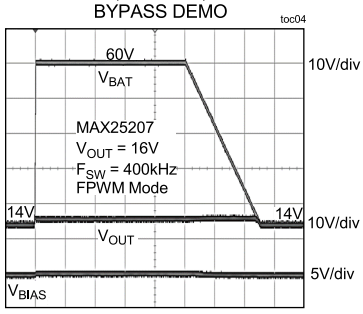
SLOW VIN RAMP
(NO LOAD)



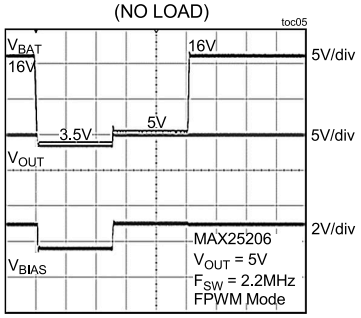
LOAD DUMP TEST
(NO LOAD)
MAX25206



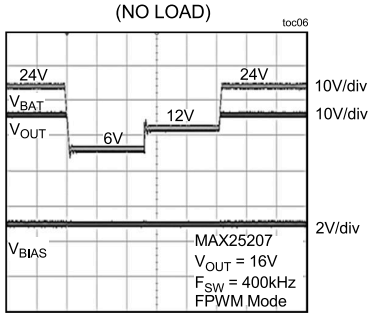
LOAD DUMP TEST
(NO LOAD)
BYPASS DEMO



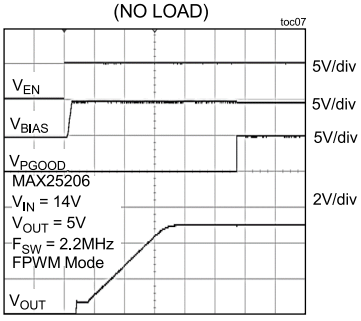
CRANK TEST
(NO LOAD)



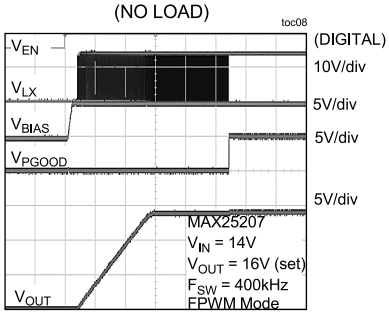
CRANK TEST
(NO LOAD)



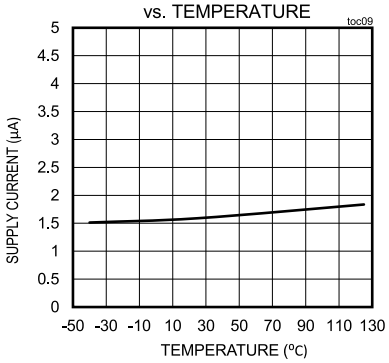
STARTUP WAVEFORM
(NO LOAD)



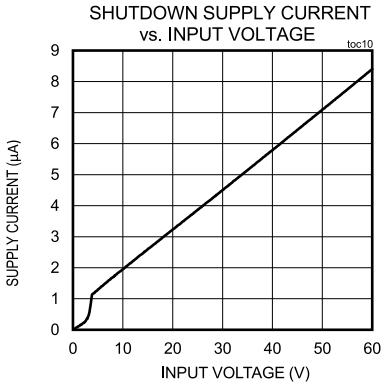
STARTUP WAVEFORM
(NO LOAD)

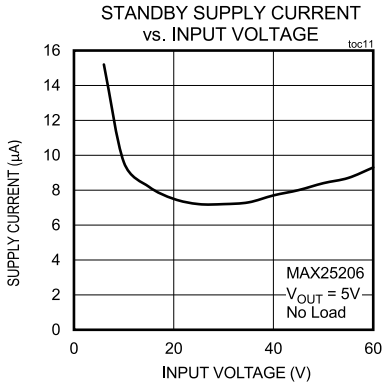


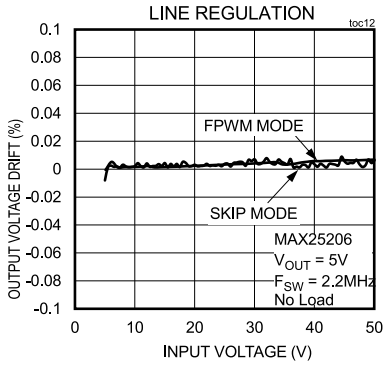
SHUTDOWN SUPPLY CURRENT
vs. TEMPERATURE

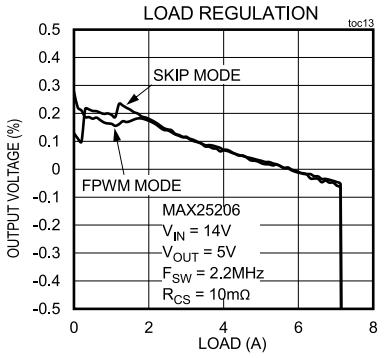


Typical Operating Characteristics (continued)



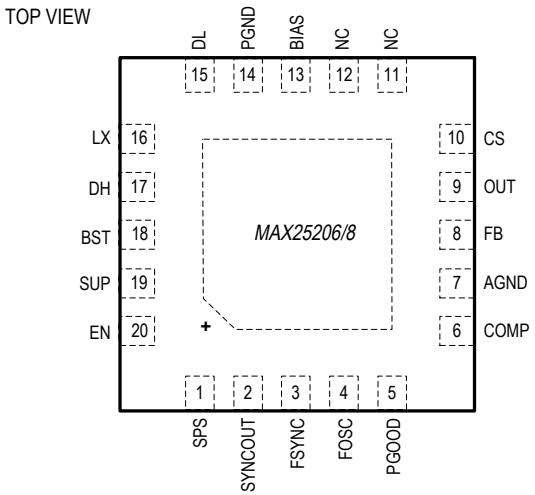






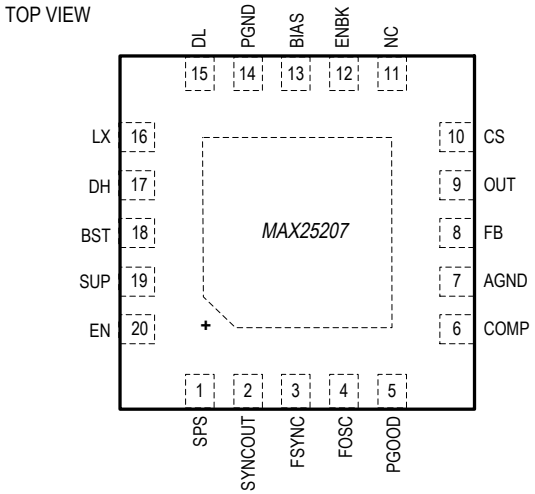
Pin Configurations

MAX25206/MAX25208



TQFN
4mm × 4mm

MAX25207



TQFN
4mm × 4mm

Pin Description

PIN		NAME	FUNCTION
MAX25206/ MAX25208	MAX25207		
1	1	SPS	Spread Spectrum Enable Pin. Pull to logic high for spread spectrum enabled. Pull to ground to disable spread spectrum.

Pin Description (continued)

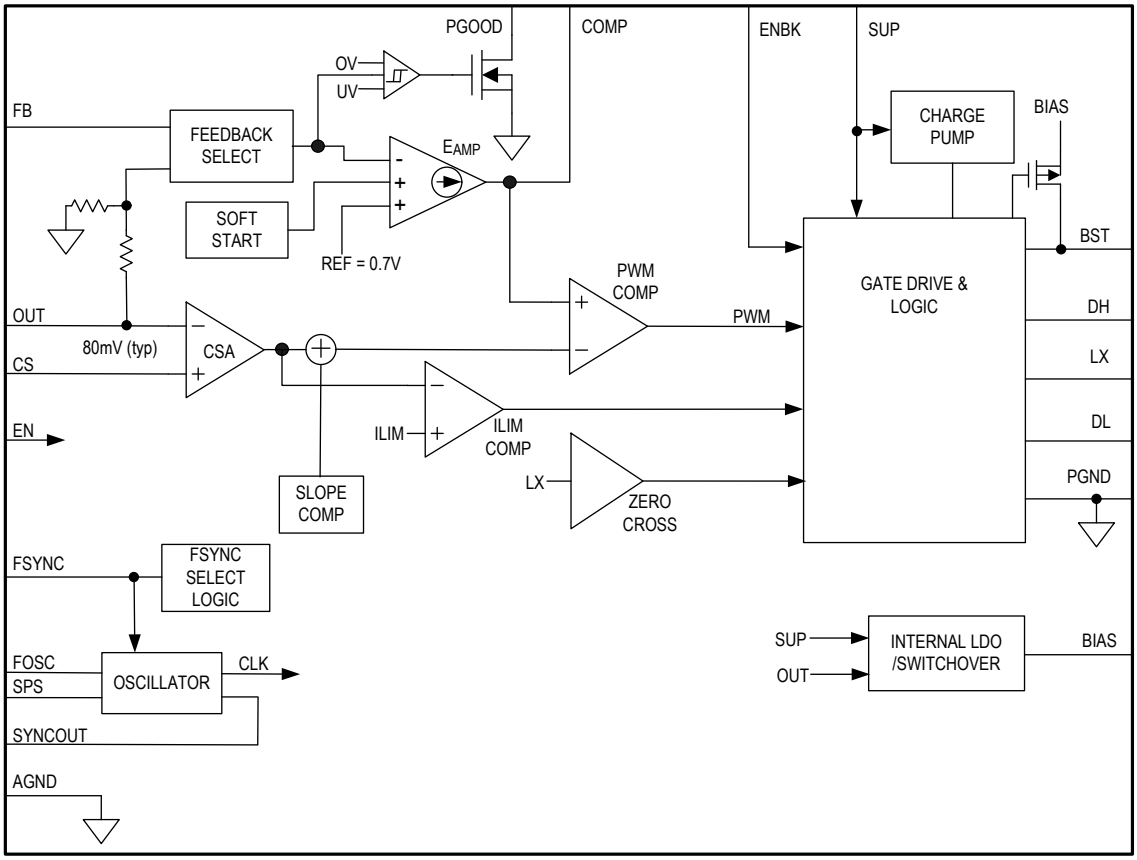
PIN		NAME	FUNCTION
MAX25206/ MAX25208	MAX25207		
2	2	SYNCOUT	Clock Output. SYNCOUT outputs 180 degrees out of phase relative to the internal oscillator.
3	3	FSYNC	External Clock Synchronization Input. Connect FSYNC to AGND to enable skip mode of operation (MAX25206/MAX25208 only). Connect to BIAS or an external clock to enable forced-PWM mode of operation. Tie FSYNC high for MAX25207. If external clock synchronization is required for MAX25207, contact factory for review. See *Switching Frequency/External Synchronization* section for additional information.
4	4	FOSC	Frequency Setting Input. Connect a resistor to FOSC to set the switching frequency of the DC-DC controller.
5	5	PGOOD	Open-Drain Power-Good Output for Buck Controller. PGOOD asserts low during soft-start and in shutdown. PGOOD becomes high impedance when OUT is in regulation. Actively pulled down if OUT is outside the regulation window. For MAX25207, PGOOD is always high impedance in bypass mode. To obtain a logic signal, pull up PGOOD with an external resistor connected to a positive voltage lower than 5.5V.
6	6	COMP	Buck Controller Error Amplifier Output. Connect an RC network between COMP and AGND to compensate the buck controller.
7	7	AGND	Analog Ground for Controller
8	8	FB	Feedback Input for Buck Controller. Connect FB to BIAS for the fixed output or to a resistor divider between OUT and GND to adjust the output voltage between 0.7V and 20V. In adjustable mode, FB regulates to 0.7V (typ).
9	9	OUT	Output Sense and Negative Current-Sense Input for Buck Controller. When using the internal preset 5V feedback-divider (FB = BIAS), the controller uses OUT to sense the output voltage. Connect OUT to the negative terminal of the current-sense element. See *Current Limiting and Current Sense Inputs* and *Current Sense Measurement* sections.
10	10	CS	Positive Current-Sense Input for Buck Controller. Connect CS to the positive terminal of the current-sense element. See *Current Limiting and Current Sense Inputs* and *Current Sense Measurement* sections.
11	11	NC	No Connect
12	12	NC/ENBK	Force Buck Mode Pin. For bypass-enabled part MAX25207, pull to logic high to force buck mode, pull to ground to let the part decide operation mode (buck or bypass) based on supply voltage. Connect to ground for MAX25206/MAX25208.
13	13	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to GND with a low-ESR ceramic capacitor of 2.2µF minimum value. BIAS provides the power to the internal circuitry and gate drivers. See *Fixed 5V Linear Regulator (BIAS)* and *BIAS Switchover* sections.
14	14	PGND	Power Ground for Controller
15	15	DL	Low-Side Gate Driver Output. DL output voltage swings from V_{PGND} to V_{BIAS}.
16	16	LX	Inductor Connection. Connect LX to the switched side of the inductor.
17	17	DH	High-Side Gate Driver Output
18	18	BST	Bootstrap capacitor connection. Connect a ceramic capacitor between BST and LX. See *High-Side Gate-Driver Supply (BST)* section.
19	19	SUP	Supply Input for IC. Bypass to ground with a 2.2µF or larger capacitor near the IC. Connect to buck power stage input voltage (V_{IN}). Power stage needs additional input capacitors (C_{IN}).

Pin Description (continued)

PIN		NAME	FUNCTION
MAX25206/ MAX25208	MAX25207		
20	20	EN	High-Voltage Tolerant, Active-High Digital Enable Input for Controller.
EP	EP	–	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND, AGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Functional Diagrams

Block Diagram



Detailed Description

The MAX25206/MAX25207/MAX25208 are automotive 2.2MHz synchronous step-down controller ICs with 5V/3.3V fixed or adjustable 0.7V to 20V output voltage. The MAX25207 offers a bypass mode that delivers high-efficiency, high-side switch-on mode.

In skip mode (MAX25206/8), with no load, the total supply current is reduced to 7µA (typ). When the controller is disabled, the total current drawn is further reduced to 1µA (typ).

To enable the IC, connect EN directly to V_{SUP}, or to a power-supply sequencing logic.

Fixed 5V Linear Regulator (BIAS)

The internal circuitry of the IC requires a 5V bias supply. An internal 5V linear regulator (BIAS) generates this supply. Bypass BIAS to PGND with a 2.2µF or greater ceramic capacitor.

The BIAS linear regulator can source up to 100mA for internal logic, DH, and DL drivers. The internal current consumption in the IC is estimated using the following equation:

$$I_{BIAS} = I_{CC} + f_{SW} \times (QG_{DH} + QG_{DL}) = 20mA\ to\ 50mA\ (typ)\ \ for\ \ 400kHz$$

where I_{CC} is the internal supply current (3mA, typ), f_{SW} is the switching frequency. QG_{DH} is the gate charge of the upper MOSFET, and QG_{DL} is the gate charge of the lower MOSFET. The BIAS linear regulator is not intended for powering external loads.

BIAS Switchover

The MAX25206/MAX25208 have a BIAS switchover option available to reduce the power dissipation in the internal BIAS regulator if the target output voltage is in the BIAS switchover range (3.1V to 5.2V). In BIAS switchover, the internal BIAS regulator is switched off and the BIAS is supplied from the OUT pin.

The MAX25207 does not feature BIAS switchover.

See the *Ordering Information* table to check the BIAS switchover settings on the MAX25206/08. The external FET gate drive voltage should be a factor while using a switchover part.

Undervoltage Lockout (UVLO)

The BIAS undervoltage-lockout (UVLO) circuitry inhibits switching if the BIAS voltage is below the BIAS UVLO threshold. Once BIAS rises above its UVLO rising threshold and EN is high, the controller starts switching and the output is allowed to ramp up.

Buck Controller

The IC provides a buck controller with synchronous rectification. The step-down controller uses a PWM, current-mode control scheme. External MOSFETs allow for optimized load-current design. Output-current sensing provides an accurate current limit with an external sense resistor, or power dissipation can be reduced by using lossless current sensing across the inductor.

Bypass Mode

To maximize the efficiency of the front-end conversion stage, the MAX25207 comes with a bypass mode. The IC enters bypass mode when the input voltage falls 0.7V below the bypass threshold ($V_{SUP} < V_{BYP} - 0.7V$). In this mode, the IC utilizes an internal charge pump to maintain 100% duty cycle on the high-side MOSFET. When $V_{SUP} > V_{BYP}$, the IC quickly resumes buck mode operation and regulates the output voltage.

The MAX25207 allows the customer to achieve high efficiency (no switching) at normal battery voltage (bypass mode) and provides a regulated output voltage during high line conditions. This protects the downstream parts from high voltage battery transients. The MAX25207 also comes with an Enable Buck (ENBK) logic input which forces buck mode operation regardless of V_{SUP} when driven high. See the *Bypass Timing Diagram* for valid states and corresponding output.

Bypass Timing Diagram

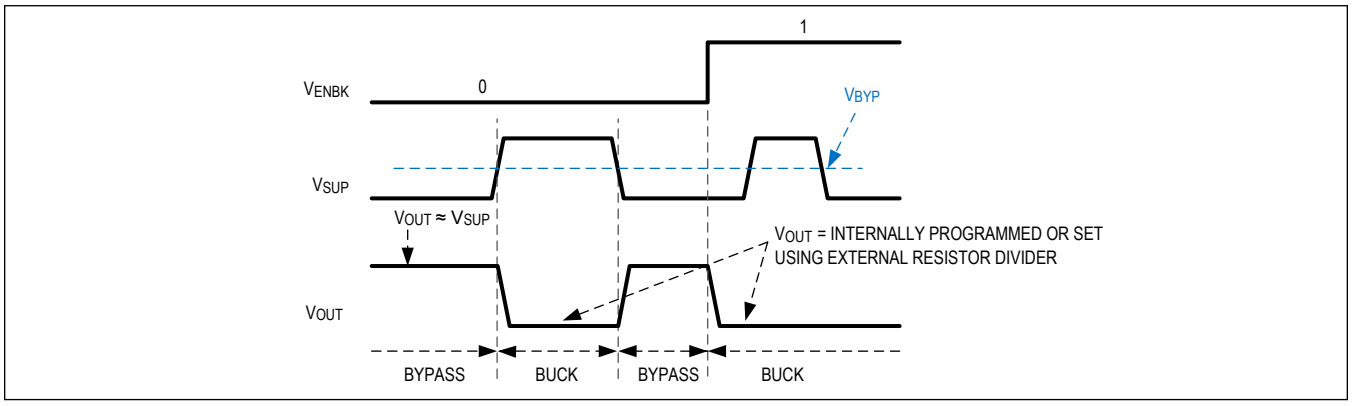


Figure 1. Bypass Timing

V_{BYP}: Bypass voltage threshold. This is an OTP programmable threshold for bypass decision making in MAX25207.

V_{OUT}: Output voltage. Buck mode output voltage is internally programmed or set using external resistor divider. Bypass mode output voltage is approximately equal to the supply voltage.

V_{ENBK}: Enable Buck. A logic high at ENBK pin forces buck mode regardless of V_{SUP}.

Soft-Start

The soft-start circuitry gradually ramps up the reference voltage during soft-start time ($t_{SOFT-START}$) to reduce the input inrush current during startup. Before the device can begin soft-start, the following conditions must be met:

- V_{BIAS} exceeds the BIAS UVLO threshold
- V_{EN} is logic high

During soft-start, PGOOD asserts low until an internal Soft-Start Done signal is received.

The MAX25207 always starts up in buck mode. The bypass mode determination is made after soft-start is complete.

Switching Frequency/External Synchronization

The IC provides an internal oscillator, adjustable from 220kHz to 2.2MHz, set with an external resistor connected to FOSC. High-frequency operation results in smaller component size at the cost of higher switching losses. Low-frequency operation offers the best overall efficiency at the expense of component size and board space. To set the switching frequency, connect a resistor (R_{FOSC}) from FOSC to AGND:

$$R_{FOSC} = \frac{400kHz \times 66k\Omega}{f_{OSC}}\left[1 + 60ns \times (2.2MHz - f_{OSC})\right]$$

where f_{OSC} is in Hz and R_{FOSC} is in Ω.

The IC can be synchronized to an external clock by connecting the external clock signal to FSYNC. A rising edge on FSYNC resets the internal clock. Keep the FSYNC frequency ±20% of the internal frequency.

The ICs can be used in parallel for multiphase operation when high power is required. Multiphase operation includes one master IC and one or more slave ICs. Synchronization is achieved by connecting the master IC's clock output SYNCOUT to the slave ICs' clock input FSYNC. Connect the COMP pin of the slave IC to that of the master. The error amplifier of the slave IC is disabled and the master IC will drive compensation adjustments. (Contact factory for slave versions of the IC)

Skip Mode for Light-Load-Efficiency

Drive FSYNC low to enable skip mode. In skip mode, the inductor current is not allowed to turn negative. Once inductor current reaches zero, the low-side MOSFET is turned off. The high-side MOSFET is not turned on again until FB voltage drops below the reference voltage. Once FB voltage drops below the reference voltage, the high-side MOSFET is turned

on until the inductor current reaches 20% of the current limit threshold.

Forced-PWM Mode

Driving FSYNC high or external synchronization prevents the IC from entering skip mode by disabling the zero-crossing detection of the inductor current. This allows the inductor current to reverse at light load and during transients.

Forced-PWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands.

Maximum Duty-Cycle Operation in Buck Mode

The IC has a maximum duty cycle of 99% (typ) (97% (min)) in buck mode. In maximum duty cycle operation, the internal logic of the IC monitors approximately 10 consecutive high-side FET ON pulses and then turns on the low-side FET for 150ns (typ) every 12µs if bypass mode is not selected. The input voltage at which the IC enters this dropout condition changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the IC enters dropout can be approximated using the following equation:

$$V_{IN} \approx \frac{V_{OUT} + I_{OUT}\left(R_{DS(ON)} + R_{DCR}\right)}{0.97}$$

where $R_{DS(ON)}$ is the on-resistance of the high-side MOSFET.

Spread Spectrum

The IC features enhanced EMI performance. It performs ±6% dithering of the switching frequency to reduce peak emission noise at the clock frequency and its harmonics, making it easier to meet stringent emission limits. A logic high on SPS pin enables spread spectrum. Using external clock source (e.g., driving the FSYNC input with an external clock) disables spread spectrum.

MOSFET Gate Drivers (DH and DL)

The high-side n-channel MOSFET driver (DH) is powered from capacitor at BST, while the low-side driver (DL) is powered from BIAS. In BIAS switchover operation, the gate drive supply voltage may be low depending on the target V_{OUT}. The impact of low gate drive voltage in BIAS switchover designs should be considered when selecting MOSFETs. A shoot-through protection circuit monitors the gate-to-source voltage of the external MOSFETs to prevent simultaneous turn on of high-side and low-side MOSFETs. There must be a low-resistance, low-inductance forward and return path from the drivers to the MOSFET gates for the protection circuits to work properly.

It may be necessary to decrease the slew rate for the gate drivers to reduce switching noise. For the high-side driver, connect a small 1Ω to 5Ω resistor between DH and the gate of the high-side MOSFET. For the low-side driver, use a 1Ω resistor between DL and the gate of the low-side MOSFET.

High-Side Gate-Driver Supply (BST)

The high-side MOSFET driver is supplied by a bootstrap capacitor (C_{BST}) connected between BST and LX pins. C_{BST} re-charges from BIAS, through an internal switch, when the low-side MOSFET is on bringing LX to ground. For MAX25207 in bypass mode, C_{BST} is kept charged using an internal charge pump.

The bootstrap capacitance (C_{BST}) is selected to limit the voltage drop on C_{BST} during high-side MOSFET turn on, as given by:

$$C_{BST} = QG / \Delta V_{BST}$$

where QG is the total gate charge of the high-side MOSFET and ΔV_{BST} (100mV to 300mV) is the voltage ripple on C_{BST}. A 100nF low-ESR ceramic capacitor is sufficient in most cases.

Current Limiting and Current-Sense Inputs (OUT and CS)

The current-sense amplifier (CSA) uses differential current-sense inputs (OUT and CS) to sense the inductor current. For normal buck operation, this sensed signal is used for peak current mode control. If the current-sense signal exceeds the current-limit threshold (V_{LIMIT} = 80mV (typ)), the PWM controller turns off the high-side MOSFET. The maximum

load current is less than the peak current-limit threshold by half the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT}/V_{IN}).

For accurate current sensing, use a current-sense shunt resistor (R_{CS}) between the inductor and the output capacitor. Connect CS to the inductor side of R_{CS} and OUT to the output capacitor side. Select R_{CS} such that

$$I_{LOAD} + \frac{\Delta I_L}{2} < \frac{V_{LIMIT}}{R_{CS}}$$

where ΔI_L is the inductor current ripple.

Inductor DCR sensing can be used for higher efficiency but can result in up to 30% error in current limit threshold due to variation in inductor DCR over temperature. See *Current-Sense Measurement* for information on DCR sensing network design.

Voltage Monitoring (PGOOD)

PGOOD is an open-drain power-good output that indicates the status of output voltage regulation. When the part is enabled (EN = High), PGOOD is actively pulled low during soft-start ramp time. Once soft-start is done and the output is in regulation, PGOOD goes high impedance after about 2ms (typ) delay. When the output voltage falls out of regulation (see PGOOD UV and Overvoltage Threshold), PGOOD goes low after PGOOD debounce time.

Connect at 10 kΩ (typ) pull up resistor from PGOOD to the relevant logic rail. To ensure PGOOD is low when buck is disabled (EN = Low), use BIAS as the pull up voltage source. Alternatively, when using an external logic rail as a pull up source for PGOOD, EN and PGOOD can be used together in the system logic to infer status of output voltage.

For the MAX25207, PGOOD is always high impedance in bypass mode.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the IC. When the junction temperature exceeds +165°C, an internal thermal sensor shuts down the IC, allowing it to cool. The thermal sensor turns on the IC again after the junction temperature cools by 20°C.

Overcurrent Protection

If the sensed voltage across CS/OUT exceeds the current limit threshold (V_{LIMIT} = 80mV (typ)), the high-side driver (DH) turns off and the low-side driver (DL) turns on. The high side MOSFET does not turn on again until voltage across CS/OUT drops below the current-limit threshold.

The MAX25207 continues to offer current-limit protection in bypass mode.

The part enters hiccup mode if the output voltage falls below the hiccup threshold (50% of target V_{OUT} for the MAX25206/MAX25208, 20% of target V_{OUT} for the MAX25207).

Overvoltage Protection

In case of an overvoltage on the output, the controller turns off high- and low-side MOSFET drivers (DH/DL). Switching resumes when the output voltage comes back into regulation.

Applications Information

Design Procedure

Effective Input Voltage Range in the Buck Converter

Although the IC can operate from input supplies up to 60V/70V and regulate down to 0.7V, the minimum voltage conversion ratio for fixed frequency operation is limited by the minimum controllable on-time ($t_{ON,MIN}$):

$$\frac{V_{OUT}}{V_{IN}} > t_{ON,\,MIN} \times f_{SW}$$

where f_{SW} is the switching frequency. If the desired voltage conversion does not meet the above condition, pulse skipping occurs to maintain regulation. Decrease the switching frequency if constant switching frequency is required at higher input voltages.

The maximum voltage conversion ratio in buck mode of operation is limited by the maximum duty cycle (see *Maximum Duty-Cycle Operation in Buck Mode*). During low-drop operation, the IC reduces the switching frequency (f_{SW}) to ~80kHz.

The MAX25207 provides 100% duty cycle operation in bypass mode.

Setting the Output Voltage

Connect FB to BIAS to enable the fixed buck-controller output voltage (5V or 3.3V) set by a preset internal resistor voltage-divider connected between OUT and AGND. To externally adjust the output voltage between 0.7V and 20V, connect a resistor divider from the output (OUT) to FB to AGND.

$$\frac{R_{FB2}}{R_{FB1}} = \left(\frac{V_{OUT}}{V_{FB}}\right) - 1$$

where V_{FB} = 0.7V (typ) (see the *Electrical Characteristics*) and R_{FB2}, R_{FB1} are top and bottom resistors in the feedback divider.

In skip mode, the IC regulates the valley of the output ripple.

Inductor Selection

The inductor is selected based on trade-off among size, cost, efficiency, and transient performance. A good starting point for inductance comes from targeting 30% peak-to-peak ripple current to average current ratio. The switching frequency, input voltage, output voltage, and target ripple are related to inductance as shown below:

$$L = \frac{\left(V_{IN} - V_{OUT}\right) \times D}{f_{SW} \times I_{OUT} \times 30\,\%}$$

where D (=V_{OUT}/V_{IN}) is the duty cycle. V_{IN}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions).

The inductance must satisfy the slope compensation criterion:

$$V_{SLOPE} f_{SW} > \frac{V_{OUT}}{2 \times L} A_{VCS} R_{CS}$$

where A_{VCS} is the current-sense amplifier gain (typical 13V/V). V_{SLOPE} is V_{OUT} dependent and is given by the following equation:

$$\begin{aligned} V_{SLOPE} &= 105\text{mV for } 0V < V_{OUT} \le 3V \\ &= 210\text{mV for } 3V < V_{OUT} \le 5.5V \\ &= 420\text{mV for } 5.5V < V_{OUT} \le 9.7V \\ &= 525\text{mV} \quad \text{otherwise} \end{aligned}$$

Peak Inductor Current

The peak inductor current is the sum of maximum load current and half of the peak-to-peak ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

For the selected inductance value, the actual peak-to-peak inductor ripple current (ΔI_L) is calculated using the following equation:

$$\Delta I_L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN} \times f_{SW} \times L}$$

The saturation current should be larger than I_{PEAK} or at least in a range where the inductance does not degrade significantly. The MOSFETs are required to handle the same peak current.

MOSFET Selection in Buck Converter

The high- and low-side n-channel MOSFETs should be selected to have sufficient voltage and current ratings. In addition, they should be able to handle the heat generated and temperature rise.

Both high- and low-side MOSFETs should be rated for maximum input voltage observed in the application. Provide additional margin for switch node ringing during switching.

Select MOSFETs with logic-level gate drive with guaranteed on-resistance specifications at V_{GS} = 4.5V. If BIAS switchover is enabled, the gate drive supply voltage follows V_{OUT}. In those cases, select MOSFETs to have guaranteed on-resistance at the lowest BIAS switchover voltage.

To reduce switching noise for smaller MOSFETs, use a series resistor in the BST path and additional gate capacitance. Contact factory for guidance using gate resistors.

Current-Sense Measurement

For best current-sense accuracy and overcurrent protection, use a ±1% tolerance current-sense resistor between the inductor and output, as shown in Figure 2 (A). This configuration continuously monitors inductor current, allowing accurate current-limit protection. Use low-inductance current-sense resistors for accurate measurement.

Alternatively, high-power applications can reduce the overall power dissipation by connecting a DCR sensing network across the inductor Figure 2 (B). Select DCR network based on the following equations:

$$R_{CSHL} = \left(\frac{R_2}{R_1 + R_2}\right) R_{DCR} \text{ and } R_{DCR} = \frac{L}{C_{eq}}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

where R_{CSHL} is the required current-sense resistor based on the current-limit threshold (V_{LIMIT}) and R_{DCR} is the inductor DC resistance. If DCR sense is the preferred current-sense method, select R1 ≤ 1kΩ. See Figure 2 (B).

Carefully observe the *Layout Recommendations* to ensure the noise and DC errors do not corrupt the differential current-sense signals seen by CS and OUT. Place the sense resistor close to the controller CS/OUT pins with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

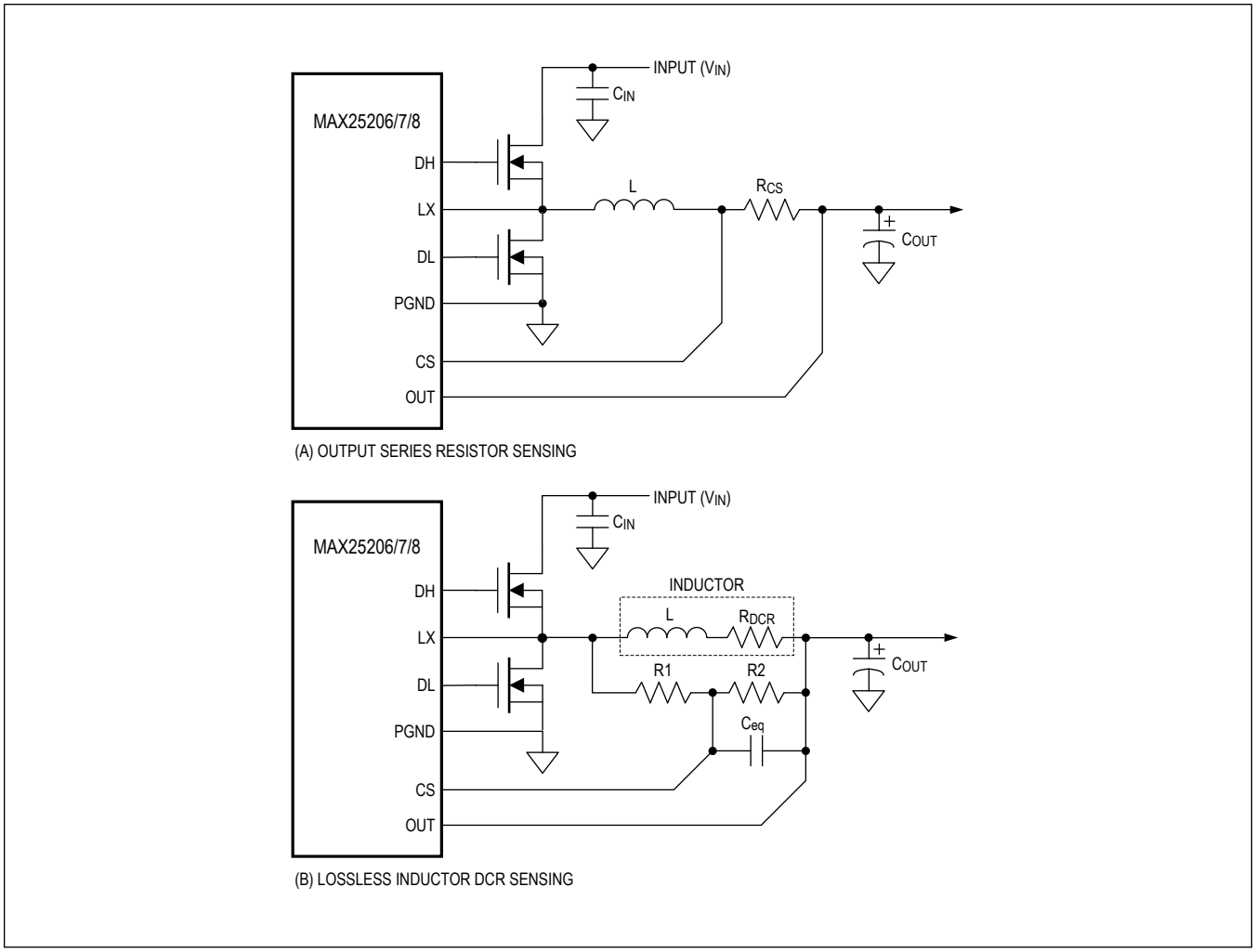


Figure 2. Current-Sense Configurations

Input Capacitor in Buck Converter

Select input capacitor to satisfy the following conditions

- Withstand input ripple current in buck power stage
- Limit the input voltage ripple

The RMS current in the input capacitor is given by:

$$I_{CIN.RMS} = I_{LOAD(MAX)}\sqrt{D \times (1 - D)}$$

The input voltage ripple is composed of $\Delta V_{IN.C}$ (caused by the capacitor discharge) and $\Delta V_{IN.ESR}$ (caused by the ESR of the input capacitor) given by:

$$\Delta V_{IN.C} = \frac{I_{LOAD(MAX)} \times D(1 - D)}{C_{IN} \times f_{SW}} \text{ and } \Delta V_{IN.ESR} = ESR_{CIN}\left(I_{LOAD(MAX)} + \frac{\Delta I_L}{2}\right)$$

$I_{LOAD(MAX)}$ is the maximum output current, ΔI_L is the peak-to-peak inductor current ripple, and C_{IN} is the input capacitor.

The internal 5V linear regulator (BIAS) includes an output UVLO with hysteresis to avoid unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. At lower input voltages, additional input capacitance helps avoid possible undershoot below the undervoltage lockout threshold during transient loading.

Output Capacitor in Buck Converter

The output capacitor is selected to meet ripple requirements, both in steady state and during transients. Low ESR ceramic capacitors can be utilized.

The steady state output ripple has capacitive and ESR based components given by:

$$\Delta V_{OUT.C} = \frac{1}{8} \frac{\Delta I_L}{f_{sw} C_{OUT}} \quad \text{and} \quad \Delta V_{OUT.ESR} = \Delta I_L \times ESR_{COUT}$$

When using low-capacity filter capacitors, such as ceramic capacitors, capacitor selection is usually driven by the need to limit undershoot and overshoot during load transients. The design should be verified in the lab to ensure undershoot and overshoot requirements are met.

Control Loop / Compensation

The IC uses a peak current-mode control scheme that regulates the output voltage by controlling the required current through the external inductor. Current mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control.

A single series resistor (R_C) and capacitor (C_C) is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (see Figure 3). For high-ESR (non-ceramic) output capacitors, the zero created by the capacitance and ESR can be close to or lower than the desired closed-loop crossover frequency. To stabilize a high-ESR (non ceramic) output capacitor loop, add another compensation capacitor (C_F) from COMP to AGND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier as shown in Figure 3. The DC gain of the modulator is given by:

$$GAIN_{MOD(DC)} = g_{mc} \times R_{LOAD}$$

where $R_{LOAD} = V_{OUT}/I_{LOAD(MAX)}$ in Ω and $g_{mc} = 1/(A_{VCS} \times R_{CS})$ in S. A_{VCS} is the voltage gain of the current-sense amplifier and is typically 13V/V. R_{CS} is current-sense resistor in Ω. When using DCR sensing network, replace R_{CS} with R_{CSHL}.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

The output capacitor and its ESR also introduce a zero given by:

$$f_{zMOD} = \frac{1}{2\pi \times ESR_{COUT} \times C_{OUT}}$$

When C_{OUT} is composed of “n” identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$, and $ESR_{COUT} = ESR_{COUT(EACH)}/n$. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 0.7V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m,EA} \times R_{OUT,EA}$, where $g_{m,EA}$ is the error amplifier transconductance, which is 450µS (typ), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 30MΩ (typ).

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{zEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by the compensation capacitor to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C, where the loop gain equals 1 (0dB)).

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times \left(R_{OUT,EA} + R_C\right)} \qquad f_{zEA} = \frac{1}{2\pi \times C_C \times R_C} \qquad f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5th of the switching frequency and much higher than the power-modulator pole (f_{pMOD}). Select a value for f_C in the range shown below:

$$f_{pMOD} \ll f_C \leq \frac{f_{SW}}{5}$$

At the crossover frequency, the total loop gain is unity. Select R_C based on the target crossover frequency:

$$R_C = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi}{g_{m,EA}} \times A_{VCS} R_{CS} \times C_{OUT}$$

Set the error-amplifier compensation zero formed by R_C and C_C at f_{pMOD}:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor C_F from COMP to AGND using the equation below:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole frequency also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

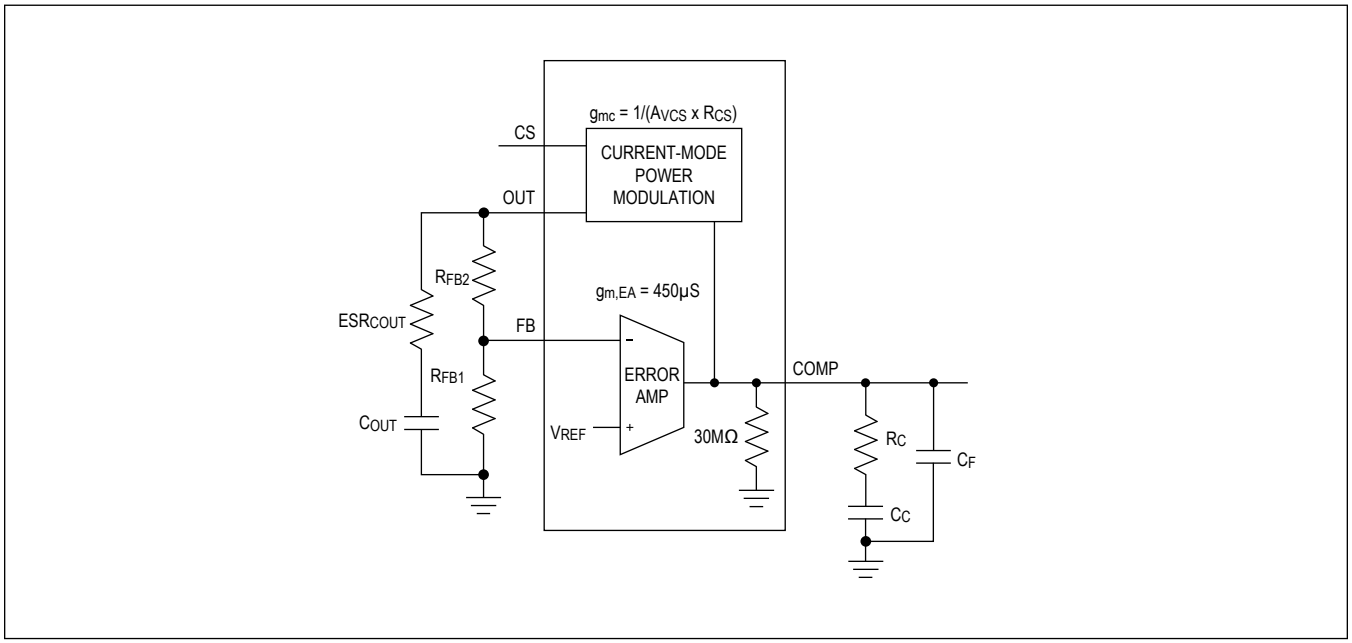


Figure 3. Compensation Network

Layout Recommendations

PCB layout is critical for stable operation, low noise, and high efficiency. Use the checklist below to achieve good circuit performance (See Figure 4 for an example):

- Place the input capacitor (C_{IN}), the high-side MOSFET (QH), and the low-side MOSFET (QL) so that the "input loop" area involving high di/dt is minimized.
- Use low-ESR/ESL ceramic capacitors (C_{IN}) close to the input loop. Bulk capacitor can be further away.
- Place the output capacitors (C_{OUT}) so that input and output capacitor grounds are close together. In addition, connect this common ground connection to ground plane layer(s) using multiple vias.
- Use short and wide traces/areas for high current paths (V_{IN}, V_{OUT}, LX, PGND). If possible, run them on multiple layers in parallel to minimize resistance.
- Minimize the area of high dv/dt nodes (LX) to the extent permitted by heating considerations.
- Route gate drive forward and return paths together using short and wide traces to minimize loop impedance.

Wherever possible, use traces wider than 25 mils for outer layers and 50 mils for inner layers.

- High-side gate charging path includes C_{BST}. Place C_{BST} as close to the IC pins (BST/LX) as possible.
- Low-side gate charging path includes C_{BIAS}. Place C_{BIAS} as close to the IC pins (BIAS/PGND) as possible.
- Low-side gate charge/discharge path includes PGND. Ensure that a continuous PGND plane is present under DL path.
- Place the sense resistor (R_{CS}) close to the CS/OUT pins. Use Kelvin connections across the sense resistor (R_{CS}) and route differentially to the IC pins (CS/OUT). Make the sense traces as short as possible. Place a 22nF capacitor near the CS/OUT pins to minimize noise due to sense trace inductance.
- Use AGND as the reference ground for sensitive analog signals (FB, COMP). Connect the ground side of the bottom feedback resistor (R_{FB1}) and compensation components (C_C, C_F) to AGND.
- Route sensitive traces (FB, CS/OUT) away from noisy (high dv/dt and di/dt) areas (BST, LX, DH, DL).
- Connect AGND/PGND under the IC at one point (Figure 4).
- Connect IC exposed pad through multiple vias to ground plane layer(s).
- Use thicker copper (preferably 2oz/ft^2) for higher current designs for better efficiency and thermal performance.

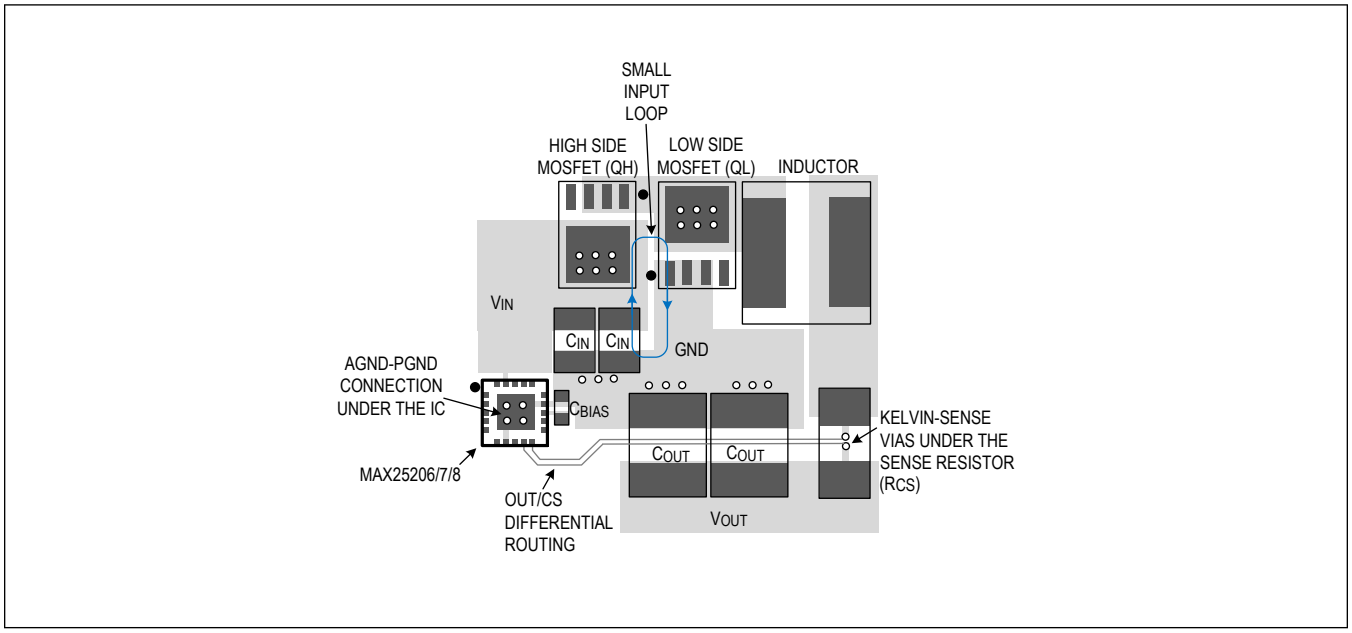
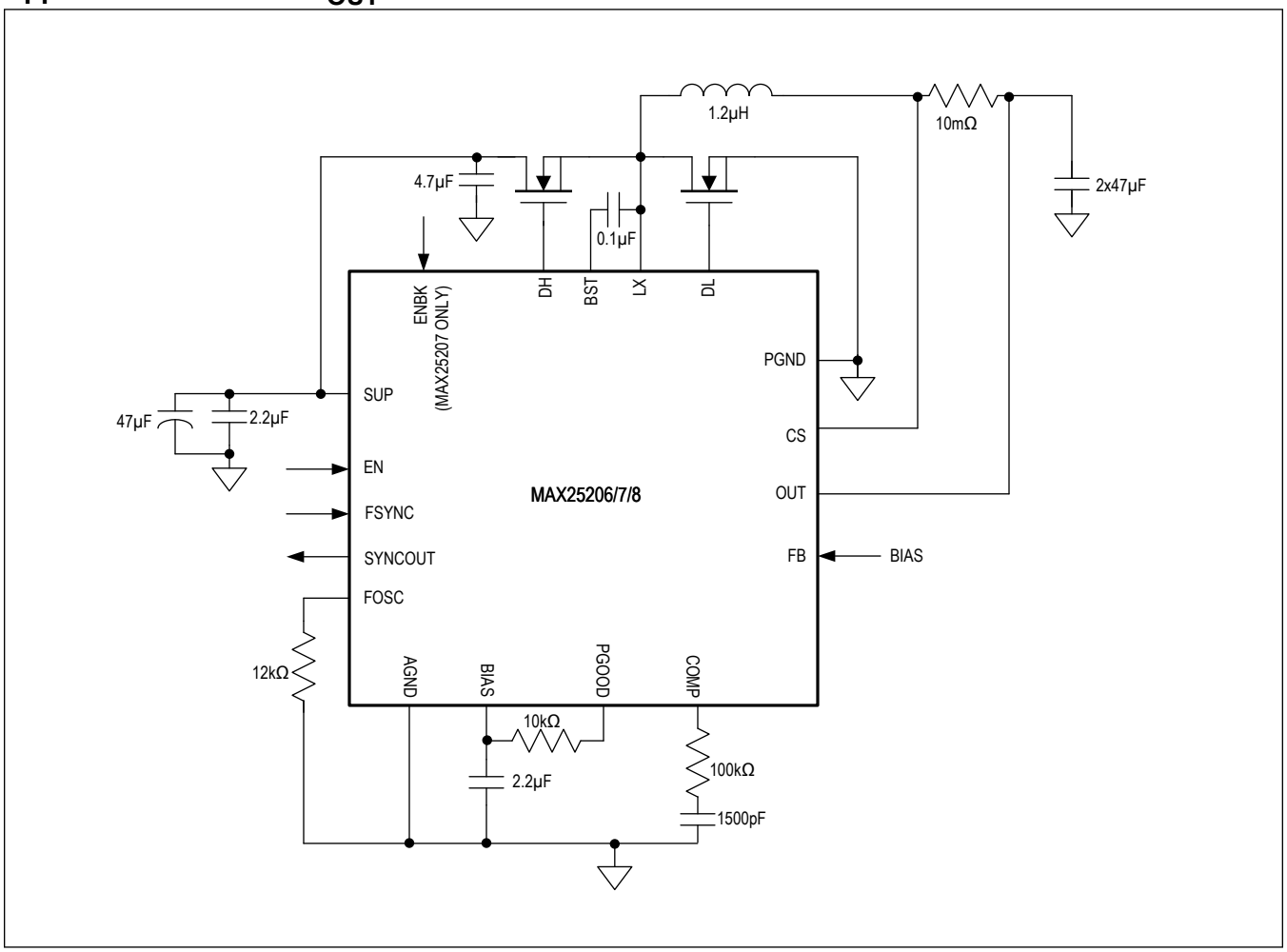


Figure 4. Layout Example

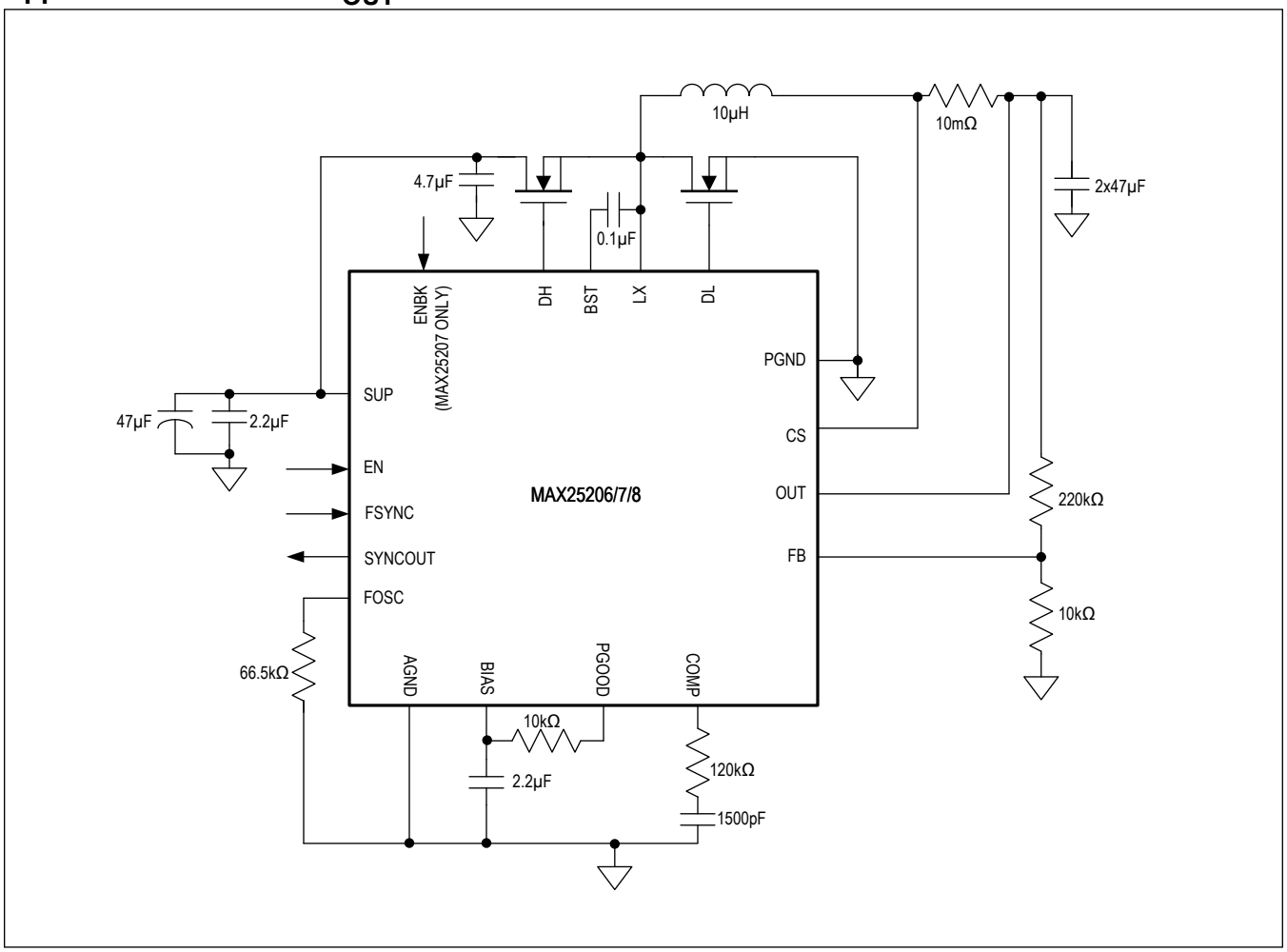
Typical Application Circuits

Application Circuit 1: $5V_{OUT}$ 2.2MHz 7A



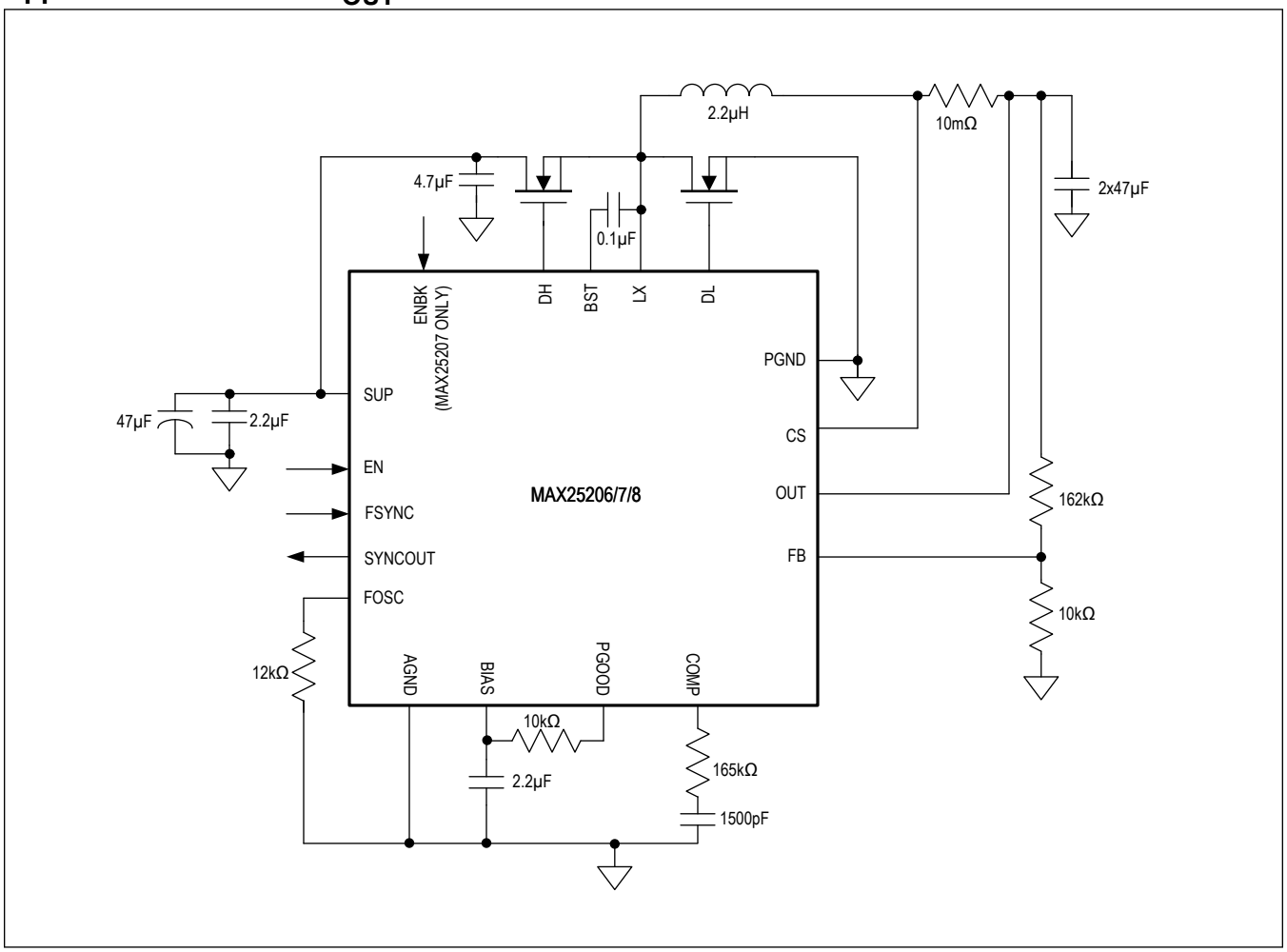
Typical Application Circuits (continued)

Application Circuit 2: 16V_{OUT} 440kHz 7A



Typical Application Circuits (continued)

Application Circuit 3: $12V_{OUT}$ 2.2MHz 7A



Ordering Information

PART	V_{OUT}		SWITCHOVER		BYPASS VOLTAGE
	ADJUSTABLE	FIXED	FPWM	SKIP	
MAX25206ATPA/VY+	0.7V TO 20V	5V	ON	ON	—
MAX25206ATPB/VY+	0.7V TO 20V	3.3V	ON	ON	—
MAX25206ATPC/VY+	0.7V TO 20V	3.3V	OFF	ON	—
MAX25207ATPA/VY+	0.7V TO 20V	5V	OFF	OFF	14V
MAX25207ATPB/VY+	0.7V TO 20V	5V	OFF	OFF	18V
MAX25208ATPA/VY+	0.7V TO 20V	5V	ON	ON	—

+ Denotes a lead(Pb)-free/RoHS-compliant package.

/V Denotes an automotive-qualified part.

Y Denotes wettable flank.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/20	Initial release	—
1	12/20	Updated *Voltage Monitoring (PGOOD)* , *Control Loop / Compensation*, and *Ordering Information*	19, 23-24, 29
2	1/22	Updated *Absolute Maximum Ratings*, *Electrical Characteristics*, *Detailed Description*, and *Ordering Information*	6, 7, 15, 27

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