

150A DC/DC μ Module Regulator with PMBus Interface

FEATURES

- **High Efficiency at High Frequency**
 - Up to 87.0% Efficiency at 1MHz, 54V_{IN} to 0.8V_{OUT}
- **PMBus-Compliant I²C Serial Interface**
 - Monitor Voltage, Current, Temperature and Faults
 - Internal EEPROM Fault Log Record
 - Digitally Programmable Control Loop
 - Program Voltage, Current Limits, Soft-Start/Soft-Stop, Frequency, Synchronization and Phasing, Power-Good, Warnings and Faults
- **Wide Input Voltage Range: 45V to 65V**
- **Output Voltage Range: 0.5V to 1.1V**
- **Optimized for 45V to 65V_{IN} to 0.8V_{OUT}**
- **±0.5% Maximum DC Output Error with Differential Remote Voltage Sense**
- **±3% Current Readback Accuracy**
- Parallel and Current Share Multiple μ Module[®] ICs
- 22mm × 24mm × 6.7mm Surface Mount Package

DESCRIPTION

The LTP[™]8800-1A is a 150A step-down μ Module regulator that provides microprocessor core voltage from 54V power distribution architecture. It features remote configurability and telemetry monitoring of power management parameters over PMBus—an open standard I²C-based digital interface protocol. The LTP8800-1A is comprised of a programmable digital control system with precision mixed-signal circuitry, EEPROM, power MOSFETs, planar transformer, inductors, and supporting components. Its high level of integration minimizes component count and design time and maximizes flexibility and power density. The LTP8800-1A preserves high efficiency at high conversion ratios by utilizing a resonant switching architecture that eliminates high voltage switching losses.

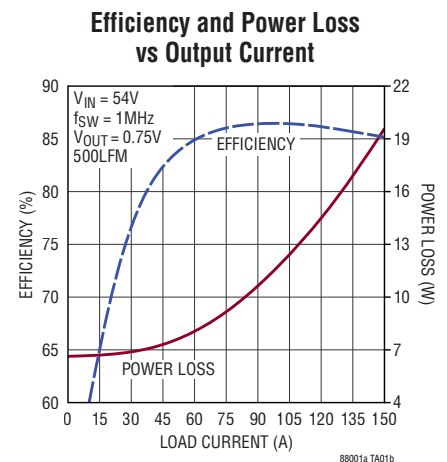
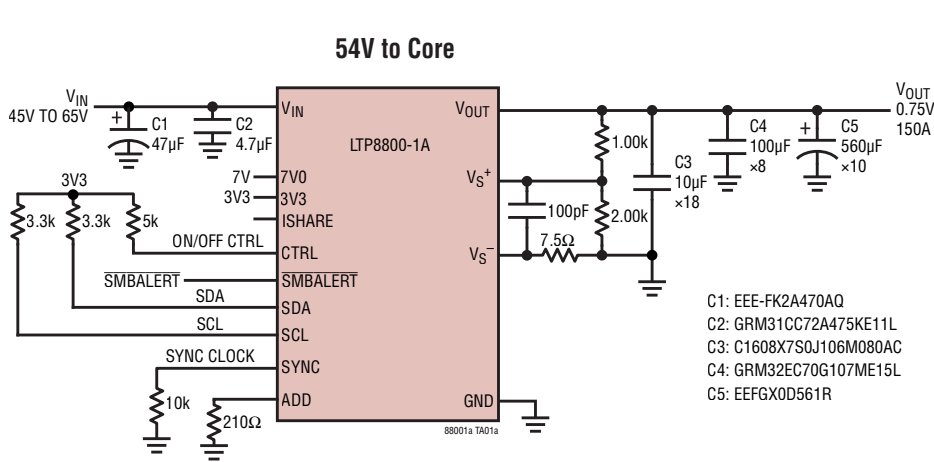
The LTP8800-1A is available in a 22mm × 24mm × 6.7mm surface-mounted open frame package.

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APPLICATIONS

- High Current Distributed Power Systems
- Servers, Network, and Storage Equipment
- Intelligent Energy Efficient Power Regulation

TYPICAL APPLICATION



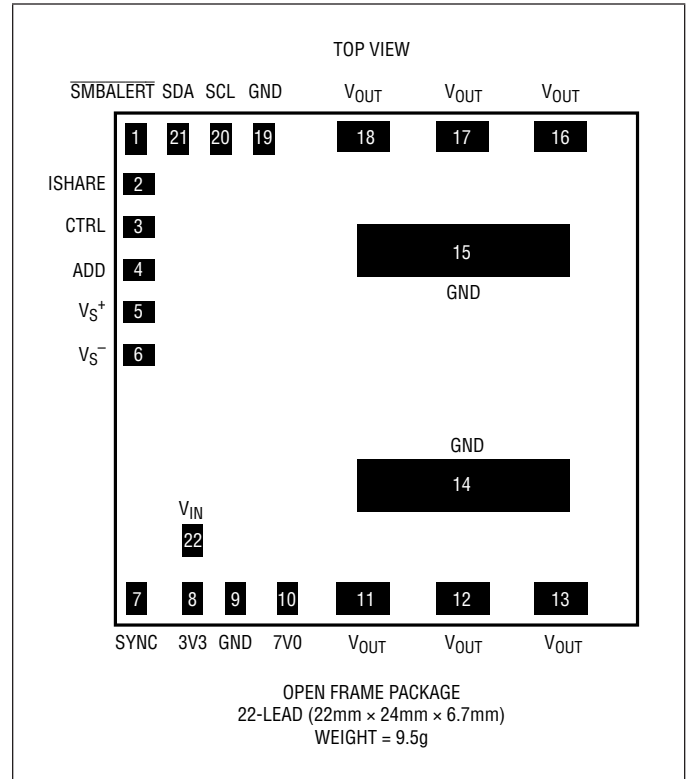
LTP8800-1A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

| | |
|--|----------------|
| V_{IN} | -0.3V to 70V |
| 7V0 | -0.3V to 7.75V |
| 3V3, SYNC, CTRL, $\overline{\text{SMBALERT}}$, SDA, SCL, ISHARE, ADD | -0.3V to 3.6V |
| V_{OUT} , V_{S^+} | -0.3V to 1.6V |
| V_{S^-} | -0.3V to 0.3V |
| Operating Junction Temperature Range | |
| LTP8800-1A (Note 2) | 0°C to 125°C |
| Storage Temperature Range (Note 2) | -40°C to 150°C |
| Peak Solder Reflow Body Temperature | 245°C |

PIN CONFIGURATION



ORDER INFORMATION

| PART NUMBER | PART MARKING | PACKAGE DESCRIPTION | MSL RATING | TEMPERATURE RANGE |
|-------------------|--------------|---------------------------------|------------|-------------------|
| LTP8800-1AIPV#PBF | LTP8800-1A | 22-Pin (22mm × 24mm) Open Frame | 3 | 0°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | |
|-----------------------------------|-----------------------|------------------|------|-----|-----|-------|---|
| V_{IN} Supply | | | | | | | |
| V_{IN} | Input Operating Range | | ● 45 | | 65 | V | |
| $V_{IN(UVLO)}$ | Input Undervoltage | V_{IN} Rising | | 38 | 40 | 42 | V |
| | | V_{IN} Falling | | 36 | 38 | 40 | V |
| $V_{IN(OVLO)}$ | Input Overvoltage | V_{IN} Rising | | 68 | 70 | 73 | V |
| | | V_{IN} Falling | | 65 | 68 | 71 | V |

Rev. D

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | |
|------------------------------|--|--|-----|-------|---------|-------|---------------|
| $I_{(VIN)}$ | Input Standby Current | CTRL = 0V | | 0.1 | | mA | |
| | Input Supply Current | $I_{OUT} = 0\text{A}$, $V_{IN} = 54\text{V}$, $V_{OUT} = 0.80\text{V}$ | | 55 | | mA | |
| | | $I_{OUT} = 10\text{A}$, $V_{IN} = 54\text{V}$, $V_{OUT} = 0.80\text{V}$ | | 0.22 | | A | |
| | | $I_{OUT} = 150\text{A}$, $V_{IN} = 54\text{V}$, $V_{OUT} = 0.80\text{V}$ | | 2.53 | | A | |
| 7V0 Supply | | | | | | | |
| 7V0 | 7V0 Operating Range | | ● | 6.5 | 7 | 7.5 | V |
| $7V0_{(UVLO)}$ | 7V0 Undervoltage | 7V0 Rising | ● | | | 4.5 | V |
| | | 7V0 Falling | ● | 3.5 | | | V |
| I_{7V0} | 7V0 Input Current | | ● | | 0.4 | 0.5 | A |
| 3V3 Supply | | | | | | | |
| 3V3 | 3V3 Operating Range | | ● | 3.0 | 3.3 | 3.6 | V |
| $3V3_{(UVLO)}$ | 3V3 Undervoltage | 3V3 Rising | ● | | | 3.0 | V |
| | | 3V3 Falling | ● | 2.75 | | | V |
| I_{3V3} | 3V3 Input Current | | ● | | 60 | 70 | mA |
| Output Specifications | | | | | | | |
| I_{OUT} | Output Current Range | | ● | 0 | | 150 | A |
| $I_{OUT(MAX)}$ | Output Current Limit | | | 200 | | | A |
| V_{OUT} | Regulated Output Voltage | $I_{OUT} = 0\text{A}$, $V_{IN} = 54\text{V}$, V_{OUT} Set to 0.800V, $T_J = 25^\circ\text{C}$ | | 0.796 | 0.800 | 0.804 | V |
| | | $I_{OUT} = 0\text{A}$, $V_{IN} = 54\text{V}$, V_{OUT} Set to 0.800V, $T_J = 0^\circ\text{C}$ to 125°C | ● | 0.788 | 0.800 | 0.812 | V |
| $V_{OUT(Load+Line)}$ | Line + Load Regulation | $I_{OUT} = 0\text{A}$ to 150A , $V_{IN} = 45\text{V}$ to 65V | ● | 0.792 | 0.800 | 0.808 | V |
| $V_{OUT(AC)}$ | $V_{OUT(P-P)}$ | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $C_{OUT} = 800\mu\text{F}$ MLCC, 5.6mF POSCAP | | | 4 | | mV |
| | $V_{OUT(RMS)}$ | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $C_{OUT} = 800\mu\text{F}$ MLCC, 5.6mF POSCAP | | | 1.6 | | mV |
| t_{START} | Start Time | CTRL High to $V_{OUT} = 0.8\text{V}$ | | | 10 | | ms |
| t_{STOP} | Stop Time | CTRL Low to Output Disable | | | 10 | | μs |
| $\Delta V_{OUT(LS)}$ | Maximum Output Voltage Excursion for Dynamic Load Step | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $I_{OUT} = 112.5\text{A}$ to 150A at $37.5\text{A}/\mu\text{s}$, $C_{OUT} = 800\mu\text{F}$ MLCC, 5.6mF POSCAP | | | 20 | | mV |
| t_{SETTLE} | V_{OUT} Settling Time to 1% | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $I_{OUT} = 112.5\text{A}$ to 150A at $37.5\text{A}/\mu\text{s}$, $C_{OUT} = 800\mu\text{F}$ MLCC, 5.6mF POSCAP | | | 25 | | μs |
| Efficiency | | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $I_{OUT} = 37.5\text{A}$ | | | 80.0 | | % |
| | | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $I_{OUT} = 75\text{A}$ | | | 86.5 | | % |
| | | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $I_{OUT} = 112.5\text{A}$ | | | 86.8 | | % |
| | | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $I_{OUT} = 150\text{A}$ | | | 85.6 | | % |
| Oscillator | | | | | | | |
| f_{SW} | Switching Frequency | Switching Frequency Set to 1.00 MHz | ● | 0.97 | 1.00 | 1.03 | MHz |
| f_{SYNC} | SYNC Range | | ● | 0.93 | 1.0 | 1.06 | MHz |
| PMBus Monitoring | | | | | | | |
| $I_{MON(OUT)}$ | Output Current Monitor | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $I_{OUT} = 150\text{A}$ | ● | | ± 3 | | % |
| $I_{MON(IN)}$ | Input Current Monitor | $V_{IN} = 54\text{V}$, $V_{OUT} = 0.8\text{V}$, $I_{OUT} = 150\text{A}$ | ● | | ± 5 | | % |

LTP8800-1A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------------------------------|---|-----|-----------|------|------------------|
| V_{OUTMON} | Output Voltage Monitor | $V_{\text{IN}} = 54\text{V}$, $V_{\text{OUT}} = 0.8\text{V}$, $I_{\text{OUT}} = 0\text{A}$, $T_J = 25^\circ\text{C}$ | | ± 0.5 | | % |
| | | $V_{\text{IN}} = 54\text{V}$, $V_{\text{OUT}} = 0.8\text{V}$, $I_{\text{OUT}} = 0\text{A}$, $T_J = 0^\circ\text{C to } 125^\circ\text{C}$ | ● | -1.5 | +1.5 | % |
| V_{INMON} | Input Voltage Monitor | $V_{\text{IN}} = 45\text{V to } 65\text{V}$, $V_{\text{OUT}} = 0.8\text{V}$, $I_{\text{OUT}} = 75\text{A}$ | ● | ± 2 | | % |
| T_{MON} | Temp Monitor | $V_{\text{IN}} = 54\text{V}$, $V_{\text{OUT}} = 0.8\text{V}$, $I_{\text{OUT}} = 75\text{A}$ | ● | ± 10 | | $^\circ\text{C}$ |
| Leakage Current Digital Inputs (CTRL, SDA, SCL, SYNC) | | | | | | |
| I_{DGL} | Input Leakage Current | $0\text{V} \leq V_{\text{PIN}} \leq 3.6\text{V}$ | ● | | 10 | μA |
| Control Section | | | | | | |
| $V_{\text{S-CM}}$ | V_{S} Common Mode Range | | ● | -100 | 100 | mV |
| V_{MRGN} | Output Voltage Margin Range | | | 0.5 | 1.10 | V |
| $V_{\text{OUT(OVLO)}}$ | Output Overvoltage Protection | | | 1.2 | | V |
| Digital Inputs (CTRL, SDA, SCL, SYNC) | | | | | | |
| V_{IH} | Input High Threshold Voltage | $V_{3\text{V}3} = 3.3\text{V}$ | ● | 2.1 | | V |
| V_{IL} | Input Low Threshold Voltage | $V_{3\text{V}3} = 3.3\text{V}$ | ● | | 0.8 | V |
| Digital Outputs (SDA, SMBALERT) | | | | | | |
| V_{OL} | Output Low Voltage | | ● | | 0.6 | V |
| PMBus Timing Characteristics (SDA, SCL) | | | | | | |
| f_{SCL} | Serial Bus Frequency | | ● | 10 | 400 | kHz |

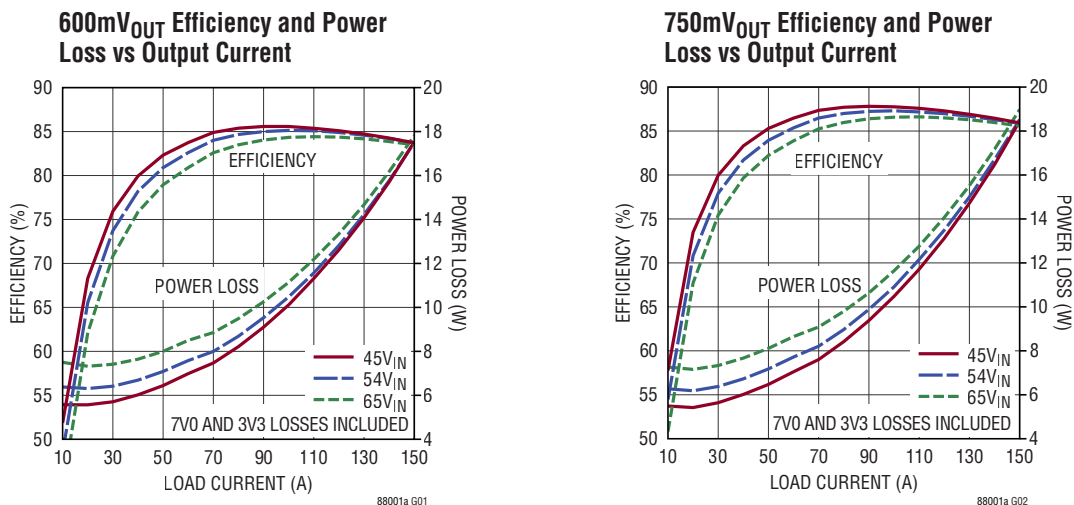
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTP8800-1AI is guaranteed over the full 0°C to 125°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C .

Note 3: The LTP8800-1AI includes overtemperature protection that is intended to protect the device during thermal overload conditions. Internal junction temperature may exceed 150°C if the overtemperature circuitry is active.

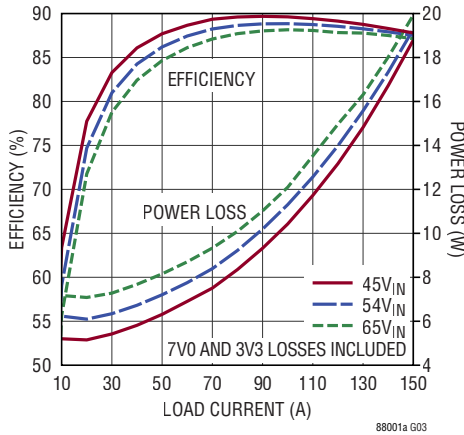
Note 4: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

900mV_{OUT} Efficiency and Power Loss vs Output Current



Load Transient Response 112.5A to 150A Load Step 37.5A/μs 45V_{IN} to 0.75V_{OUT}

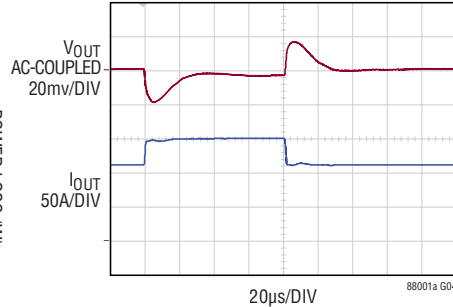


FIGURE 10 CIRCUIT
 $V_{IN} = 45V, V_{OUT} = 0.75V, f_{SW} = 1MHz$
 $C_{OUT} = 560\mu F \times 10 \text{ POSCAP} + 100\mu F \times 8 \text{ CERAMIC}$
 REG FE01h = 24, REG FE02h = 223, REG FE03h = 72, REG FE04h = 149

Load Transient Response 112.5A to 150A Load Step 37.5A/μs 54V_{IN} to 0.75V_{OUT}

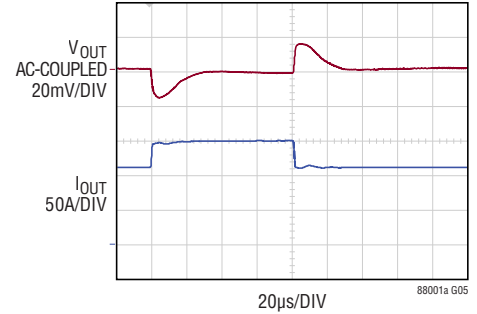


FIGURE 10 CIRCUIT
 $V_{IN} = 54V, V_{OUT} = 0.75V, f_{SW} = 1MHz$
 $C_{OUT} = 560\mu F \times 10 \text{ POSCAP} + 100\mu F \times 8 \text{ CERAMIC}$
 REG FE01h = 24, REG FE02h = 223, REG FE03h = 72, REG FE04h = 149

Load Transient Response 112.5A to 150A Load Step 37.5A/μs 65V_{IN} to 0.75V_{OUT}

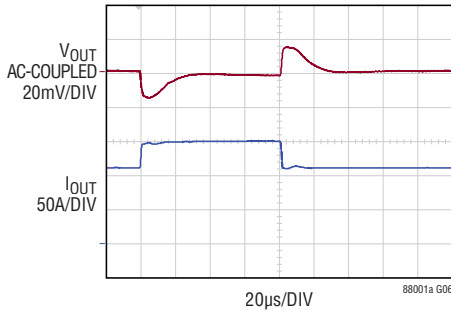


FIGURE 10 CIRCUIT
 $V_{IN} = 65V, V_{OUT} = 0.75V, f_{SW} = 1MHz$
 $C_{OUT} = 560\mu F \times 10 \text{ POSCAP} + 100\mu F \times 8 \text{ CERAMIC}$
 REG FE01h = 24, REG FE02h = 223, REG FE03h = 72, REG FE04h = 149

Full Load Start-Up and Shut-Down Triggered by CTRL

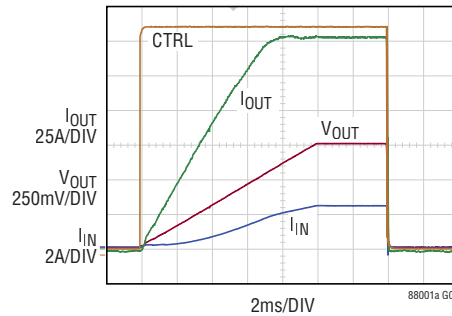


FIGURE 10 CIRCUIT

No Load Start-Up and Shut-Down Triggered by CTRL

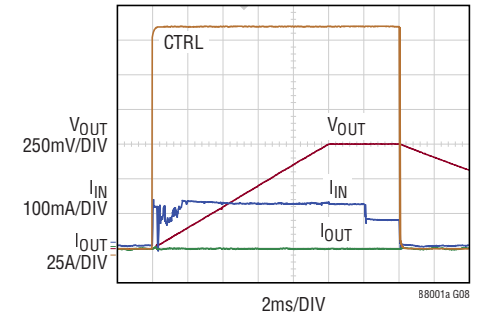


FIGURE 10 CIRCUIT

45V_{IN} No Load V_{OUT} Ripple

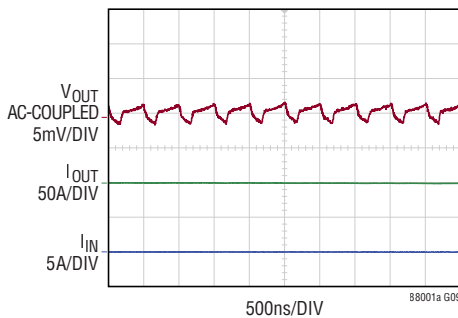


FIGURE 10 CIRCUIT
 $V_{IN} = 45V, V_{OUT} = 0.75V, f_{SW} = 1MHz$
 NO LOAD ON V_{OUT}

54V_{IN} No Load V_{OUT} Ripple

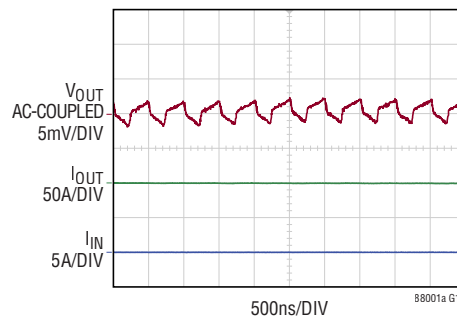


FIGURE 10 CIRCUIT
 $V_{IN} = 54V, V_{OUT} = 0.75V, f_{SW} = 1MHz$
 NO LOAD ON V_{OUT}

65V_{IN} No Load V_{OUT} Ripple

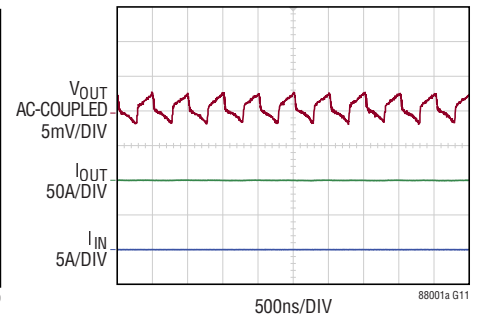


FIGURE 10 CIRCUIT
 $V_{IN} = 65V, V_{OUT} = 0.75V, f_{SW} = 1MHz$
 NO LOAD ON V_{OUT}

TYPICAL PERFORMANCE CHARACTERISTICS

45V_{IN} Full Load V_{OUT} Ripple

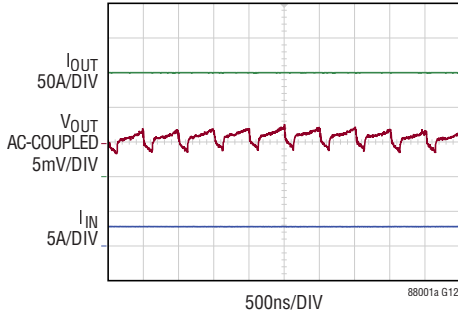


FIGURE 10 CIRCUIT
 $V_{IN} = 45V$, $V_{OUT} = 0.75V$, $f_{SW} = 1MHz$
 150A LOAD ON V_{OUT}

54V_{IN} Full Load V_{OUT} Ripple

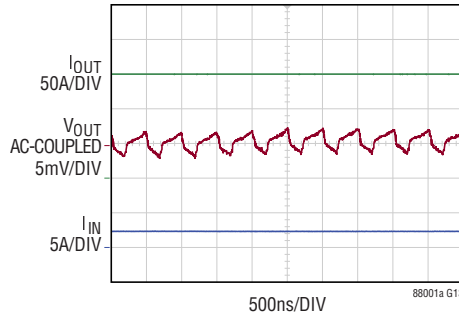


FIGURE 10 CIRCUIT
 $V_{IN} = 54V$, $V_{OUT} = 0.75V$, $f_{SW} = 1MHz$
 150A LOAD ON V_{OUT}

65V_{IN} Full Load V_{OUT} Ripple

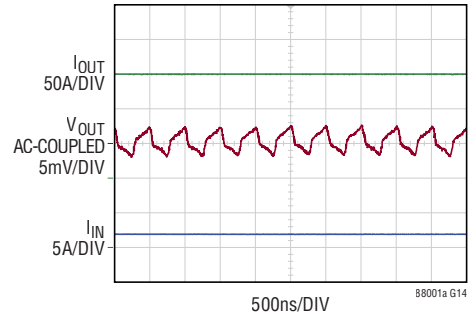
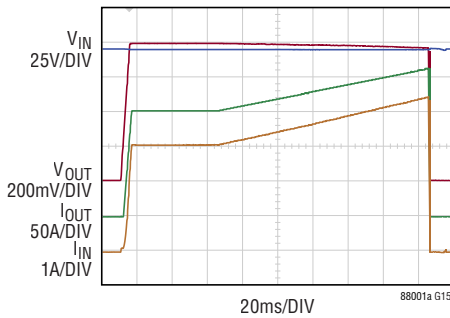
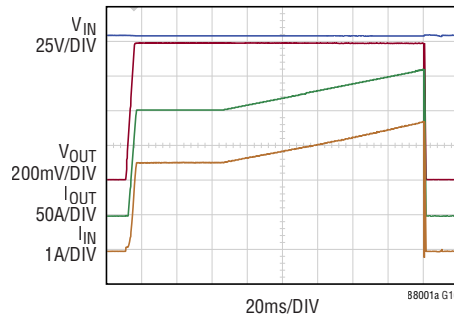


FIGURE 10 CIRCUIT
 $V_{IN} = 65V$, $V_{OUT} = 0.75V$, $f_{SW} = 1MHz$
 150A LOAD ON V_{OUT}

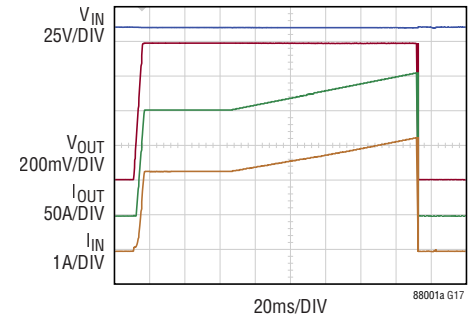
45V_{IN} OCP



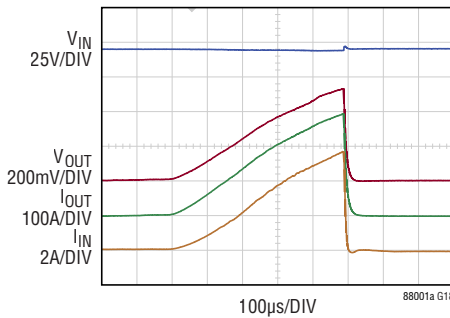
54V_{IN} OCP



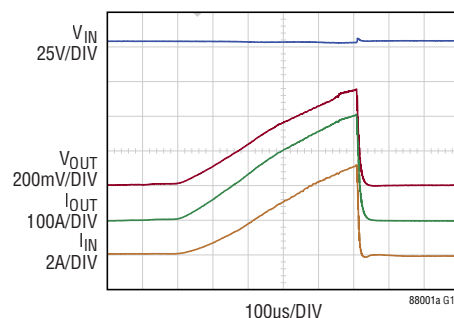
60V_{IN} OCP



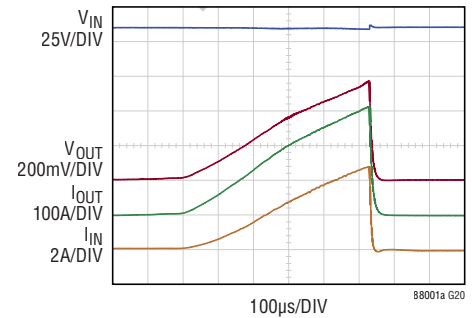
45V_{IN} Short-Circuit Start-Up



54V_{IN} Short-Circuit Start-Up



60V_{IN} Short-Circuit Start-Up



PIN FUNCTIONS

SMBALERT (Pin 1): Power-Good Output (Open-Drain). This pin is also used as the PMBus SMBALERT# signal. If unused, connect to GND.

ISHARE (Pin 2): Analog Current Sharing Input and Output. This pin must connect to other μ Module IC's ISHARE pins for current sharing. If not used, this pin should be left floating. Do not load ISHARE with external circuitry.

CTRL (Pin 3): Power Supply ON/OFF Input. This pin performs hardware on/off control. The factory default setting is to enable the LTP8800-1A only when CTRL is logic-high (active-high), but can optionally be changed to active-low, or ignored, using register 0x02.

If this pin is not used, connect to 3V3 if it is configured active-high, or GND if it is configured active-low or ignored.

ADD (Pin 4): I²C/PMBus Address Select Input. Connect a resistor from ADD to GND. See the Applications Information section for more information about the PMBus address selection.

V_S⁺ (Pin 5): Non-Inverting Voltage Sense Input. This pin functions as the Kelvin sense of V_{OUT} at the load, and as the feedback point for the converter control loop. The V_S⁺ pin should be tied to a precision feedback resistor divider connected to the output voltage. The V_S⁺ pin requires 100pF capacitance to the V_S⁻ pin placed close to the LTP8800-1A. The V_S⁺ feedback resistors need to have an equivalent parallel resistance < 2k. Otherwise, the control loop may be adversely affected.

V_S⁻ (Pin 6): Inverting Voltage Sense Input. This pin functions as the Kelvin sense of GND at the load, and as the GND connection for the feedback point for the converter control loop.

SYNC (Pin 7): Synchronization Input Signal. This pin is used as a reference for the internal oscillator and is referenced to GND. Synchronization is disabled by default.

To enable synchronization, set 0xFE55[6] = 0 and then set 0xFE00 = 0b0100000 for the value to take effect.

It is recommended that this input be disabled when not in use. To disable, set 0xFE55[6] = 1 and then set 0xFE00 = 0b0100000 for the value to take effect.

To accomplish phase interleaving of multiple devices, a phase delay in steps of 22.5 degrees can be added using register 0x37[3:0].

3V3 (Pin 8): The 3V3 pin powers internal μ Module circuitry. The typical 3V3 supply current when operating is 60mA. The voltage on this pin must be within the specified operating range before the LTP8800-1A can be enabled.

GND (Pins 9, 14, 15, 19): μ Module Ground. The GND pins carry high current and must be connected to large planes with sufficient internal layers. Be sure to keep the voltage at the pins roughly equal by taking care of the direction of current flow and debiasing of the ground planes.

7V0 (Pin 10): The 7V0 pin powers internal μ Module circuitry, including gate drivers. The typical 7V0 supply current when operating is 0.4A. The voltage on this pin must be within the specified operating range before the LTP8800-1A can be enabled.

V_{OUT} (Pins 11, 12, 13, 16, 17, 18): The V_{OUT} pins carry the high output current of the converter. As such, these pins must be connected to large power planes with sufficient internal layers. The PCB layout must be such that the two sets of V_{OUT} pins see roughly the same voltage. This ensures high efficiency and balanced currents. The output voltage is digitally programmable from 0.5V to 1.10V. The V_{OUT} pins are two rows of terminals and carry high steady-state output currents (from 0A up to 150A) and transient currents up to 200A.

SCL (Pin 20): I²C/PMBus Serial Clock Input and Output (Open-Drain).

SDA (Pin 21): I²C/PMBus Serial Data Input and Output (Open-Drain).

V_{IN} (Pin 22): The V_{IN} pin supplies current to the primary power switches and operates from 54V/48V nominal inputs; for further details, see Absolute Maximum Ratings and Electrical Characteristics table for input voltage range. The LTP8800-1A requires, at minimum, a total of 5 μ F from low ESR ceramic bypass capacitors, located as close as possible to the V_{IN} and GND pins. A single 4.7 μ F 1206/1210 X7* capacitor is recommended.

APPLICATIONS INFORMATION

COMPENSATION

The LTP8800-1A offers programmable loop compensation to optimize the transient response without any hardware change. A Type 3 filter architecture has been implemented. To tailor the loop response to the specific application, the low frequency gain, zero location, pole location and high frequency gain can all be set individually (see the Digital Filter Programming Registers section). From the sensed voltage to the duty cycle, the transfer function of the filter in z-domain is resolved by Equation 1.

$$H(z) = \left(\frac{D}{LFG} \cdot \frac{1}{(1-z^{-1})} + \frac{C}{HFG} \left(\frac{1 - \frac{B}{256}z^{-1}}{1 - \frac{A}{256}z^{-1}} \right) \right) \quad (1)$$

Where:

A = filter pole register value (in decimal), 0xFE03.

B = filter zero register value (in decimal), 0xFE02.

C = high frequency gain register value (in decimal), 0xFE04.

D = low frequency gain register value (in decimal), 0xFE01.

$LFG = 9.5488 \times 10^7 / f_{SW}$.

$HFG = 5.968 \times 10^6 / f_{SW}$.

As shown in Figure 1, adjusting low frequency gain register value will change the gain of the compensation over the low frequency range without moving the pole and zero locations. Adjusting high frequency gain register value will change the gain of the compensation over the high frequency range without moving the pole and zero locations. As shown in Figure 2, adjusting the pole and zero register values will move the double poles and double zeroes of the compensation. Increasing the filter zero and pole register values will separate the double zeroes and double poles. It is recommended that **LTpowerPlay**® be used to program the filter.

It is recommended that the user determines the appropriate value for the compensation registers using the **LTpowerCAD**® tool. An example of the bode plot of the typical application circuit with the recommended

compensation settings is shown in Figure 3. Measured bode plot of the LTP8800-1A in circuit Figure 10 with register setting (in decimal): 0xFE02 = 226, 0xFE03 = 160, 0xFE04 = 50, 0xFE01 = 8. (Crossover frequency: 28.84kHz, phase margin 64.5deg, gain margin 17.31dB).

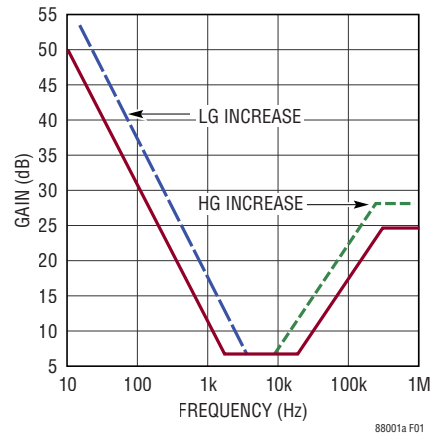


Figure 1. Compensation Gain Adjustment

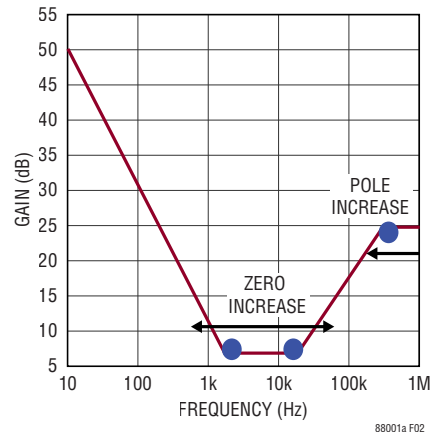


Figure 2. Compensation Poles and Zeroes Adjustment

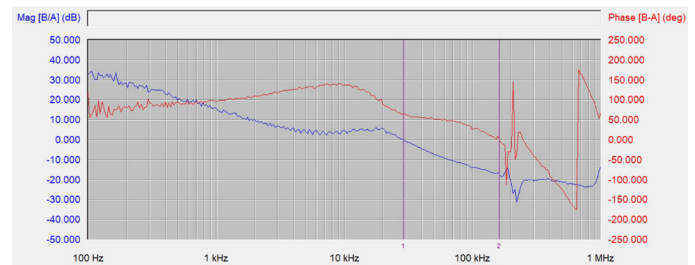


Figure 3. Measured Bode Plot of the LTP8800-1A

APPLICATIONS INFORMATION

PolyPhase CONFIGURATION

When configuring a PolyPhase[®] rail with multiple LTP8800-1A, the user must share the SYNC and ISHARE pins. An external clock source at the desired switching frequency is required for current sharing applications. The internal digital phase-locked loop is capable of determine the frequency on the SYNC pin and locking the internal switching frequency to the external frequency. The lock or capture range is $\pm 10\%$ of the switching frequency (Register 0x33). The relative phasing of all the channels should be spaced equally. This can be configured using Register 0x37. A phase shift in steps of 22.5 degree can be added.

PolyPhase LOAD SHARING

Multiple LTP8800-1A can be arrayed in order to provide a balanced load-share solution by bussing the ISHARE pins. Figure 4 illustrates a 2-phase design sharing connections required for load sharing.

PMBus COMMANDS AND LTPOWERPLAY

PMBus Commands

There are multiple PMBus commands and manufacturer specific commands, which can be customized to adjust the settings of LTP8800-1A μ Module, as listed in Table 1. These commands comply to the PMBus Power System Management Protocol. Users are encouraged to refer to the PMBus Communication and Command Processing section for details.

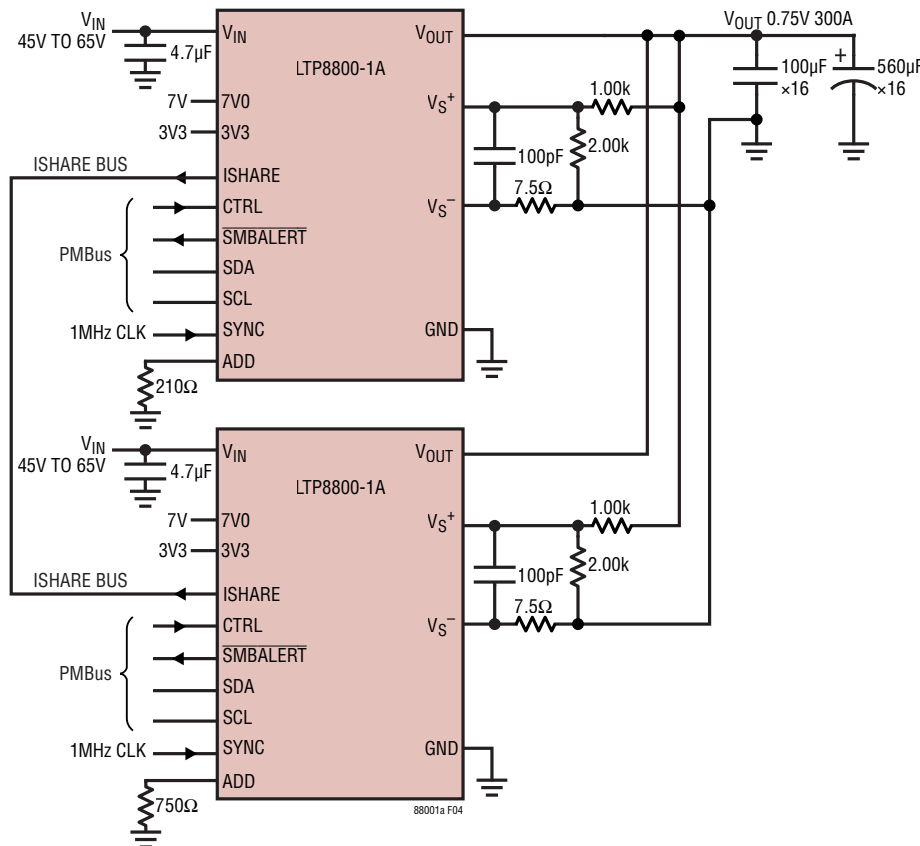


Figure 4. 2-Phase Operation Producing 0.75V at 300A

APPLICATIONS INFORMATION

Table 1. LTP8800-1A Summary of Customizable Commands and Features

| PMBus COMMAND NAME, OR FEATURE | CMD CODE REGISTER | COMMAND OR FEATURE DESCRIPTION | TYPE | DATA UNITS | DATA FORMAT | NVM ATTRIBUTES |
|--------------------------------|-------------------|---|----------|------------|-------------|------------------------------|
| WRITE_PROTECT | 0x10 | Protect the PMBus device against accidental writes. | R/W Byte | NA | Bit Field | Stored in user-editable NVM. |
| VIN_ON | 0x35 | Sets the value of the input voltage (V_{RMS}) at which the device starts power conversion. | R/W Word | Volts | Linear 11 | Stored in user-editable NVM. |
| VIN_OFF | 0x36 | Sets the value of the input voltage (V_{RMS}) at which the device stops power conversion. | R/W word | Volts | Linear 11 | Stored in user-editable NVM. |
| VIN_OV_FAULT_LIMIT | 0x55 | Sets the upper voltage threshold (in volts) measured at the sense/input pin that causes an overvoltage fault condition. | R/W Word | Volts | Linear 11 | Stored in user-editable NVM. |
| VIN_UV_FAULT_LIMIT | 0x59 | Sets the lower voltage threshold (in volts) measured at the sense/input pin that causes an undervoltage fault condition. | R/W Word | Volts | Linear 11 | Stored in user-editable NVM. |
| IIN_OC_FAULT_LIMIT | 0x5B | Sets the threshold value (in amperes) measured at the sense/input pin that causes an overcurrent fault condition. | R/W Word | Amps | Linear 11 | Stored in user-editable NVM. |
| POUT_OP_FAULT_LIMIT | 0x68 | Sets the upper power threshold (in watts) measured at the sense/output pin that causes an output overpower fault condition. | R/W Word | Watts | Linear 11 | Stored in user-editable NVM. |
| NM_DIGFILT_LF_GAIN_SETTING | 0xFE01 | Determines the low frequency gain of the loop response in normal mode. | R/W Byte | NA | NA | Stored in user-editable NVM. |
| NM_DIGFILT_ZERO_SETTING | 0xFE02 | Determines the position of the final zero in normal mode. | R/W Byte | NA | NA | Stored in user-editable NVM. |
| NM_DIGFILT_POLE_SETTING | 0xFE03 | Determines the position of the final pole in normal mode. | R/W Byte | NA | NA | Stored in user-editable NVM. |
| NM_DIGFILT_HF_GAIN_SETTING | 0xFE04 | Determines the high frequency gain of the loop response in normal mode. | R/W Byte | NA | NA | Stored in user-editable NVM. |

APPLICATIONS INFORMATION

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER μ Module ICs

LTpowerPlay is a powerful Graphical User Interface (GUI) that supports the digital power μ Module LTP8800-1A, as shown in Figure 5. In online mode, LTpowerPlay can be used to evaluate single or multiple LTP8800-1A power μ Module ICs of different types by connecting to a demo board or the user application. In offline mode with no hardware connected via PMBus, LTpowerPlay can also be used to build the project file with configuration of multiple μ Module ICs, and the project file can be saved

and reloaded later. Moreover, during board bring-up, LTpowerPlay can be used as a valuable diagnostic tool to program the power system, to tweak the system settings, or to diagnose system issues.

The LTpowerPlay utilizes Analog Device's USB-to-I²C/SMBus/PMBus Controller, [DC1613A](#), to communicate with circuit boards including the [DC3190A-A](#) (single LTP8800-1A module) demo board or a customer target system. Further context information, including tutorial demos, is available [here](#).

The screenshot shows the LTpowerPlay software interface. The main window is titled 'Config: U0 (7h40) -LTP8800_1'. The central pane displays a configuration table for the 'VOUT_COMMAND' register. The table includes the following entries:

| Register Name | Value | Description |
|----------------------|---------------------------|--|
| VOUT_COMMAND | 0.7500 V | Nominal DC/DC converter output voltage setpoint. |
| VOUT_MAX | 1.1000 V | |
| VOUT_MIN | 0.66 | |
| VOUT_TRANSITION_RATE | 0.100 V/ms | |
| VOUT_WARN_LIMIT | +46.7 % above/below VOUT | |
| VOUT_FAULT_LIMIT | +60.0 % above/below VOUT | |
| VOUT_WARN_LIMIT | -46.6 % above/below VOUT | |
| VOUT_FAULT_LIMIT | -71.2 % above/below VOUT | |
| POWER_GOOD_ON | -100.0 % above/below VOUT | |
| POWER_GOOD_OFF | -100.0 % above/below VOUT | |
| VIN_ON | 40.0000 V | |
| VIN_OFF | 38.0000 V | |
| VIN_WARN_LIMIT | 65.0000 V | |
| VIN_FAULT_LIMIT | 3.2500 V | |

The right-hand pane shows the 'Reg Info' for 'VOUT_COMMAND'. It includes a description, register information (Command Code: 0x21, Data Type: Unsigned Linear 16, Scope: Paged), and value analysis (GUI Value (hex): 0x3000, GUI Value (meaning): 0.75V). Below this, it provides example code for writing and reading the register, along with protocol diagrams for both write and read sequences.

Figure 5. LTpowerPlay Main Interface

APPLICATIONS INFORMATION

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTP8800-1A series communicate through PMBus with other compliant devices. The LTP8800-1A is always configured as a subordinate device in the overall system, requiring a two-wire interface with one data pin (SDA) and one clock pin (SCL). As subordinate devices, LTP8800-1A power μ Module ICs decode the command sent from the main device and respond accordingly. Data transfer of the PMBus subordinate is based on PMBus commands. According to the PMBus/SMBus/I²C communication protocol, all PMBus commands start with a subordinate address with the R/W bit cleared (set to 0), followed by the command code, with mostly the stop bit as the last bit in a complete data transfer.

Commands can be categorized as send, read, or write types. For read or write commands, data is transferred between devices in a byte wide format. For send commands, the subordinate device execute the commands upon receiving the stop bit. To ensure robust communication, the main and subordinate devices send acknowledge (ACK) or no acknowledge (NACK) bits as a method of handshaking, eliminating the busy errors between devices.

Manufacturer-specific extended commands are also supported by LTP8800-1A. These commands follow the same protocol as the standard PMBus commands. However, the command code consists of two bytes: Command code

extension (0xFE) and Extended command code (0x00 to 0xFF). By use of the manufacturer-specific extended commands, the PMBus command set is greatly extended.

PMBus ADDRESS SELECTION

The PMBus address is set by connecting an external resistor from the ADD pin to GND. Table 2 lists the recommended resistor values and associated PMBus addresses.

Table 2. Recommended Resistor Values and Associated PMBus Addresses

| PMBus ADDRESS | 1% RESISTOR ON ADD PIN (Ω) |
|---------------|-------------------------------------|
| 0x40 | 210 (or Connect to GND) |
| 0x41 | 750 |
| 0x42 | 1330 |
| 0x43 | 2050 |
| 0x44 | 2670 |
| 0x45 | 3570 |
| 0x46 | 4420 |
| 0x47 | 5360 |
| 0x48 | 6340 |
| 0x49 | 7320 |
| 0x4A | 8450 |
| 0x4B | 9530 |
| 0x4C | 10,700 |
| 0x4D | 12,100 |
| 0x4E | 13,700 |
| 0x4F | 15,000 (or Connect to 3V3) |

APPLICATIONS INFORMATION

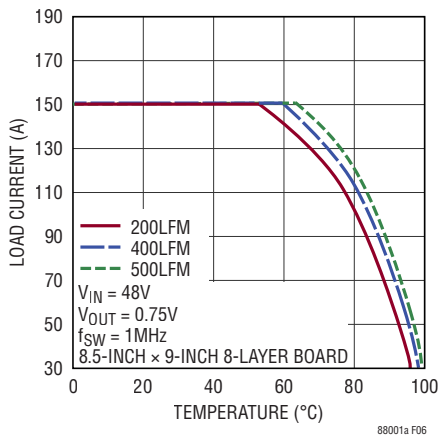


Figure 6. Thermal Derating
48V_{IN}, 0.75V_{OUT}

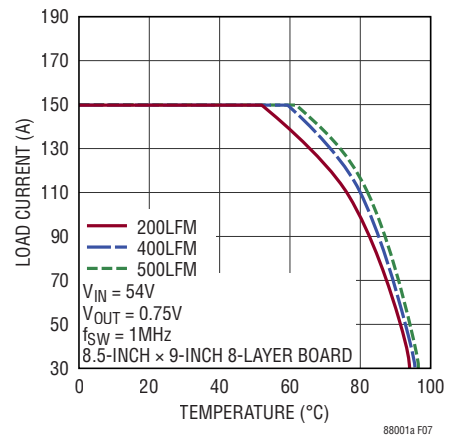
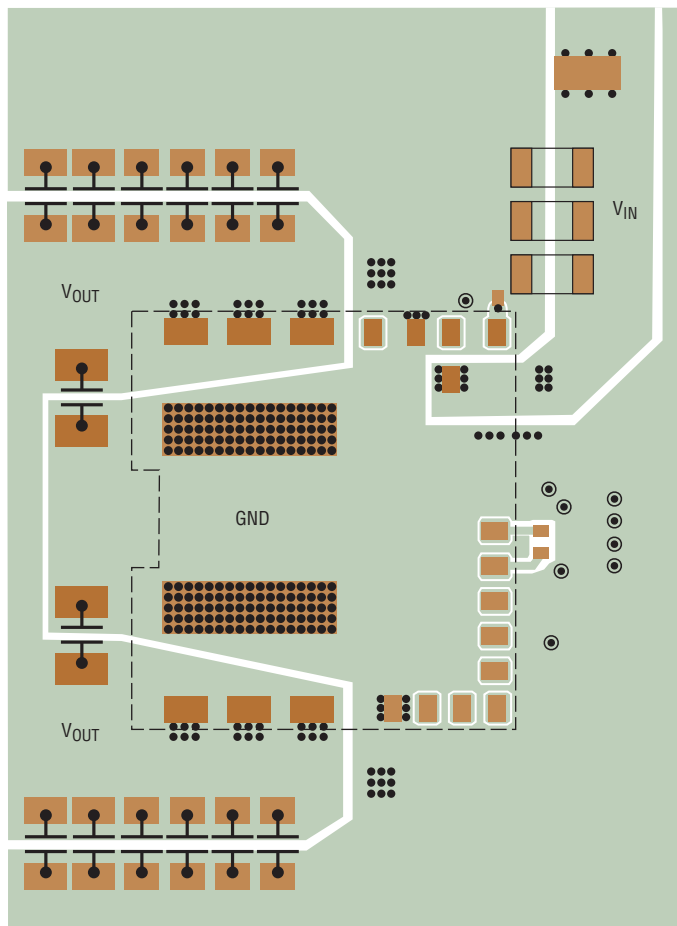
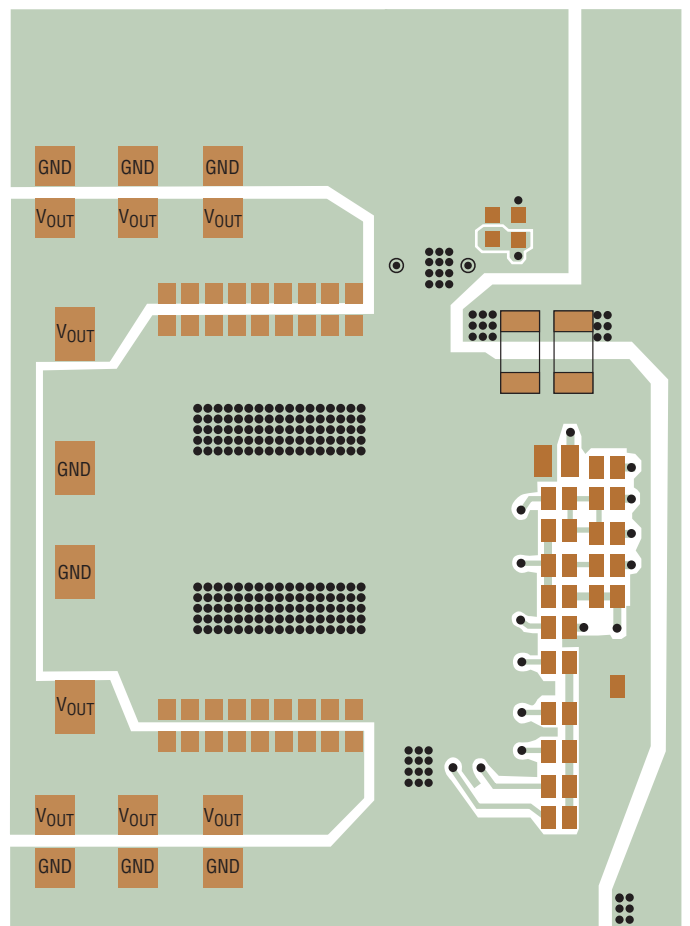


Figure 7. Thermal Derating
54V_{IN}, 0.75V_{OUT}



(a) Top Layers



(b) Bottom Layers

Figure 8. Recommended PCB Layout, Top View

TYPICAL APPLICATIONS

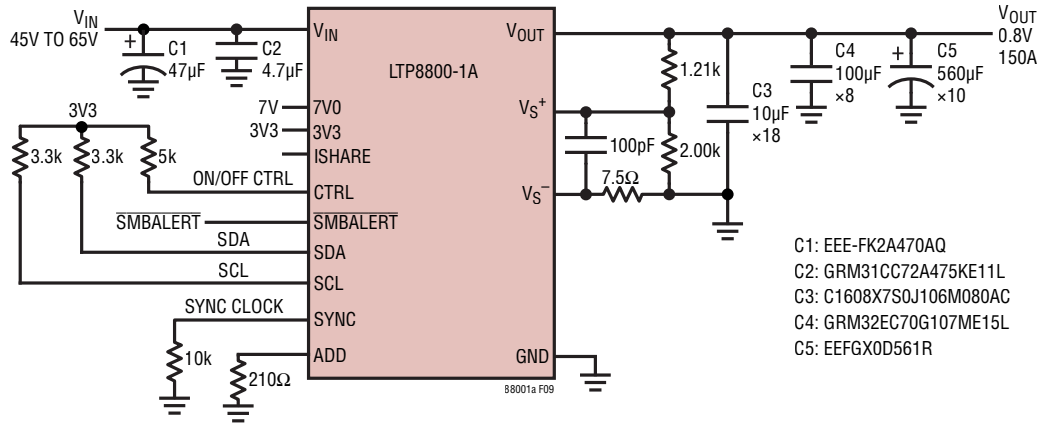


Figure 9. 0.8V 150A 1MHz Step-Down μModule with PMBus

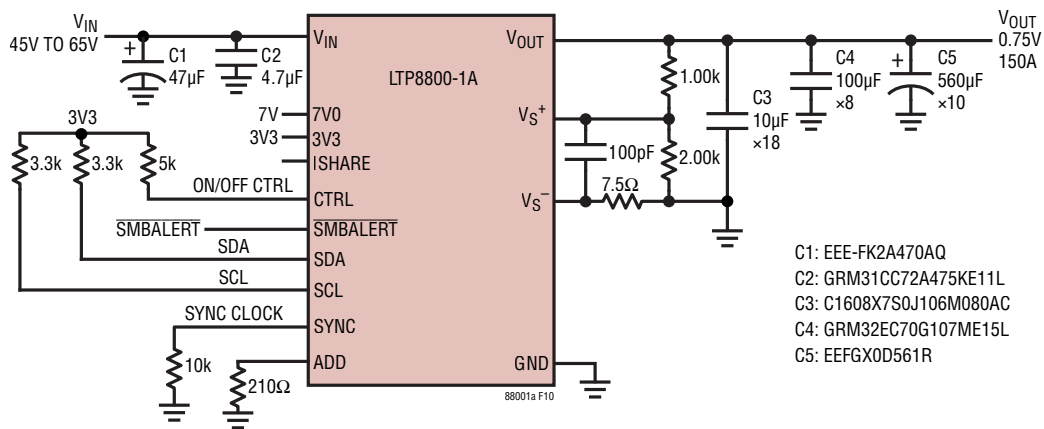


Figure 10. 0.75V 150A 1MHz Step-Down μModule with PMBus

TYPICAL APPLICATIONS

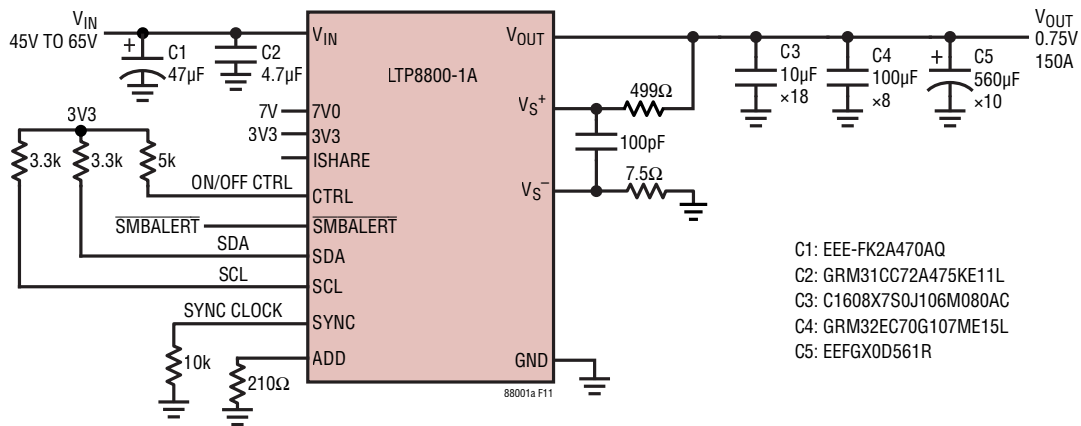


Figure 11. 0.75V 150A 1MHz Step-Down μ Module with Unity Gain for Faster Transient Response

Utilizing unity gain provides better DC accuracy and transient response. See Compensation Section for determining PID settings for optimal loop response.

LTP8800-1A requires the following registers to be adjusted for correct output voltage are listed in Table 3.

Table 3. Unity Gain Application PMBus Commands

| REGISTER OFFSETS | ADI FACTORY SETTINGS | UNITY GAIN APPLICATION SETTINGS |
|----------------------------|----------------------|---------------------------------|
| VOUT_COMMAND (0x21h) | 0x3000h | 0x3000h |
| VOUT_SCALE_LOOP (0x29h) | 0xB2A6h | 0xBA00h |
| VOUT_SCALE_MONITOR (0x2Ah) | 0xB2A6h | 0xBA00h |

TYPICAL APPLICATIONS

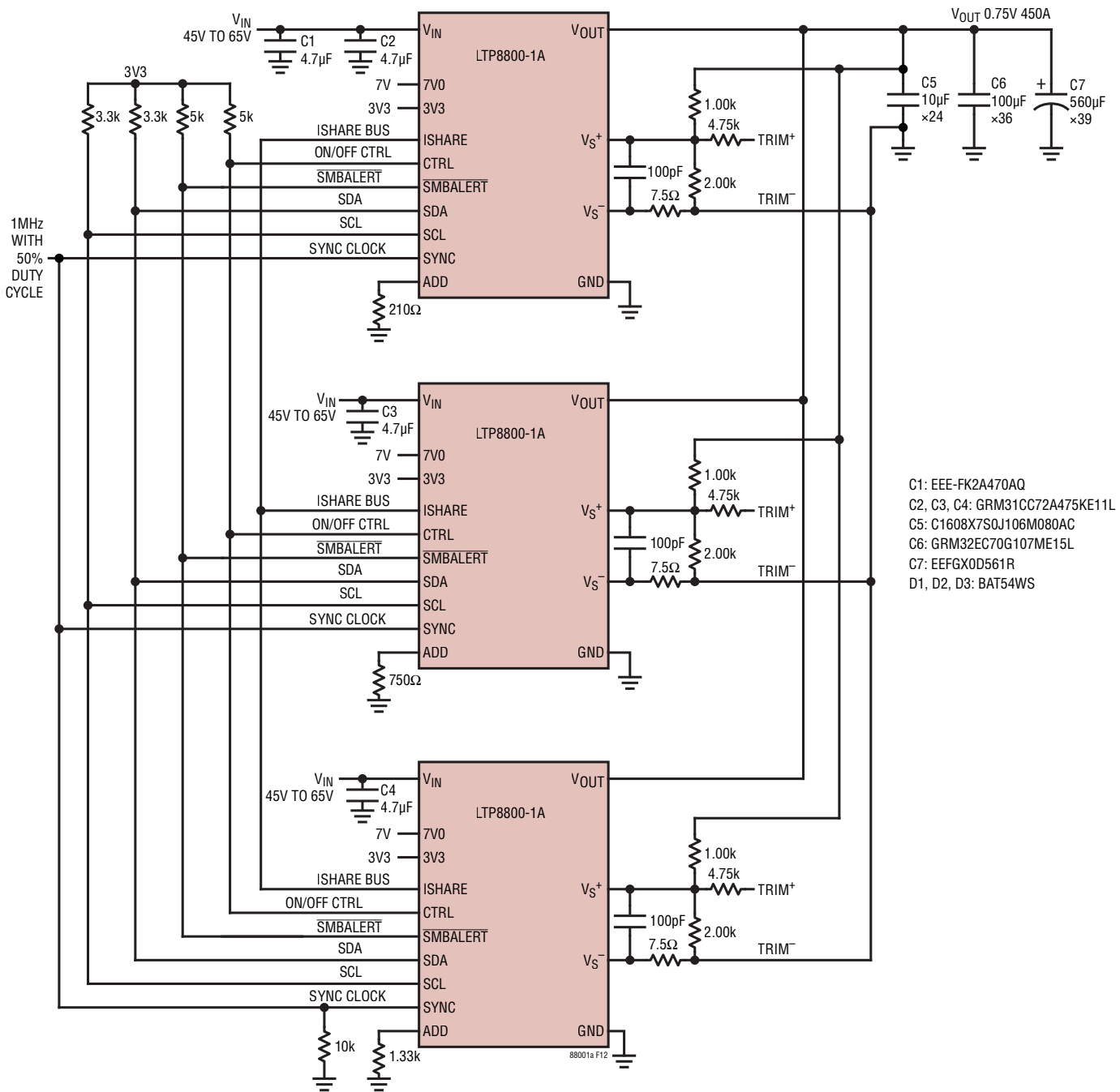
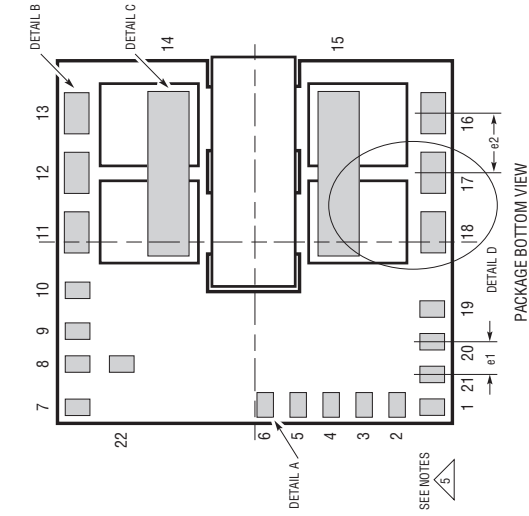


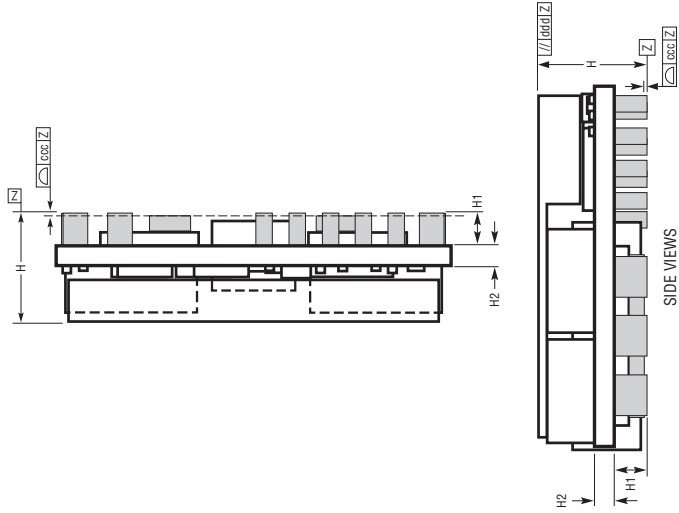
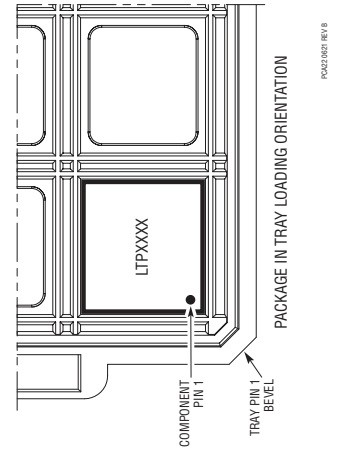
Figure 12. 3-Phase Operation Producing 0.75V at 450A with Power System Management Features

PACKAGE DESCRIPTION

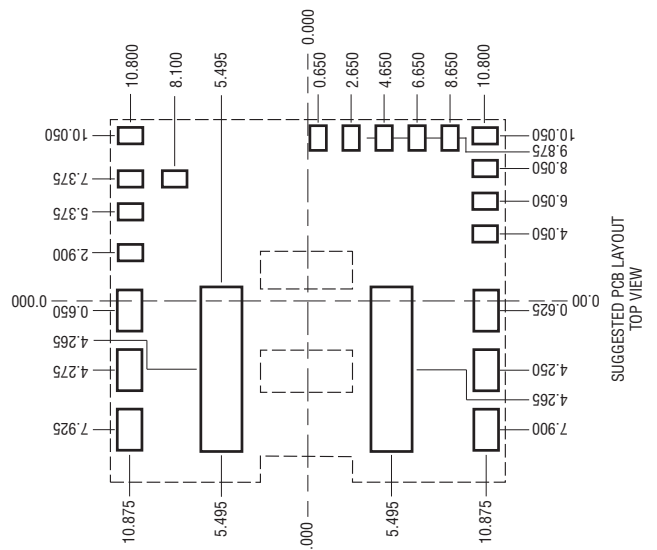
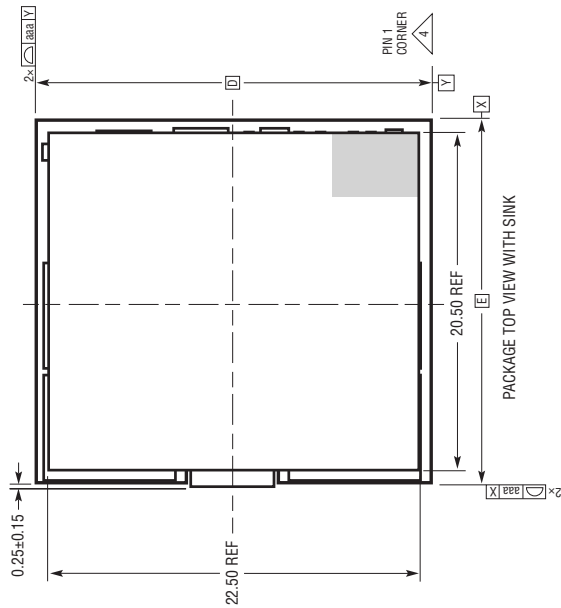
PCA Package
22-Lead (22mm × 24mm × 6.70mm)
 (Reference LTC DWG #05-08-7006 Rev B)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. ALL DIMENSIONS ARE IN MILLIMETERS
 3. PRIMARY DATUM - Z - IS SEATING PLANE
 4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
 5. PACKAGE PIN LABELING MAY VARY AMONG PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

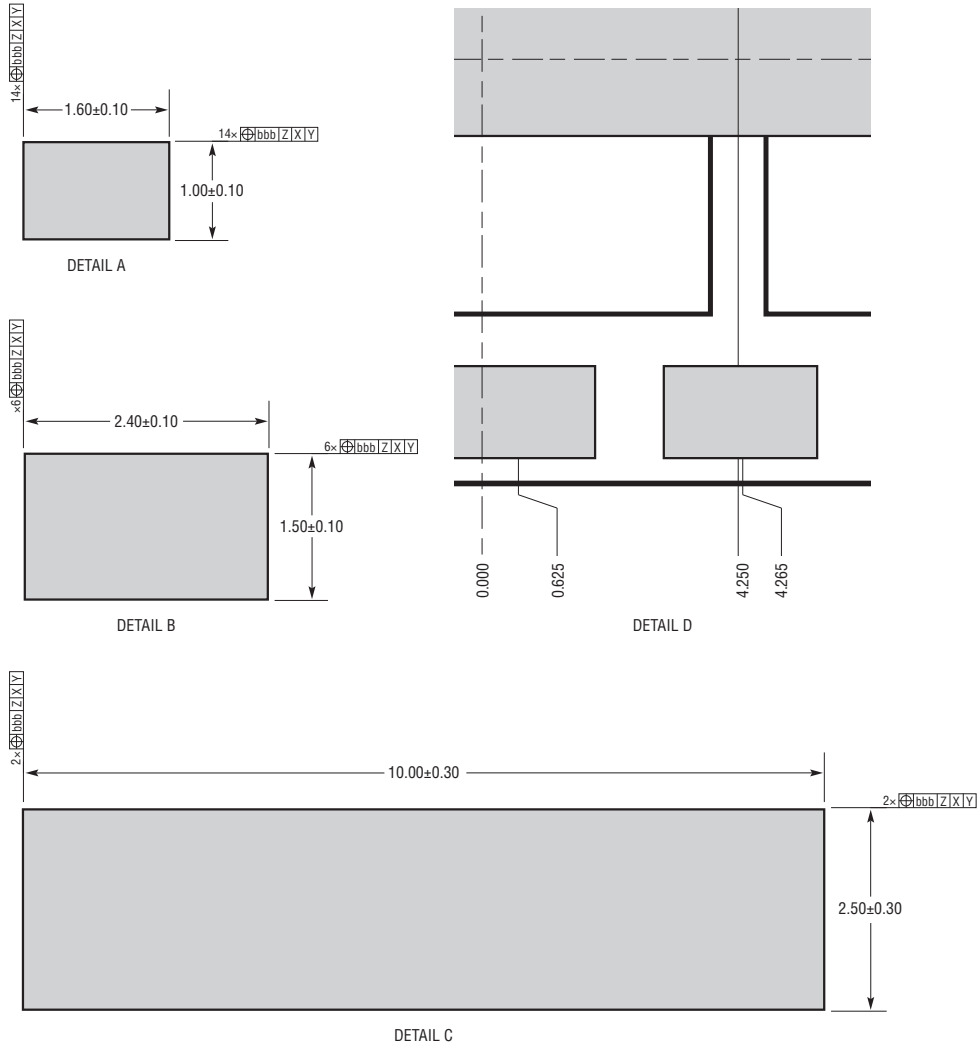


| SYMBOL | DIMENSIONS | | NOTES |
|-----------------------------------|------------|------|---------|
| | MIN | MAX | |
| D | 24.00 | | |
| E | 22.00 | | |
| H | 6.35 | 6.70 | 7.05 |
| H1 | 1.70 | 1.90 | 2.10 |
| H2 | 1.05 | 1.20 | 1.35 |
| e1 | 2.00 | | PCB THK |
| e2 | 3.65 | | |
| aaa | | | 0.20 |
| bbb | | | 0.40 |
| ccc | | | 0.20 |
| ddd | | | 0.35 |
| TOTAL NUMBER OF INTERCONNECTS: 22 | | | |



PACKAGE DESCRIPTION

PCA Package
22-Lead (22mm × 24mm × 6.70mm)
 (Reference LTC DWG #05-08-7006 Rev B)



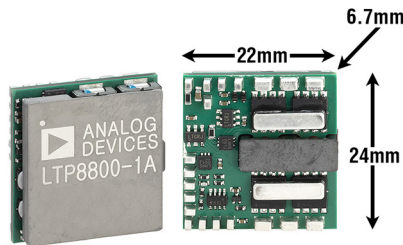
PCA22 0021 REV B

REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|-------|--|-------------|
| SpA | 10/22 | Changed Module to μ Module. | All |
| | | Removed Tape and Reel criteria. | 2 |
| | | Corrected LFG and HFG values for Equation 1. | 8 |
| | | Updated Figure 8 (Recommended PCB Layout drawing). | 13 |
| B | 6/23 | Release to open market | — |
| C | 5/24 | Updated SMBALERT (Pin 1) in Pin Functions. | 7 |
| D | 11/24 | Updated Pin Functions. | 7 |
| | | Updated Ltpowerplay: An Interactive GUI For Digitalpower μ module ICs. | 11 |
| | | Updated Pmbus Communication and Command Processing. | 12 |
| | | Updated Figure 12. | 16 |

LTP8800-1A

PACKAGE PHOTOS Part marking is either ink mark or laser mark



DESIGN RESOURCES

| SUBJECT | DESCRIPTION |
|--|---|
| µModule Design and Manufacturing Resources | <p>Design:</p> <ul style="list-style-type: none"> • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools <p>Manufacturing:</p> <ul style="list-style-type: none"> • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability |
| µModule Regulator Products Search | <ol style="list-style-type: none"> 1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. |
| Digital Power System Management | Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging. |

RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|-------------------------------------|--|---|
| LTP8800-4A | 54V _{IN} , 200A µModule Regulator with Digital Power System Management, Optimized 0.8V _{OUT} | 45V ≤ V _{IN} ≤ 65V, 0.5V ≤ V _{OUT} ≤ 1.1V, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 22mm × 24mm × 22mm Surface-Mount Package |
| LTP8802A-1A | 54V _{IN} , 140A µModule Regulator with Digital Power System Management, Optimized 3.3V _{OUT} | 45V ≤ V _{IN} ≤ 65V, 0.5V ≤ V _{OUT} ≤ 3.6V, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 22mm × 24mm × 22mm Surface-Mount Package |
| LTP8803-1A | 54V _{IN} , 140A µModule Regulator with Digital Power System Management, Optimized 1.2V _{OUT} | 45V ≤ V _{IN} ≤ 65V, 0.5V ≤ V _{OUT} ≤ 1.5V, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 22mm × 24mm × 22mm Surface-Mount Package |
| LTM[®]4664 | 54V _{IN} , Dual 25A or Single 50A µModule Regulator with Digital Power System Management | 30V ≤ V _{IN} ≤ 58V, 0.5V ≤ V _{OUT} ≤ 1.5V, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 16mm × 16mm × 7.72mm BGA Package |
| LTM4664A | 54V _{IN} , Dual 30A or Single 60A µModule Regulator with Digital Power System Management | 30V ≤ V _{IN} ≤ 58V, 0.5V ≤ V _{OUT} ≤ 1.2V, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error. 16mm × 16mm × 7.72mm BGA Package. |
| LTM4700 | Dual 50A or Single 100A µModule Regulator with Digital Power System Management | 4.5V ≤ V _{IN} ≤ 16V, 0.5V ≤ V _{OUT} ≤ 1.8V, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 15mm × 22mm × 7.87mm BGA Package |
| LTM4681 | Quad 31.25A or Single 125A µModule Regulator with Digital Power System Management | 4.5V ≤ V _{IN} ≤ 16V, 0.5V ≤ V _{OUT} ≤ 3.3V, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error. 15mm × 22mm × 8.17mm BGA Package. |
| LTM4660 | 60V, 300W Non-Isolated µModule Bus Converter | 30V ≤ V _{IN} ≤ 60V, 7.5V ≤ V _{OUT} ≤ 18V, Up to 300W, 16mm × 16mm × 10.34 BGA Package |

Mouser Electronics

Authorized Distributor

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[LTP8800-1AIPV#PBF](#) [DC3190A-A](#)