

Description

RClamp2272ZC is specifically designed to protect sensitive electronics from damage or latch-up due to ESD. This device offers desirable characteristics for board level protection including fast response time, clamping voltage, and no device degradation.

RClamp2272ZC is in a DFN 0.62 x 0.32 x 0.25mm 3-Lead package. Each device will protect two lines operating at 22 volts. The small package gives the designer the flexibility to protect dual lines in space constraint applications. The combination of small size and high ESD surge capability makes them ideal for use in portable applications.

Applications

- RF Antenna
- FM Antenna
- Near Field Communication (NFC) lines
- IoT Devices
- USB Type-C

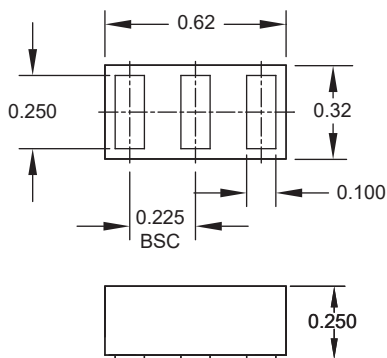
Features

- High ESD withstand Voltage
 - IEC 61000-4-2 (ESD): $\pm 10\text{kV}$ (Contact), $\pm 15\text{kV}$ (Air)
 - IEC 61000-4-5 (Lightning): 4A (8/20 μs)
- Ultra-small package
- Protects dual data lines
- Working voltage: $\pm 22\text{V}$
- Low ESD clamping voltage
- Low capacitance: 0.14pF typical
- Low leakage current
- Low dynamic resistance: 0.34 Ω typical
- Solid-State Silicon-Avalanche Technology

Mechanical Characteristics

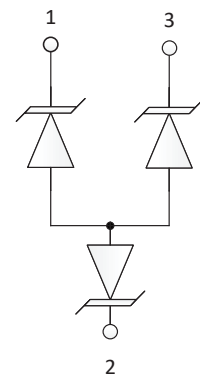
- Package: DFN 0.62 x 0.32 x 0.25mm 3-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Pb-Free
- Marking: Marking Code
- Packaging: Tape and Reel

Package Dimension



Nominal Dimensions in mm

Functional Schematic & Pin Configuration



Device Schematic

Absolute Maximum Rating

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PK}	26	W
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	4	A
ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V_{ESD}	± 10	kV
ESD per IEC 61000-4-2 (Air) ⁽¹⁾		± 15	
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

T=25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage	V_{RWM}				22	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	24	28	32	V
Trigger Voltage ⁽²⁾	I_{Trig}	$t_p = 0.2/100ns$ (TLP)	30			V
Reverse Leakage Current	I_R	$V_{RWM} = 22V$		<1	50	nA
Clamping Voltage ⁽³⁾	V_C	$t_p = 1.2/50\mu s$ (Voltage), 8/20 μs (Current) Combination Waveform, $R_S = 12\Omega$		$I_{PP} = 4A$ 6.4		V
ESD Clamping Voltage ⁽⁴⁾	V_C	$t_p = 0.2/100ns$ (TLP)		$I_{TLP} = 4A$ 6.8 $I_{TLP} = 16A$ 11.0	20	V
Dynamic Resistance ^{(4),(5)}	R_{DYN}	$t_p = 0.2/100ns$ (TLP)		0.34		Ω
Junction Capacitance	C_J	$V_R = 0V$, $f = 1MHz$		0.14	0.2	pF

Notes:

(1): ESD Gun return path to Ground Reference Plane (GRP).

(2): Guaranteed by design, not production tested.

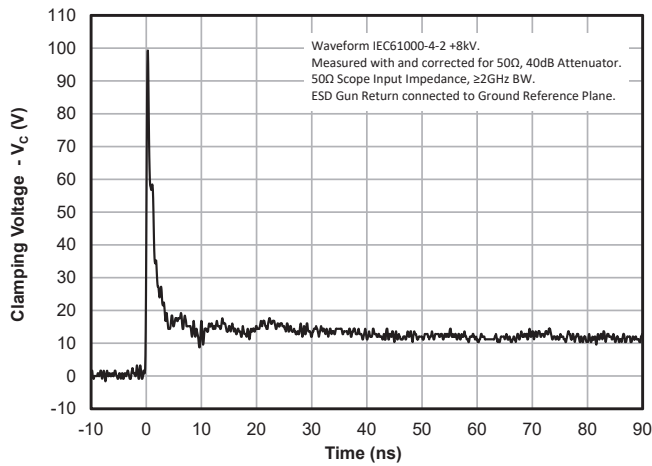
(3): Measured using a 1.2/50 μs (voltage), 8/20 μs (current) combination waveform, $R_S = 12\Omega$. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

(4): Transmission Line Pulse Test (TLP) Settings: $t_p = 100ns$, $t_r = 0.2ns$, I_{TLP} and V_{TLP} averaging window: $t_1 = 70ns$ to $t_2 = 90ns$.

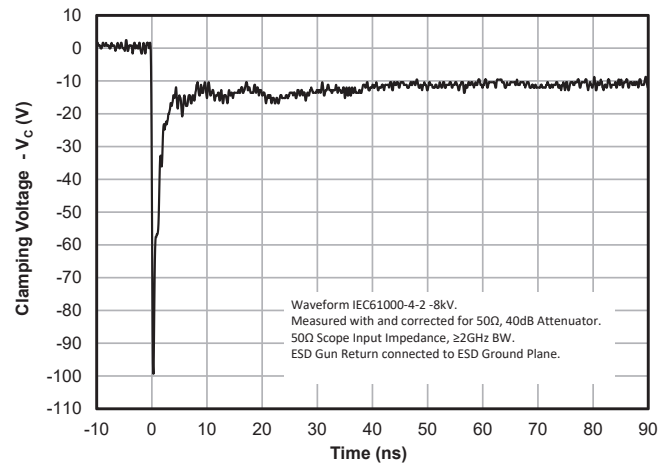
(5): Dynamic resistance calculated from $I_{TLP} = 4A$ to $I_{TLP} = 16A$.

Typical Characteristics

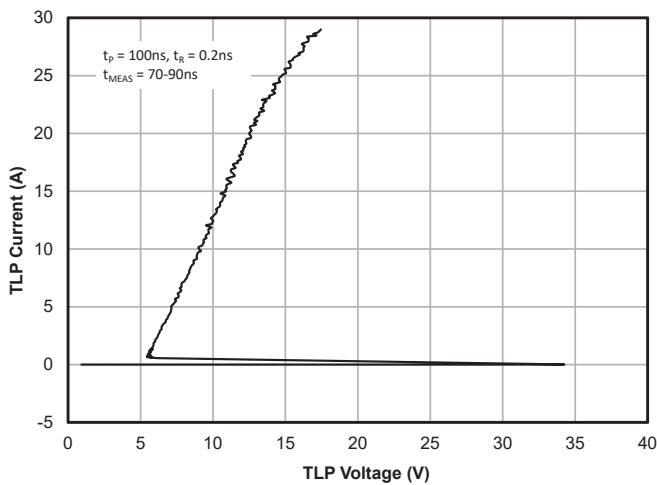
ESD Clamping (+8kV Contact per IEC 61000-4-2)



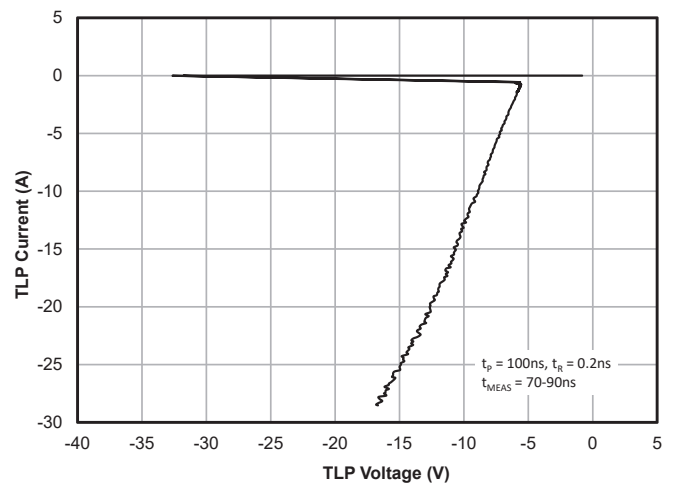
ESD Clamping (-8kV Contact per IEC 61000-4-2)



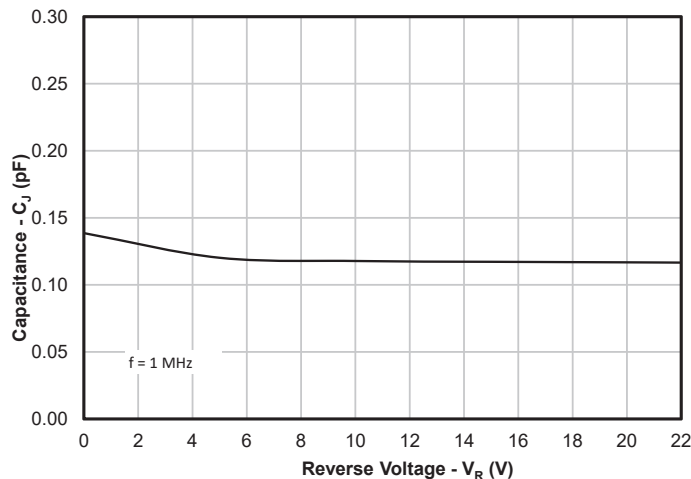
TLP Characteristics (Positive Pulse)



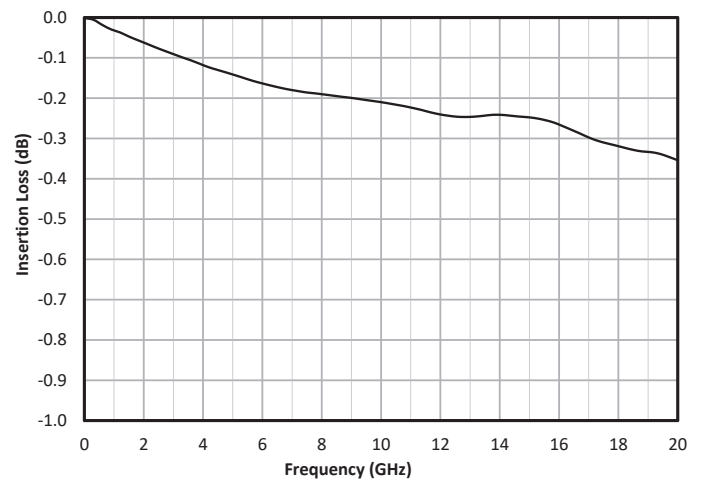
TLP Characteristics (Negative Pulse)



Capacitance vs. Reverse Voltage



Insertion Loss - S21



Applications Information

Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

L = Aperture Length

W = Aperture Width

T = Stencil Thickness

The outer pads are designed to have an area ratio of 0.71. The minimum recommended area ratio is 0.66 to achieve good solder paste transfer. In addition to increasing the area ratio, the increased width of the pads aid in self-centering the package during reflow soldering. During reflow, the solder will tend to "pull" the package outward on each side, thus aiding in centering the device. Some device "tilt" may be observed and is normal. Tilting will not affect the electrical performance. Pad length may be slightly reduced in order to minimize device tilt, however this will also reduce the area ratio as described above.

The center pad opening is minimized in order to reduce the chance of solder bridging. While the area ratio is slightly less than optimal, increasing the pad size would reduce the gap between the pads thus increasing the chance of solder bridging. Note however that the package is fully encapsulated and is not conductive to any of the pins.

Semtech recommends the stencil have a rectangular aperture with rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended.

Recommended Mounting Pattern

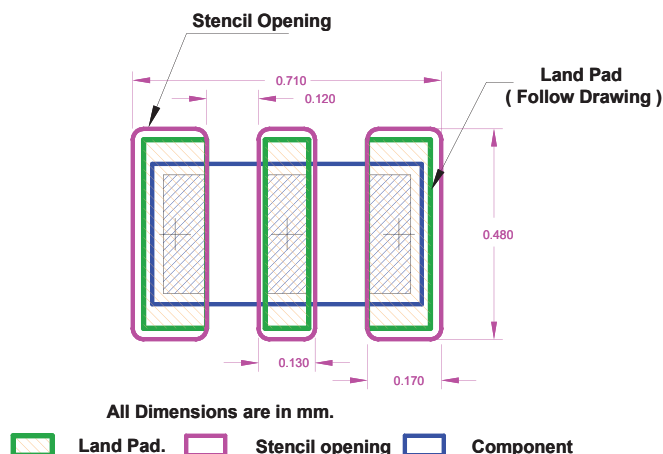
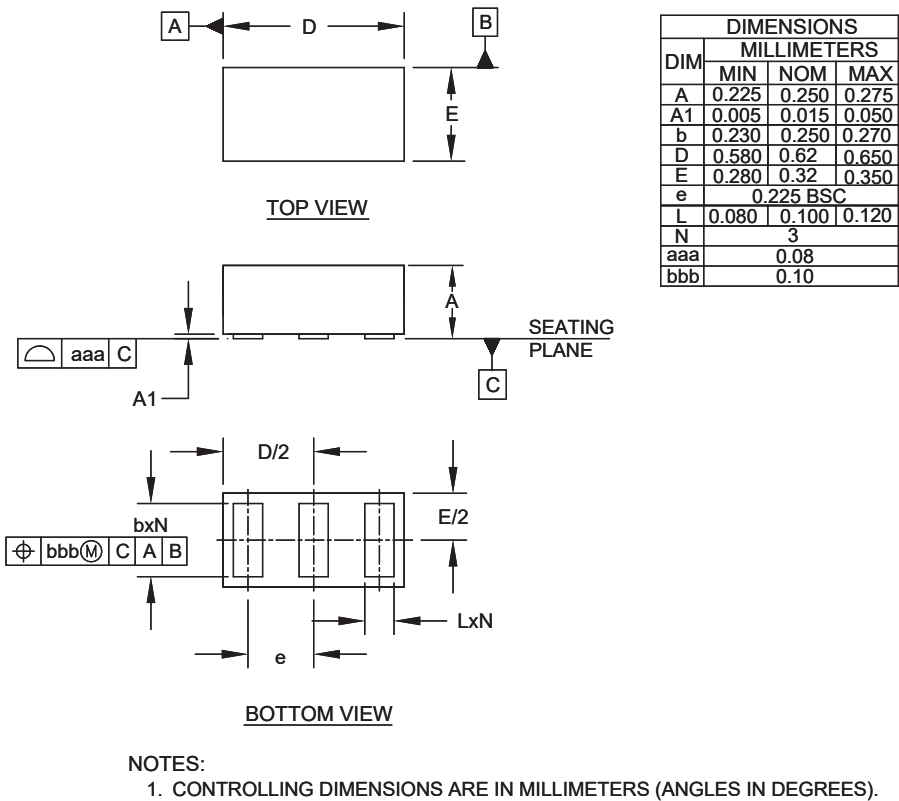


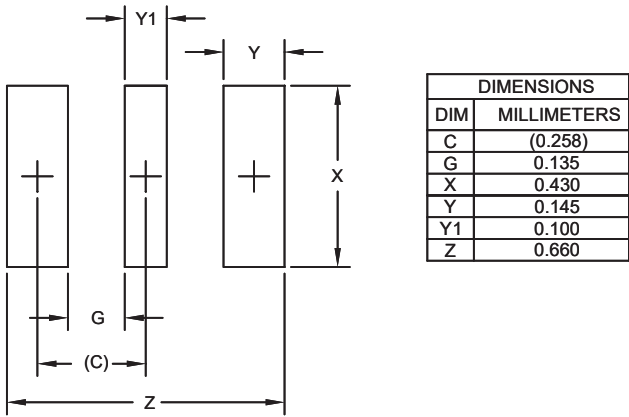
Table 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.075mm (0.003")
Solder Paste Type	Type 4 Size Sphere or Smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Solder Mask Defined (Preferred) or Non Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - DFN 0.62 x 0.32 x 0.25 mm 3-Lead



Landing Pattern - DFN 0.62 x 0.32 x 0.25 mm 3-Lead



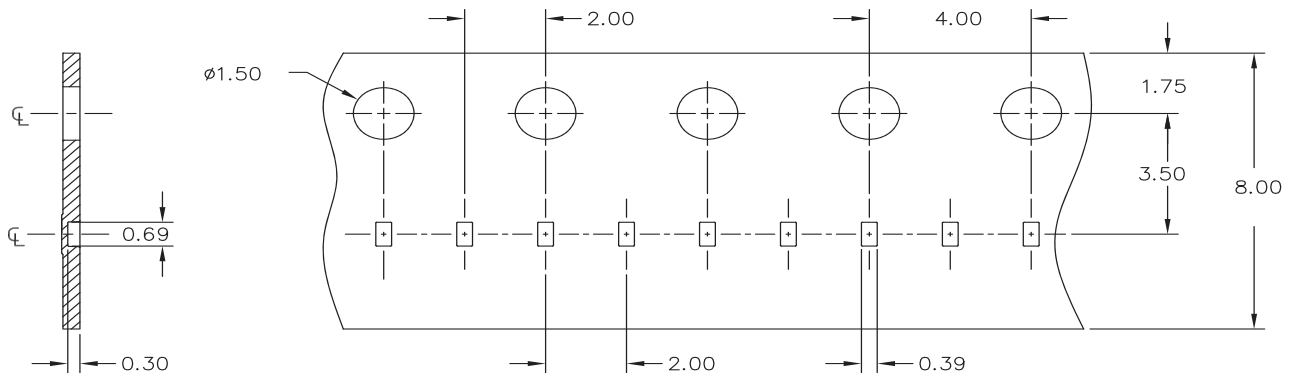
- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

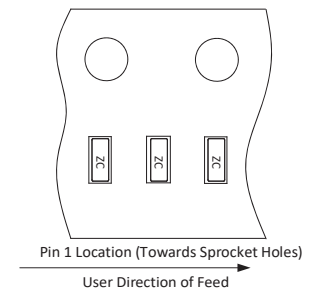
ZC

Note: Device is electrically symmetrical.

Tape and Reel Specification



Note: All dimensions are nominal dimensions in mm.



Order Information

PART NUMBER	QTY PER REEL	REEL SIZE
RClamp2272ZC.F	15,000	7"

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