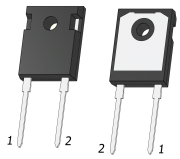
Silicon Carbide (SiC) Diode – EliteSiC, TO247-2, 10 A, 1200 V SiC Merged PiN-Schottky (MPS) Diode

UJ3D1210K2



TO247-2
CASE 340CY

Description

onsemi offers the 3rd generation of high performance SiC Merged-PiN-Schottky (MPS) diodes. With zero reverse recovery charge and 175 °C maximum junction temperature, these diodes are ideally suited for high frequency and high efficiency power systems with minimum cooling requirements.

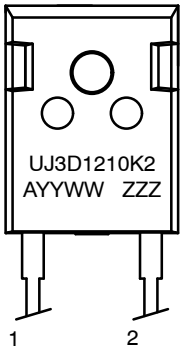
Features

- Maximum Operating Temperature of 175 °C
- Easy Paralleling
- Extremely Fast Switching not Dependent on Temperature
- No Reverse or Forward Recovery
- Enhanced Surge Current Capability, MPS Structure
- 100% UIS Tested
- This Device is Halogen Free and RoHS Compliant with Exemption 7a, Pb−Free 2LI (on second level interconnection)

Typical Applications

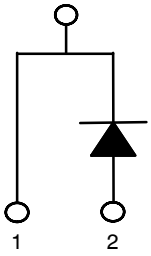
- Power Converters
- Industrial Motor Drives
- Switch Mode Power Supplies
- Power Factor Correction Modules

MARKING DIAGRAM



UJ3D1210K2	= Specific Device Code
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
DC Blocking Voltage	V_R		1200	V
Repetitive Peak Reverse Voltage, T_J = 25 °C	V_{RRM}		1200	V
Surge Peak Reverse Voltage	V_{RSM}		1200	V
Maximum DC Forward Current	I_F	T_C = 146 °C	10	A
Non-repetitive Forward Surge Current Sine Halfwave	I_{FSM}	T_C = 25 °C, t_p = 10 ms	120	A
		T_C = 110 °C, t_p = 10 ms	110	
Repetitive Forward Surge Current Sine Halfwave, D = 0.1	I_{FRM}	T_C = 25 °C, t_p = 10 ms	39.4	A
		T_C = 110 °C, t_p = 10 ms	24	
Non-repetitive Peak Forward Current	$I_{F, max}$	T_C = 25 °C, t_p = 10 μs	720	A
		T_C = 110 °C, t_p = 10 μs	720	
i^2t Value	$\int i^2dt$	T_C = 25 °C, t_p = 10 ms	72	A^2s
		T_C = 110 °C, t_p = 10 ms	60	
Power Dissipation	P_{tot}	T_C = 25 °C	136.4	W
		T_C = 146 °C	26.4	
Maximum Junction Temperature	$T_{J, max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Soldering Temperatures, Wavesoldering only Allowed at Leads	T_{sold}	1.6 mm from case for 10 s	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		–	0.83	1.1	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward Voltage	V_F	I_F = 10 A, T_J = 25 °C	–	1.4	1.6	V
		I_F = 10 A, T_J = 150 °C	–	1.85	2.3	
		I_F = 10 A, T_J = 175 °C	–	2	2.6	
Reverse Current	I_R	V_R = 1200 V, T_J = 25 °C	–	10	110	μA
		V_R = 1200 V, T_J = 175 °C	–	450	–	
Total Capacitive Charge (Note 1)	Q_C	V_R = 800 V	–	51	–	nC
Total Capacitance	C	V_R = 1 V, f = 1 MHz	–	510	–	pF
		V_R = 400 V, f = 1 MHz	–	48	–	
		V_R = 800 V, f = 1 MHz	–	41	–	
Capacitance Stored Energy	E_C	V_R = 800 V	–	15	–	μJ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Q_C is independent on T_J, di_F/dt, and I_F as shown in the application note AND90316/D

TYPICAL PERFORMANCE DIAGRAMS

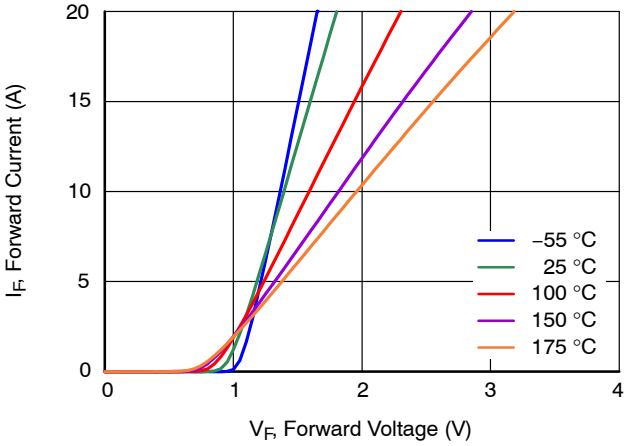


Figure 1. Typical Forward Characteristics

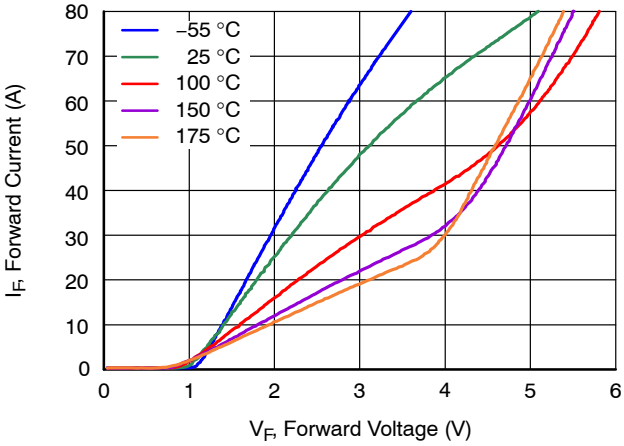


Figure 2. Typical Forward Characteristics in Surge Current

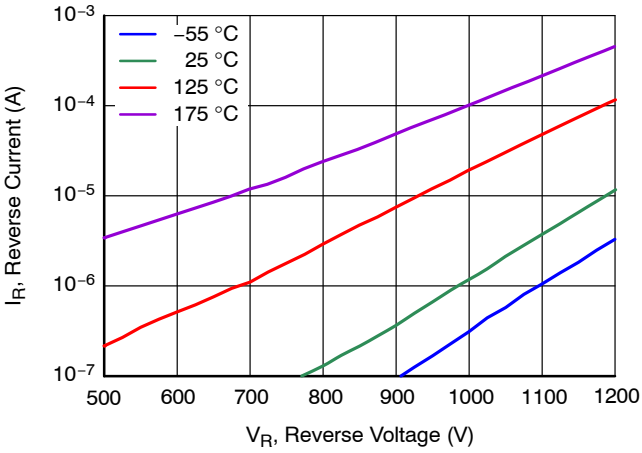


Figure 3. Typical Reverse Characteristics

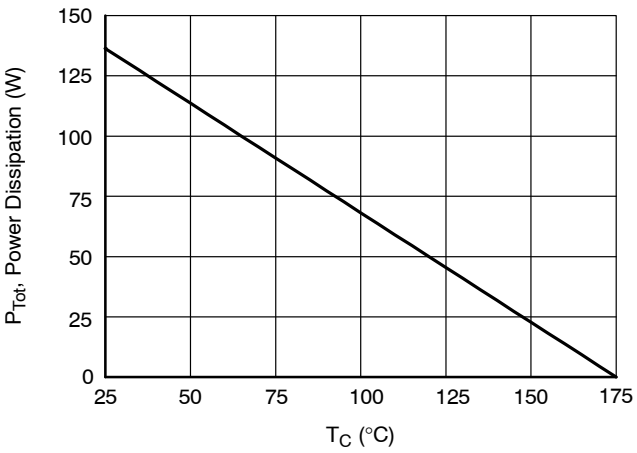


Figure 4. Power Dissipation

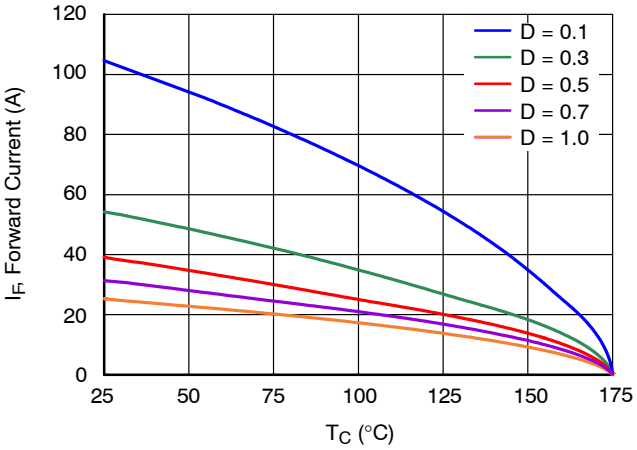


Figure 5. Diode Forward Current

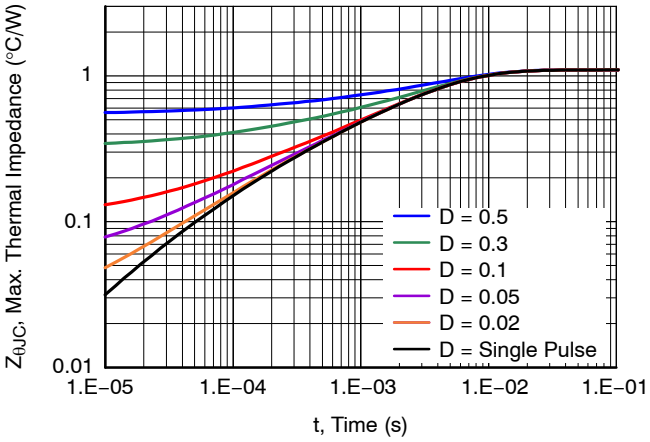


Figure 6. Maximum Transient Thermal Impedance

TYPICAL PERFORMANCE DIAGRAMS (continued)

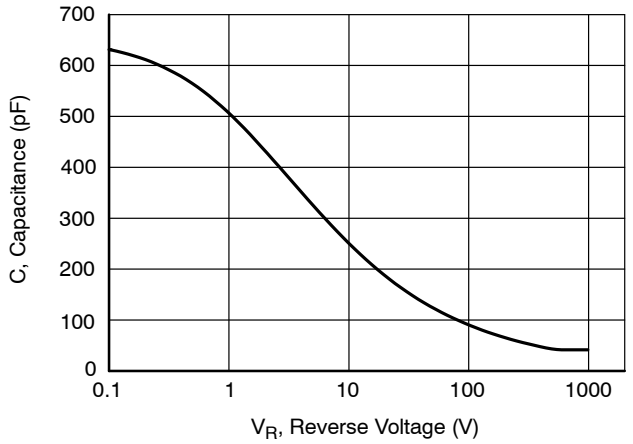


Figure 7. Capacitance vs. Reverse Voltage at 1 MHz

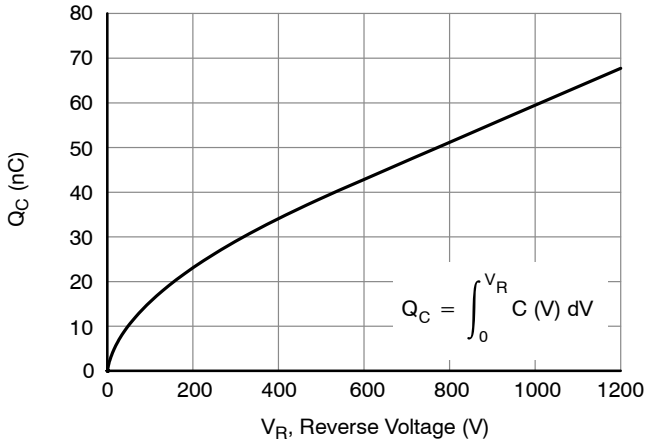


Figure 8. Typical Capacitive Charge vs. Reverse Voltage

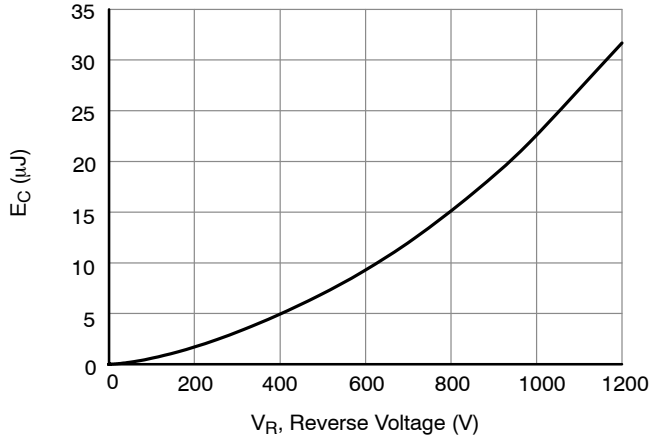


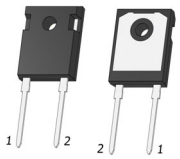
Figure 9. Typical Capacitance Stored Energy vs. Reverse Voltage

ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UJ3D1210K2	UJ3D1210K2	TO247-2 (Pb-Free, Halogen Free)	600 Units / Tube

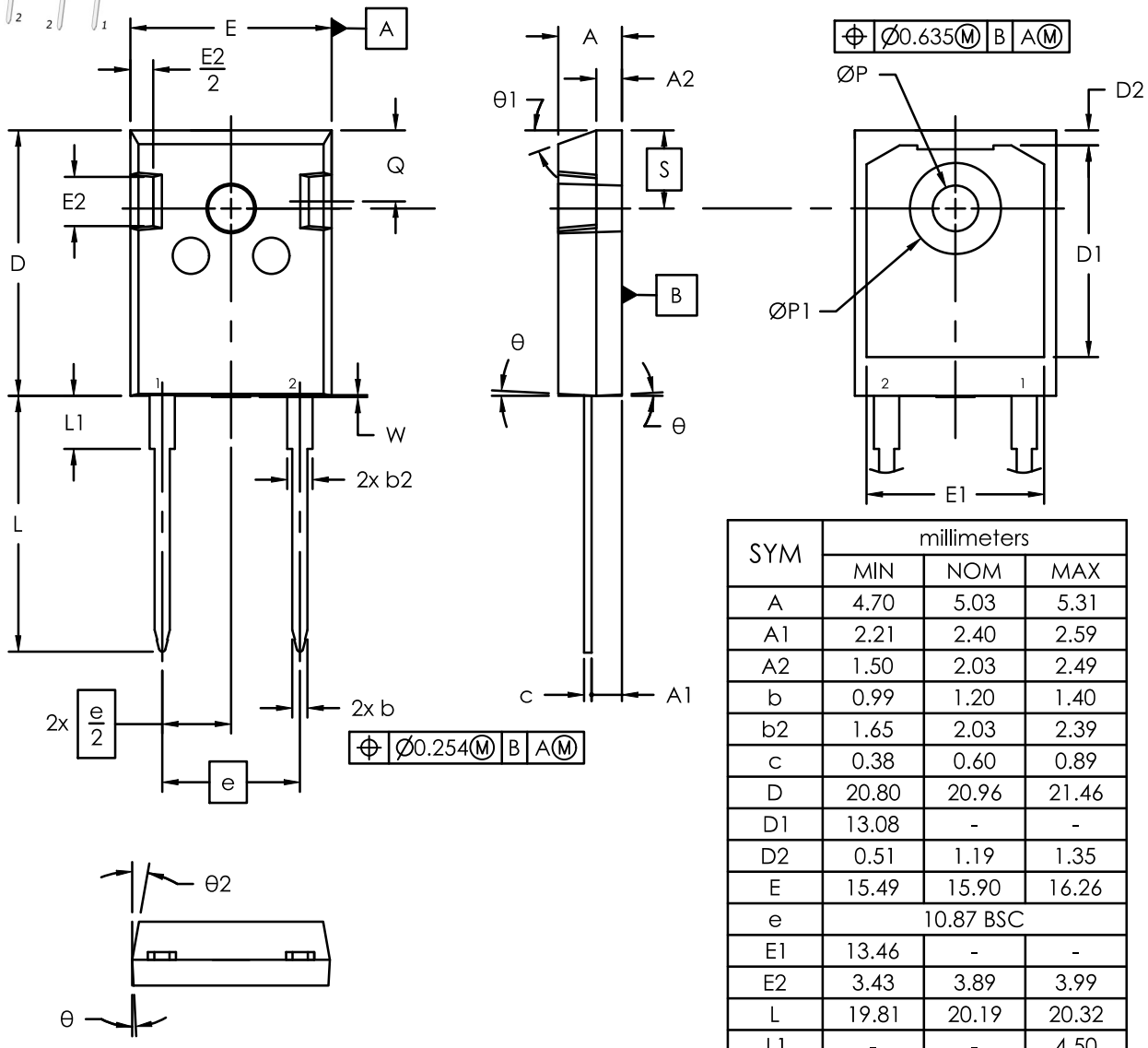
REVISION HISTORY

Revision	Description of Changes	Date
C	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with **onsemi** standards for SiC products.	1/15/2025
3	Converted the Data Sheet to **onsemi** format.	5/13/2025



TO247−2 15.90x20.96x5.03, 5.44P
CASE 340CY
ISSUE B

DATE 16 APR 2025



SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	-	-
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	10.87 BSC		
E1	13.46	-	-
E2	3.43	3.89	3.99
L	19.81	20.19	20.32
L1	-	-	4.50
ØP	3.56	3.60	3.66
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
W	-	-	0.15
θ	3°		
θ1	20°		
θ2	10°		

NOTE:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Dimension "W" = max. allowable plastic protrusion.
4. Package Outline in compliance with JEDEC standard var. AD.
5. Dimensions D & E does not include mold flash.
6. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.

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DESCRIPTION:	**TO247−2 15.90x20.96x5.03, 5.44P**	**PAGE 1 OF 1**

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