

# 3.3 V/5 V ECL D Flip-Flop with Set and Reset

## MC100EP31

### Description

The MC100EP31 is a D flip-flop with set and reset. The device is pin and functionally equivalent to the EL31 and LVEL31 devices. With AC performance much faster than the EL31 and LVEL31 devices, the EP31 is ideal for applications requiring the fastest AC performance available. Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when CLK is low and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK.

The 100 Series contains temperature compensation.

### Features

- 340 ps Typical Propagation Delay
- Maximum Frequency = > 3 GHz Typical
- PECL Mode Operating Range:  
 $V_{CC} = 3.0\text{ V to }5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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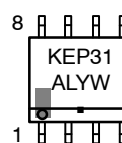


**SOIC-8 NB**  
**D SUFFIX**  
**CASE 751-07**

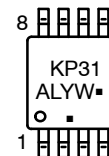


**TSSOP-8**  
**DT SUFFIX**  
**CASE 948R-02**

### MARKING DIAGRAMS\*



**SOIC-8 NB**



**TSSOP-8**

K = MC100  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

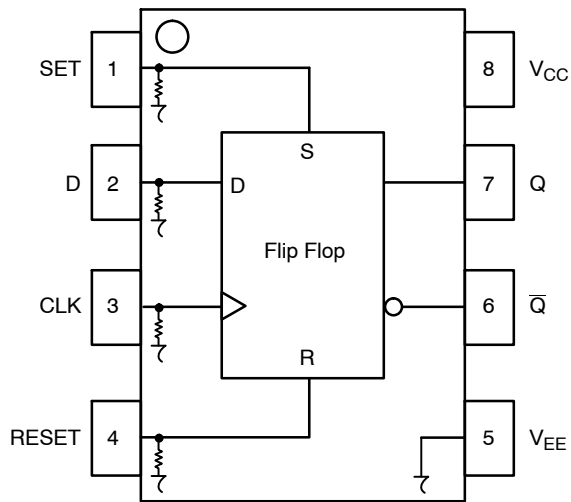
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device       | Package                | Shipping†        |
|--------------|------------------------|------------------|
| MC100EP31DG  | SOIC-8 NB<br>(Pb-Free) | 98 Units / Tube  |
| MC100EP31DTG | TSSOP-8<br>(Pb-Free)   | 100 Units / Tube |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100EP31



**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

| Pin             | Function               |
|-----------------|------------------------|
| CLK*            | ECL Clock Inputs       |
| Reset*          | ECL Asynchronous Reset |
| Set*            | ECL Asynchronous Set   |
| D*              | ECL Data Input         |
| Q, $\bar{Q}$    | ECL Data Outputs       |
| V <sub>CC</sub> | Positive Supply        |
| V <sub>EE</sub> | Negative Supply        |

\*Pins will default LOW when left open.

**Table 2. TRUTH TABLE**

| D | SET | RESET | CLK | Q     |
|---|-----|-------|-----|-------|
| L | L   | L     | Z   | L     |
| H | L   | L     | Z   | H     |
| X | H   | L     | X   | H     |
| X | L   | H     | X   | L     |
| X | H   | H     | X   | UNDEF |

Z = LOW to HIGH Transition

**Table 3. ATTRIBUTES**

| Characteristics                                                             | Value                       |
|-----------------------------------------------------------------------------|-----------------------------|
| Internal Input Pulldown Resistor                                            | 75 k $\Omega$               |
| Internal Input Pullup Resistor                                              | N/A                         |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 4 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)               | Pb-Free Pkg                 |
| SOIC-8 NB<br>TSSOP-8                                                        | Level 1<br>Level 3          |
| Flammability Rating<br>Oxygen Index: 28 to 34                               | UL 94 V-0 @ 0.125 in        |
| Transistor Count                                                            | 75 Devices                  |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                      |                             |

1. For additional information, see Application Note [AND8003/D](#).

# MC100EP31

**Table 4. MAXIMUM RATINGS**

| Symbol        | Parameter                                          | Condition 1                                    | Condition 2                            | Rating      | Unit |
|---------------|----------------------------------------------------|------------------------------------------------|----------------------------------------|-------------|------|
| $V_{CC}$      | PECL Mode Power Supply                             | $V_{EE} = 0\text{ V}$                          |                                        | 6           | V    |
| $V_{EE}$      | NECL Mode Power Supply                             | $V_{CC} = 0\text{ V}$                          |                                        | -6          | V    |
| $V_I$         | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$<br>$V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>-6     | V    |
| $I_{out}$     | Output Current                                     | Continuous<br>Surge                            |                                        | 50<br>100   | mA   |
| $T_A$         | Operating Temperature Range                        |                                                |                                        | -40 to +85  | °C   |
| $T_{stg}$     | Storage Temperature Range                          |                                                |                                        | -65 to +150 | °C   |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-8 NB<br>SOIC-8 NB                 | 190<br>130  | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SOIC-8 NB                              | 41 to 44    | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP-8<br>TSSOP-8                     | 185<br>140  | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | TSSOP-8                                | 41 to 44    | °C/W |
| $T_{sol}$     | Wave Solder (Pb-Free)                              | < 2 to 3 sec @ 260°C                           |                                        | 265         | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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**Table 5. 100EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

| Symbol   | Characteristic                    | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|----------|-----------------------------------|-------|------|------|------|------|------|------|------|------|------|
|          |                                   | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| $I_{EE}$ | Power Supply Current              | 26    | 34   | 44   | 26   | 35   | 45   | 28   | 37   | 47   | mA   |
| $V_{OH}$ | Output HIGH Voltage (Note 2)      | 2155  | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV   |
| $V_{OL}$ | Output LOW Voltage (Note 2)       | 1355  | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV   |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2075  |      | 2420 | 2075 |      | 2420 | 2075 |      | 2420 | mV   |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | 1355  |      | 1675 | 1355 |      | 1675 | 1355 |      | 1675 | mV   |
| $I_{IH}$ | Input HIGH Current                |       |      | 150  |      |      | 150  |      |      | 150  | μA   |
| $I_{IL}$ | Input LOW Current                 | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
2. All loading with 50 Ω to  $V_{CC} - 2.0\text{ V}$ .

**Table 6. 100EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

| Symbol   | Characteristic                    | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|----------|-----------------------------------|-------|------|------|------|------|------|------|------|------|------|
|          |                                   | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| $I_{EE}$ | Power Supply Current              | 26    | 34   | 44   | 26   | 35   | 45   | 28   | 37   | 47   | mA   |
| $V_{OH}$ | Output HIGH Voltage (Note 2)      | 3855  | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV   |
| $V_{OL}$ | Output LOW Voltage (Note 2)       | 3055  | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV   |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3775  |      | 4120 | 3775 |      | 4120 | 3775 |      | 4120 | mV   |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | 3055  |      | 3375 | 3055 |      | 3375 | 3055 |      | 3375 | mV   |
| $I_{IH}$ | Input HIGH Current                |       |      | 150  |      |      | 150  |      |      | 150  | μA   |
| $I_{IL}$ | Input LOW Current                 | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
2. All loading with 50 Ω to  $V_{CC} - 2.0\text{ V}$ .

**Table 7. 100EP DC CHARACTERISTICS, NECL** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 1))

| Symbol   | Characteristic                    | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit |
|----------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|
|          |                                   | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |      |
| $I_{EE}$ | Power Supply Current              | 26    | 34    | 44    | 26    | 35    | 45    | 28    | 37    | 47    | mA   |
| $V_{OH}$ | Output HIGH Voltage (Note 2)      | -1145 | -1020 | -895  | -1145 | -1020 | -895  | -1145 | -1020 | -895  | mV   |
| $V_{OL}$ | Output LOW Voltage (Note 2)       | -1945 | -1820 | -1695 | -1945 | -1820 | -1695 | -1945 | -1820 | -1695 | mV   |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | -1225 |       | -880  | -1225 |       | -880  | -1225 |       | -880  | mV   |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | -1945 |       | -1625 | -1945 |       | -1625 | -1945 |       | -1625 | mV   |
| $I_{IH}$ | Input HIGH Current                |       |       | 150   |       |       | 150   |       |       | 150   | μA   |
| $I_{IL}$ | Input LOW Current                 | 0.5   |       |       | 0.5   |       |       | 0.5   |       |       | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with 50 Ω to  $V_{CC} - 2.0\text{ V}$ .

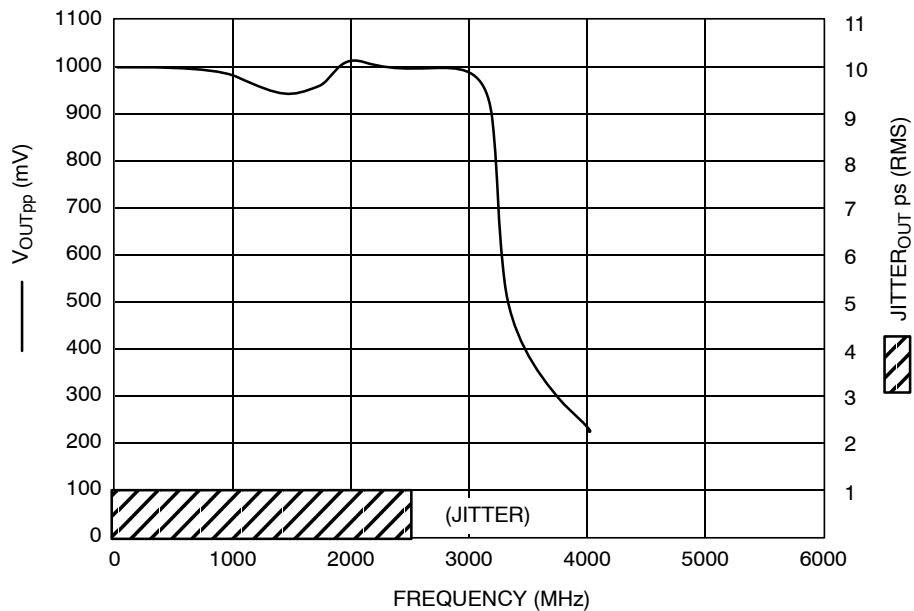
# MC100EP31

**Table 8. AC CHARACTERISTICS** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 1))

| Symbol                   | Characteristic                                                                             | -40°C      |            |            | 25°C       |            |            | 85°C       |            |            | Unit |
|--------------------------|--------------------------------------------------------------------------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------|
|                          |                                                                                            | Min        | Typ        | Max        | Min        | Typ        | Max        | Min        | Typ        | Max        |      |
| $f_{\max}$               | Maximum Frequency<br>(Figure 2)                                                            |            | > 3        |            |            | > 3        |            |            | > 3        |            | GHz  |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to<br>Output Differential<br>CLK to Q, $\bar{Q}$<br>S, R to Q, $\bar{Q}$ | 250<br>300 | 330<br>380 | 400<br>450 | 270<br>330 | 340<br>400 | 410<br>470 | 300<br>360 | 370<br>430 | 440<br>500 | ps   |
| $t_{RR}$                 | Set/Reset Recovery                                                                         | 225        |            |            | 225        |            |            | 225        |            |            | ps   |
| $t_S$<br>$t_H$           | Setup Time<br>Hold Time                                                                    | 100<br>150 |            |            | 100<br>150 |            |            | 100<br>150 |            |            | ps   |
| $t_{PW}$                 | Minimum Pulse width<br>SET, RESET                                                          | 550        | 450        |            | 550        | 450        |            | 550        | 450        |            | ps   |
| $t_{JITTER}$             | Cycle-to-Cycle Jitter<br>(Figure 2)                                                        |            | 0.2        | < 1        |            | 0.2        | < 1        |            | 0.2        | < 1        | ps   |
| $t_r$<br>$t_f$           | Output Rise/Fall Times<br>Q, $\bar{Q}$ (20% – 80%)                                         | 50         | 120        | 180        | 60         | 130        | 200        | 70         | 150        | 220        | ps   |

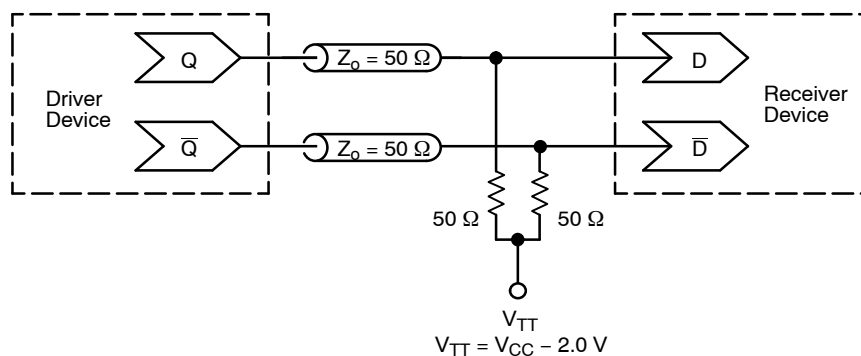
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC}-2.0\text{ V}$ .



**Figure 2.  $F_{\max}$ /Jitter**

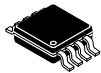
## MC100EP31



**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

### Resource Reference of Application Notes

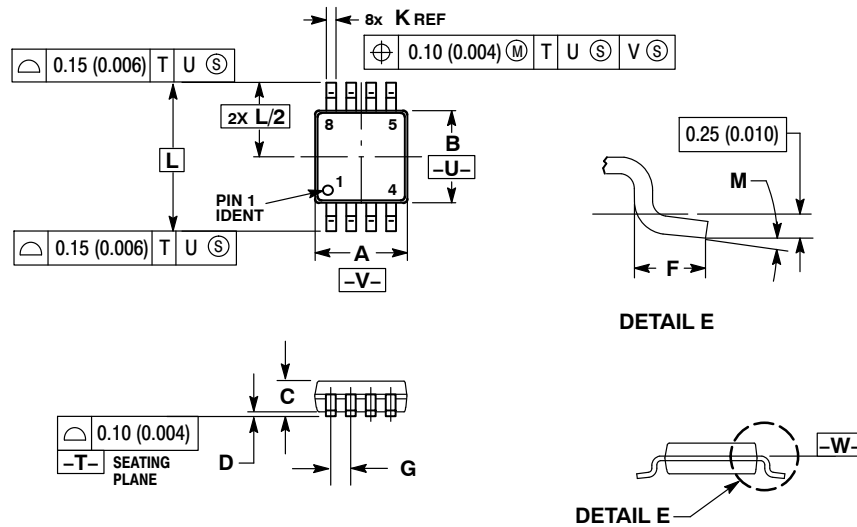
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices



SCALE 2:1

**TSSOP-8 3.00x3.00x0.95**  
CASE 948R-02  
ISSUE A

DATE 07 APR 2000



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

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DESCRIPTION: TSSOP-8 3.00x3.00x0.95

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