

Dual J-K Flip-Flops with Preset and Clear

74VHC112

General Description

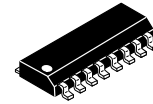
The VHC112 is an advanced high speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. The LOW signal on PR or CLR prevents clocking and forces Q and $\bar{Q}$ HIGH, respectively. Simultaneous LOW signals on PR and CLR force both Q and $\bar{Q}$ HIGH.

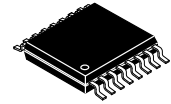
An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: $f_{MAX} = 200$ MHz (Typ.) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max.) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (Min.)
- Power Down Protection is Provided on All Inputs
- Pin and Function Compatible with 74HC112
- These are Pb-Free Devices

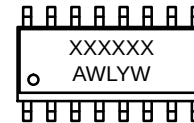


SOIC-16, 150 mils
CASE 751BG

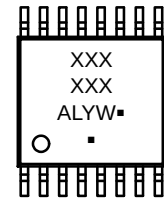


TSSOP 16
CASE 948AH

MARKING DIAGRAM



SOIC-16



TSSOP 16

XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

74VHC112

Connection Diagram

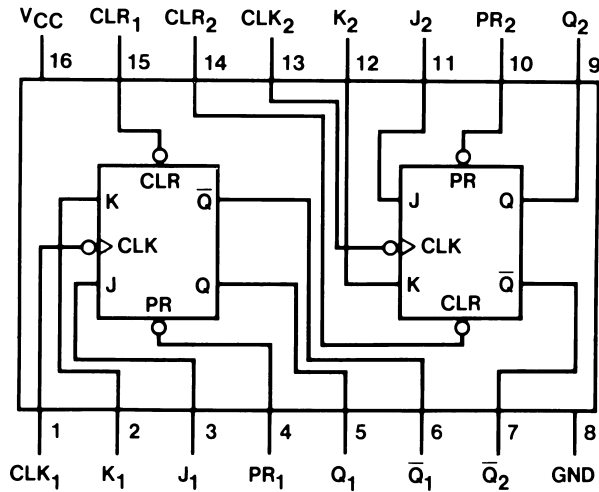


Figure 1. Connection Diagram

TRUTH TABLE

Input					Outputs	
PR	CLR	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\sim$	h	h	$\overline{Q}_0$	Q_0
H	H	$\sim$	l	h	L	H
H	H	$\sim$	h	l	H	L
H	H	$\sim$	l	l	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

X = Immaterial

$\sim$ = HIGH-to-LOW Clock Transition

Q_0 ($\overline{Q}_0$) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

PIN DESCRIPTION

Pin Names	Description
J_1, J_2, K_1, K_2	Data Inputs
CLK_1, CLK_2	Clock Pulse Inputs (Active Falling Edge)
CLR_1, CLR_2	Direct Clear Inputs (Active LOW)
PR_1, PR_2	Direct Preset Inputs (Active LOW)
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

Logic Diagram (One Half Shown)

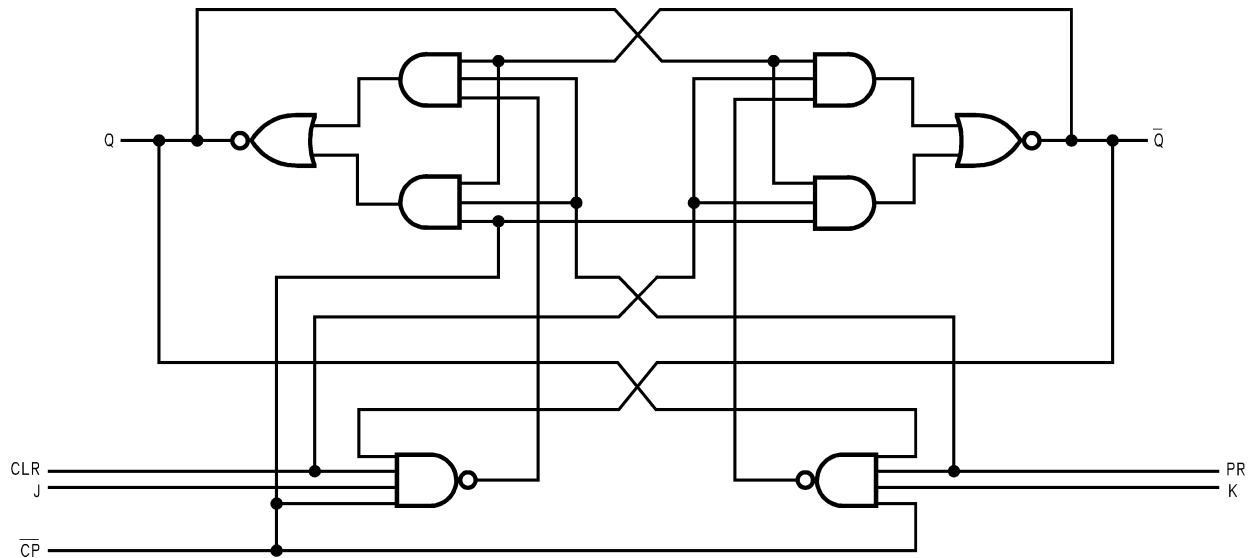


Figure 2. Logic Diagram (One Half Shown)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		−0.5 to +6.5	V
V _{IN}	DC Input Voltage		−0.5 to +6.5	V
V _{OUT}	DC Output Voltage		−0.5 to V _{CC} + 0.5	V
I _{IN}	DC Input Current, per Pin		±20	mA
I _{OUT}	DC Output Current, per Pin		±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins		±75	mA
I _{IK}	Input Clamp Current		−20	mA
I _{OK}	Output Clamp Current		±20	mA
T _{STG}	Storage Temperature Range		−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T _J	Junction Temperature Under Bias		+150	°C
θ _{JA}	Thermal Resistance (Note 2)	SOIC-16	126	°C/W
		TSSOP 16	159	
P _D	Power Dissipation in Still Air at 25°C	SOIC-16	995	mW
		TSSOP 16	787	
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.112 in	
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage		2.0	5.5	V
V _{IN}	DC Input Voltage (Note 4)		0	5.5	V
V _{OUT}	DC Output Voltage (Note 4)		0	V _{CC}	V
T _A	Operating Temperature		−40	+85	°C
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 3.0 V to 3.6 V	0	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			T _A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		2.0	1.50	–	–	1.50	–	V
			3.0–5.5	0.7 × V _{CC}	–	–	0.7 × V _{CC}	–	
V _{IL}	LOW Level Input Voltage		2.0	–	–	0.50	–	0.50	V
			3.0–5.5	–	–	0.3 × V _{CC}	–	0.3 × V _{CC}	
V _{OH}	HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = –50 μA	2.0	1.9	2.0	–	1.9	V
				3.0	2.9	3.0	–	2.9	
				4.5	4.4	4.5	–	4.4	
			I _{OH} = –4 mA	3.0	2.58	–	–	2.48	
			I _{OH} = –8 mA	4.5	3.94	–	–	3.80	
V _{OL}	LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	–	0.0	0.1	–	V
				3.0	–	0.0	0.1	–	
				4.5	–	0.0	0.1	–	
			I _{OL} = 4 mA	3.0	–	–	0.36	–	
			I _{OL} = 8 mA	4.5	–	–	0.36	–	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0–5.5	–	–	±0.1	–	±1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	–	–	2.0	–	20.0	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			T _A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	C _L = 15 pF	3.3 ±0.3	110	150	–	100	–	MHz
		C _L = 50 pF		90	120	–	80	–	
		C _L = 15 pF	5.0 ±0.5	150	200	–	135	–	MHz
		C _L = 50 pF		120	185	–	110	–	
t _{PLH} , t _{PHL}	Propagation Delay Time (CP to Q _n or $\bar{Q}_n$)	C _L = 15 pF	3.3 ±0.3	–	8.5	11.0	1.0	13.4	ns
		C _L = 50 pF		–	10.0	15.0	1.0	16.5	
		C _L = 15 pF	5.0 ±0.5	–	5.1	7.3	1.0	8.8	ns
		C _L = 50 pF		–	6.3	10.5	1.0	12.0	
t _{PLH} , t _{PHL}	Propagation Delay Time (PR or CLR to Q _n or $\bar{Q}_n$)	C _L = 15 pF	3.3 ±0.3	–	6.7	10.2	1.0	11.7	ns
		C _L = 50 pF		–	9.7	13.5	1.0	15.0	
		C _L = 15 pF	5.0 ±0.5	–	4.6	6.7	1.0	8.0	ns
		C _L = 50 pF		–	6.4	9.5	1.0	11.0	
C _{IN}	Input Capacitance	V _{CC} = Open		–	4	10	–	10	pF
C _{PD}	Power Dissipation Capacitance	(Note 5)		–	18	–	–	–	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation:
 $I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4$ (per F/F), and the total C_{PD} when n pcs of the Flip-Flop operate can be calculated by the following equation:
 $C_{PD}(\text{total}) = 30 + 14 \cdot n$

AC ELECTRICAL REQUIREMENTS

Symbol	Parameter	V _{CC} (V) (Note 6)	T _A = 25°C		T _A = −40°C to +85°C	Unit
			Typ	Guaranteed Minimum		
t _W	Minimum Pulse Width (CP or CLR or PR)	3.3	–	5.0	5.0	ns
		5.0	–	5.0	5.0	
t _S	Minimum Setup Time (J _n or K _n to CP _n)	3.3	–	5.0	5.0	ns
		5.0	–	4.0	4.0	
t _H	Minimum Hold Time (J _n or K _n to CP _n)	3.3	–	1.0	1.0	ns
		5.0	–	1.0	1.0	
t _{REC}	Minimum Recovery Time (CLR or PR to CP)	3.3	–	6.0	6.0	ns
		5.0	–	5.0	5.0	

6. V_{CC} is 3.3 ±0.3 V or 5.0 ±0.5 V.

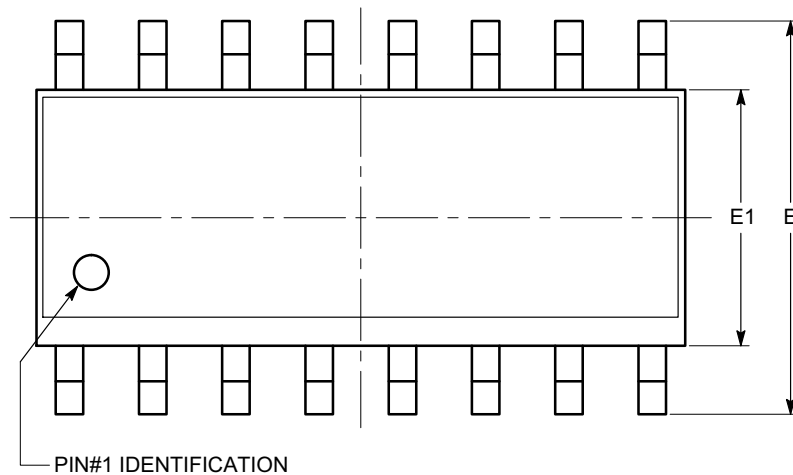
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
74VHC112MX	VHC112	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
74VHC112MTCX	VHC 112	TSSOP-16 (Pb-Free, Halide Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

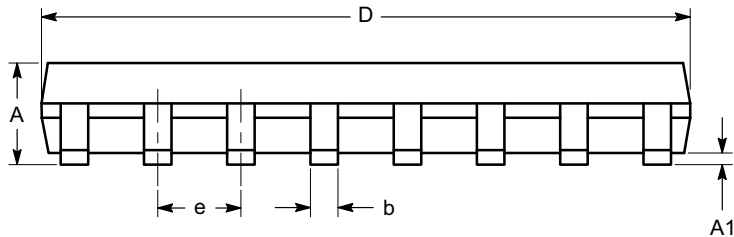
SOIC-16, 150 mils
CASE 751BG
ISSUE O

DATE 19 DEC 2008

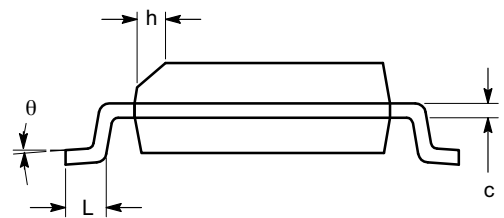


SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

Notes:

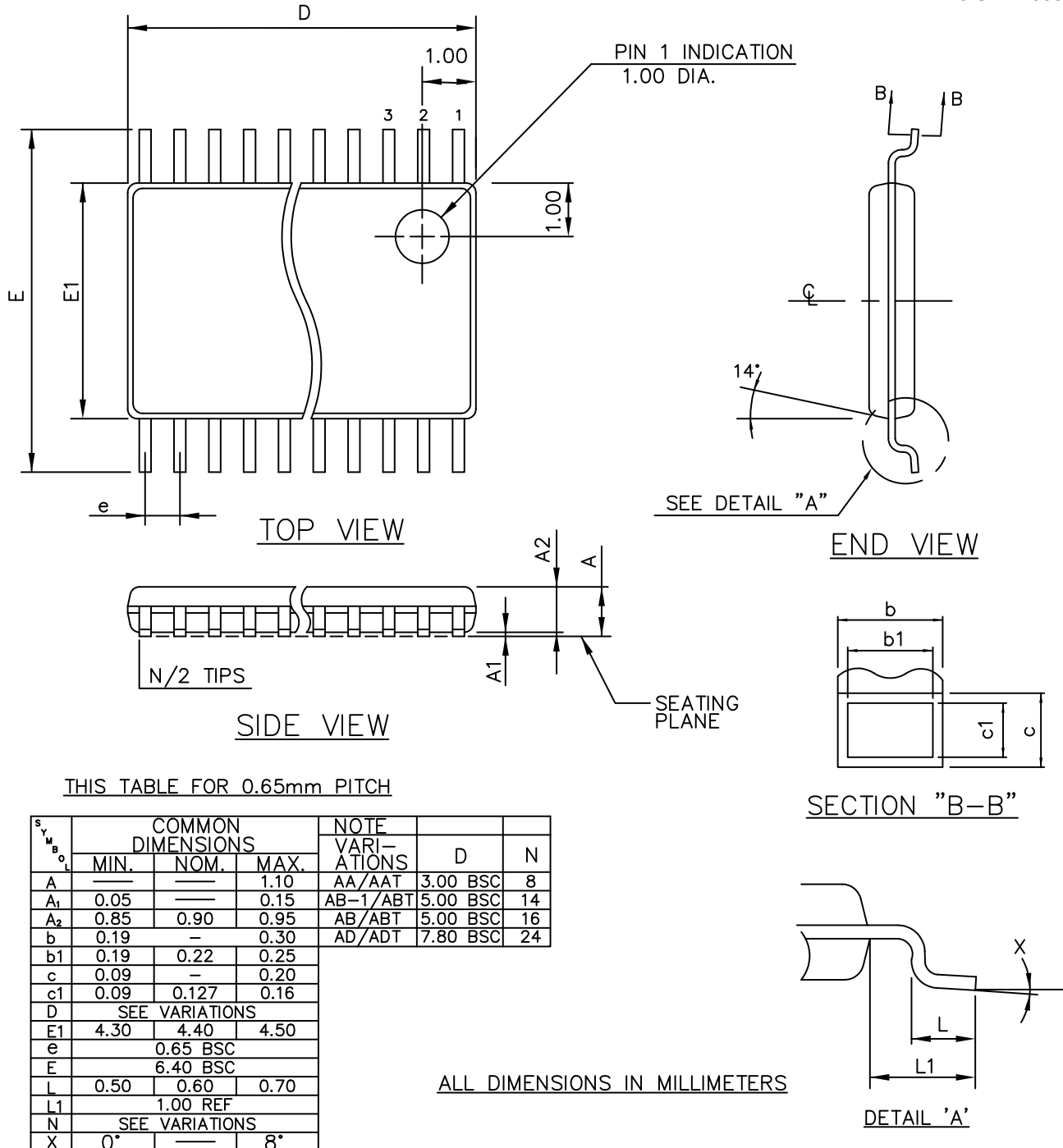
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

DOCUMENT NUMBER:	98AON34275E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16, 150 mils	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

TSSOP 16
CASE 948AH
ISSUE O

DATE 19 SEP 2008



MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

DOCUMENT NUMBER:	98AON34923E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP 16	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales