ESD4238

ESD Clamp Array with ESD Protection

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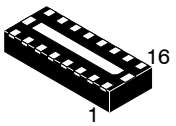
http://onsemi.com



WDFN16
CASE 511AU

Functional Description

The ESD4238 is ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading and tightly controlled signal skews (with channel−to−channel matching at 2% max deviation).

The device is particularly well−suited for protecting systems using high−speed ports such as DVI or HDMI, along with corresponding ports in removable storage, digital camcorders, DVD−RW drives and other applications where extremely low loading capacitance with ESD protection are required.

The ESD4238 also features easily routed "pass−through" pinouts in a RoHS−compliant (Pb−Free), 16−lead WDFN, small footprint package.

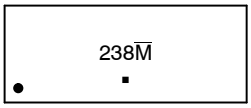
Features

- ESD Protection for Four Pairs of Differential Channels
- ESD protection to IEC61000−4−2 Level 4:
  - ♦ ±20 kV contact discharge
  - ♦ ±25 kV air discharge
- Pass−through Impedance Matched Clamp Architecture
- Flow−through Routing for High−speed Signal Integrity
- 100 Ω Matched Impedance for Each Paired Differential Channel
- Capacitance Change with Temperature and Voltage
- Each I/O Pin Can Withstand Over 1000 ESD Strikes*
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

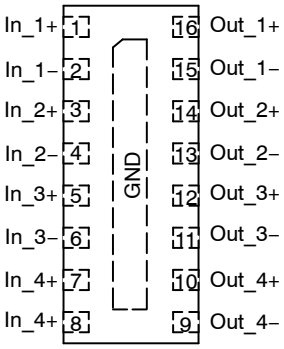
- DVI ports, HDMI Ports in Notebooks, Set−top Boxes, Digital TVs, LCD Displays
- General Purpose High−speed Data Line ESD Protection

MARKING DIAGRAM



238 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

*Standard test condition is IEC61000−4−2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

January, 2014 − Rev. 1

Publication Order Number:
ESD4238/D

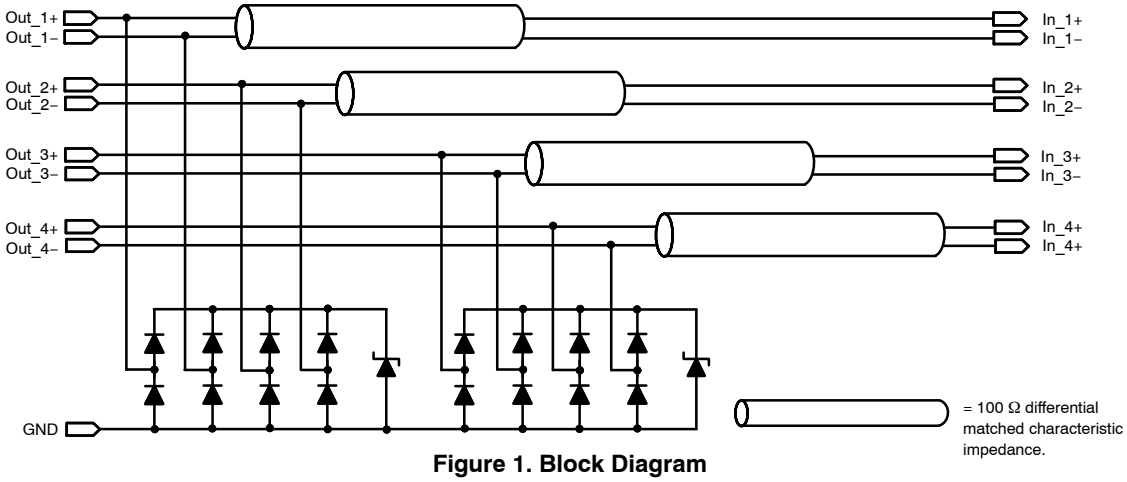


Figure 1. Block Diagram

ESD Protection Architecture

Conceptually, an ESD protection device performs the following actions upon an ESD strike discharge into a protected ASIC (see Figure 2):

1. When an ESD potential is applied to the system under test (contact or air−discharge), Kirchoff's Current Law (KCL) dictates that the Electrical Overstress (EOS) currents will immediately divide throughout the circuit, based on the dynamic impedance of each path.
2. Ideally, the classic shunt ESD clamp will switch within 1 ns to a low−impedance path and return the majority of the EOS current to the chassis shield/reference ground. In actuality, if the ESD component's response time (t_{CLAMP}) is slower than the ASIC it is protecting, or if the Dynamic Clamping Resistance (RDYN) is not significantly lower than the ASIC's I/O cell circuitry, then the ASIC will have to absorb a large amount of the EOS energy, and be more likely to fail.
3. Subsequent to the ESD/EOS event, both devices must immediately return to their original specifications, and be ready for an additional strike. Any deterioration in parasitics or clamping capability should be considered a failure, since it can then affect signal integrity or subsequent protection capability. (This is known as "multi−strike" capability.)

In the ESD4238 architecture, the signal line leading the connector to the ASIC routes through the ESD4238 chip which provides 100 Ω matched differential channel characteristic impedance that helps optimize 100 Ω load impedance applications such as the HDMI high speed data lines.

NOTES: When each of the channels is used individually for single−ended signal lines protection, the individual channel provides 50 Ω characteristic impedance matching.

The load impedance matching feature of the ESD4238 helps to simplify system designer's PCB layout considerations in impedance matching and also eliminates associated passive components.

The route through the architecture enables the ESD4238 to provide matched impedance for the signal path between the connector and the ASIC. Besides this function, this circuit arrangement also changes the way the parasitic inductance interacts with the ESD protection circuit and helps reduce the $I_{RESIDUAL}$ current to the ASIC.

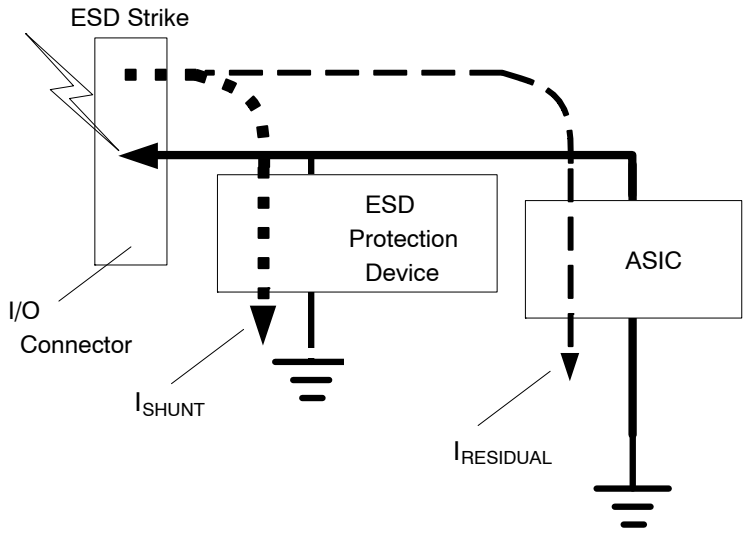


Figure 2. Standard ESD Protection Device Block Diagram

The Architecture Advantages

Figure 3 illustrates a standard ESD protection device. The inductor element represents the parasitic inductance arising from the bond wire and the PCB trace leading to the ESD protection diodes.

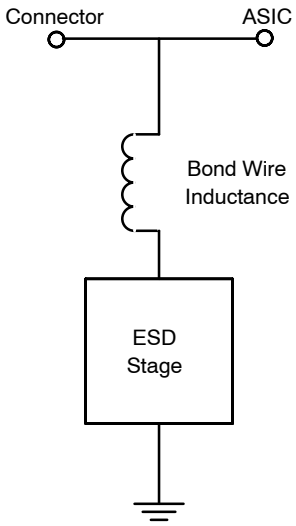


Figure 3. Standard ESD Protection Model

Figure 4 illustrates one of the channels. Similarly, the inductor elements represent the parasitic inductance arising from the bond wire and PCB traces leading to the ESD protection diodes as well.

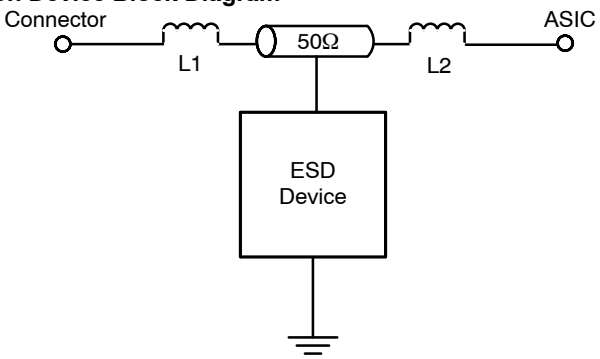


Figure 4. ESD4238 ESD Protection Model

ESD4238 Inductor Elements

In the ESD4238 architecture, the inductor elements and ESD protection diodes interact differently compared to the standard ESD model. In the standard ESD protection device model, the inductive element presents high impedance against high slew rate strike voltage, i.e. during an ESD strike. The impedance increases the resistance of the conduction path leading to the ESD protection element. This limits the speed that the ESD pulse can discharge through the ESD protection element.

In the architecture, the inductive elements are in series to the conduction path leading to the protected device. The elements actually help to limit the current and voltage striking the protected device.

First the reactance of the inductive element, L1, on the connector side when an ESD strike occurs, acts in the opposite direction of the ESD striking current. This helps limit the peak striking voltage. Then the reactance of the inductive element, L2, on the ASIC side forces this limited ESD strike current to be shunted through the ESD protection diodes. At the same time, the voltage drop across both series element acts to lower the clamping voltage at the protected device terminal.

Through this arrangement, the inductive elements also tune the impedance of the ESD protection element by cancelling the capacitive load presented by the ESD diodes to the signal line. This improves the signal integrity and makes the overall ESD protection device more transparent to the high bandwidth data signals passing through the channel.

The innovative architecture turns the disadvantages of the parasitic inductive elements into useful components that help to limit the ESD current strike to the protected device and also improves the signal integrity of the system by balancing the capacitive loading effects of the ESD diodes. At the same time, this architecture provides an impedance matched signal path for 50 Ω loading applications.

Precision Internal Component Matching

Board designs can take advantage of precision internal component matching for improved signal integrity, not otherwise possible with discrete components at the system level. This simplifies PCB layout considerations and eliminates associated passive components for load matching normally required by standard ESD protection circuits.

Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the Zener diode or to ground. This eliminates the need for a separate bypass capacitor to absorb positive ESD strikes. The ESD4238 protects against ESD pulses up to ±20 kV contact per the IEC 61000−4−2 standard.

PIN DESCRIPTIONS

Pin	Name	Description
1	In_1+	Bidirectional Clamp to ASIC (inside system)
2	In_1−	Bidirectional Clamp to ASIC (inside system)
3	In_2+	Bidirectional Clamp to ASIC (inside system)
4	In_2−	Bidirectional Clamp to ASIC (inside system)
5	In_3+	Bidirectional Clamp to ASIC (inside system)
6	In_3−	Bidirectional Clamp to ASIC (inside system)
7	In_4+	Bidirectional Clamp to ASIC (inside system)
8	In_4−	Bidirectional Clamp to ASIC (inside system)
9	Out_4−	Bidirectional Clamp to Connector (outside system)
10	Out_4+	Bidirectional Clamp to Connector (outside system)
11	Out_3−	Bidirectional Clamp to Connector (outside system)
12	Out_3+	Bidirectional Clamp to Connector (outside system)
13	Out_2−	Bidirectional Clamp to Connector (outside system)
14	Out_2+	Bidirectional Clamp to Connector (outside system)
15	Out_1−	Bidirectional Clamp to Connector (outside system)
16	Out_1+	Bidirectional Clamp to Connector (outside system)
PAD	GND	Ground return to shield

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
Breakdown Voltage (Positive)	6	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL OPERATING CHARACTERISTICS (See Note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	I/O Voltage Relative to GND		−0.5		5.5	V
I_{IN}	Continuous Current through signal pins (IN to OUT) 1000 Hr			100		mA
I_F	Channel Leakage Current	T_A = 25°C; V_N = 0 V, V_{TEST} = 5 V		0.1	1.0	μA
V_{ESD}	ESD Protection − Peak Discharge Voltage at any channel input, in system: a) Contact discharge per IEC 61000−4−2 Standard b) Air discharge per IEC 61000−4−2 Standard	 T_A = 25°C (Note 2) T_A = 25°C (Note 2)	 ±20 ±25			 kV kV
I_{RES}	Residual ESD Peak Current on RDUP (Resistance of Device Under Protection)	IEC 61000−4−2 8 kV; RDUP = 5 Ω, T_A = 25°C (Note 2)		3.8		A
V_{CL}	Channel Clamp Voltage (Channel clamp voltage per IEC 61000−4−5 Standard) Positive Transients Negative Transients	I_{PP} = 1 A, T_A = 25°C, t_P = 8/20 μs (Note 2)		 +10 −1.9		 V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1 A, T_A = 25°C t_P = 8/20 μs (Note 2)		 2.0 0.7		 Ω Ω
Zo	Differential Channels pair characteristic impedance	T_R = 200 ps (Note 2)		100		Ω
ΔZo	Channel−to−Channel Impedance Match (Differential)	T_R = 200 ps (Note 2)		2		%
$Z_{CHANNEL}$	Individual Channel Characteristic Impedance in Single−ended Connection	T_R = 200 ps		50		Ω
$\Delta Z_{CHANNEL}$	Channel−to−Channel Impedance Match (Individual)	T_R = 200 ps (Note 2)		2		%

1. All parameters specified at T_A = −40°C to +85°C unless otherwise noted.
2. This parameter is guaranteed by design and verified by device characterization.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PERFORMANCE INFORMATION

Graphical Comparison and Test Setup

Figure 5 shows that the ESD4238 lowers the peak voltage and clamping voltage by more than 60% across a wide range of loading conditions in comparison to a standard ESD protection device. Figure 6 also indicates that the DUP/ASIC protected by the ESD4238 dissipates less power than a standard ESD protection device. This data was derived using the test setups shown in Figure 7.

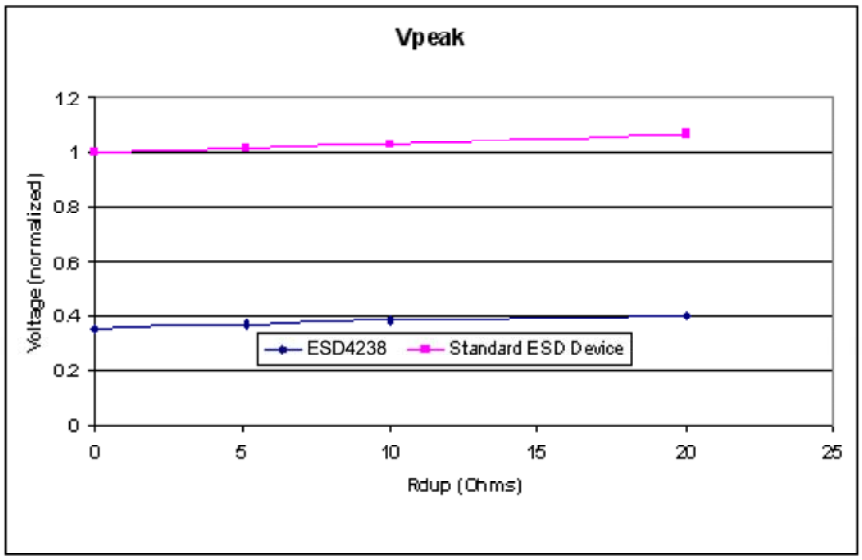


Figure 5. Normalized V_{Peak} (8 kV IEC−61000 4−2 ESD Contact Strike) vs. Loading (RDUP)*

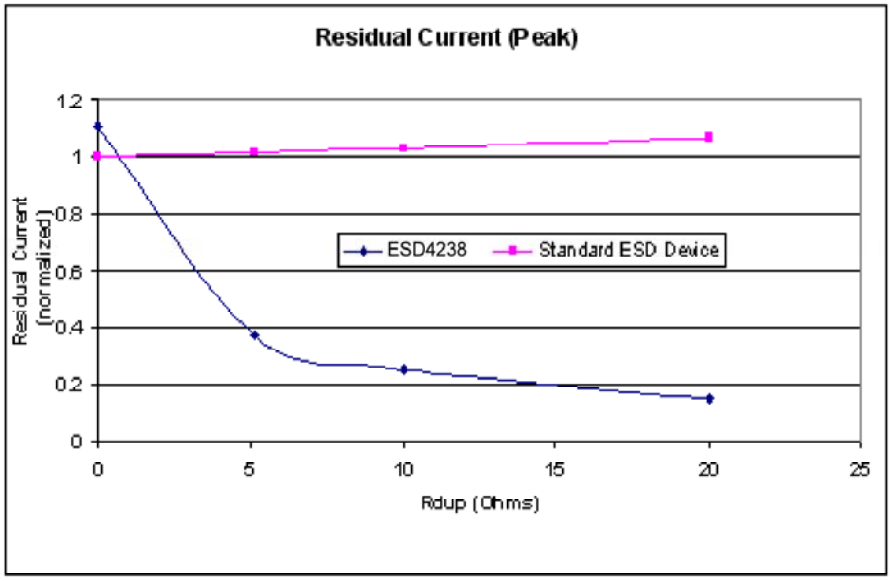


Figure 6. Normalized Residual Current into DUP vs. RDUP*

*RDUP is the emulated Dynamic Resistance (load) of the Device Under Protection (DUP). See Figure 7.

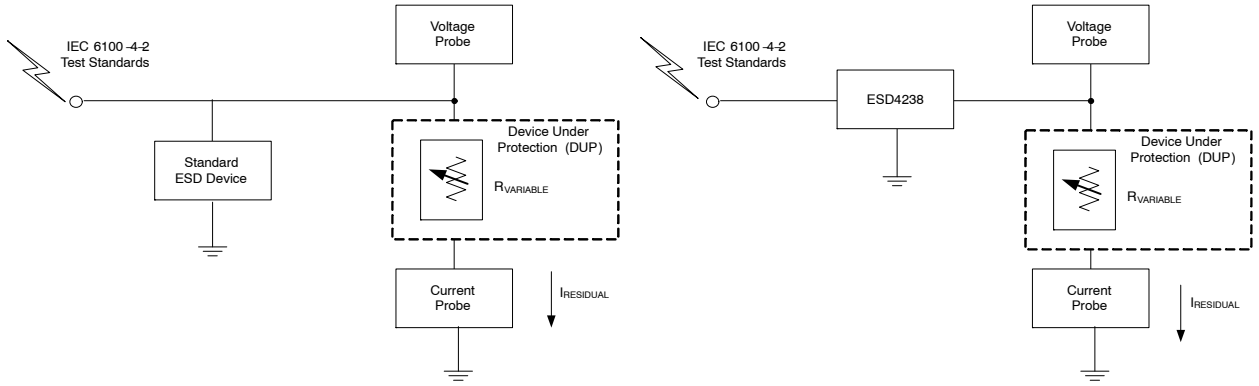


Figure 7. Test Setups: Standard Device (Left) and ESD4238 (Right)

ESD4238 Application and Guidelines

As a general rule, the ESD4238 ESD protection array should be located as close as possible to the point of entry of expected electrostatic discharges with minimum PCB trace lengths to the ground planes and between the signal input and the ESD device to minimize stray series inductance.

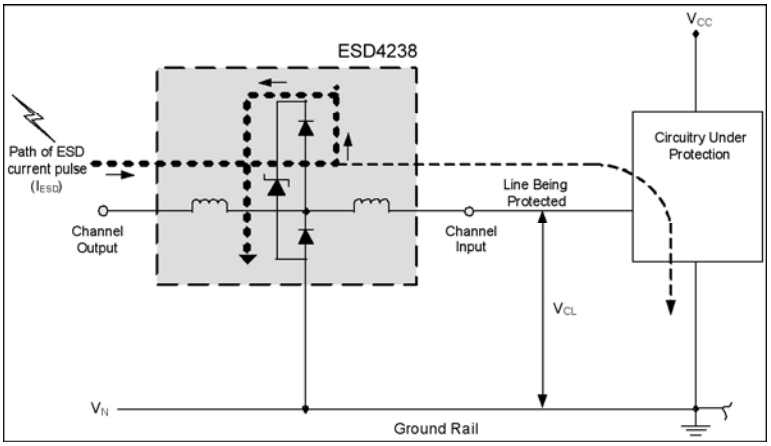


Figure 8. Application of Positive ESD Pulse Between Input Channel and Ground

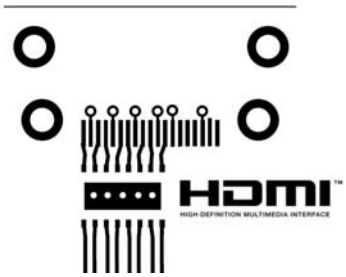


Figure 9. Typical PCB Layout

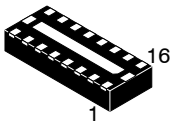
ORDERING INFORMATION

Ordering Part Number (Note 3)	Number of Pins	Part Marking (Note 4)	Package	Shipping
ESD4238MTTAG	16	238(M)	WDFN (Pb−Free)	3000 / Tape & Reel

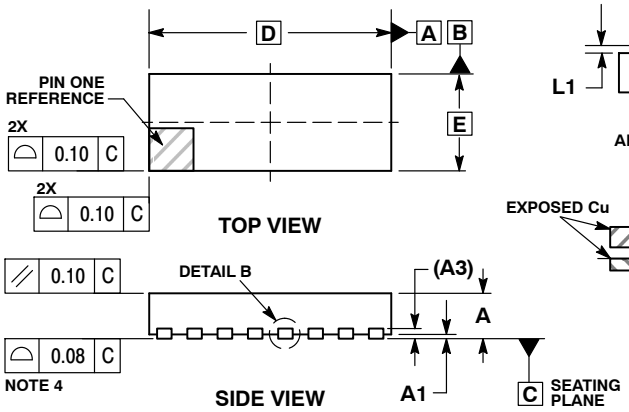
3. Parts are shipped in tape and reel form.
4. (M) is a 2−character datecode.

WDFN16, 4x1.6, 0.5P
CASE 511AU
ISSUE O

DATE 06 JUL 2010

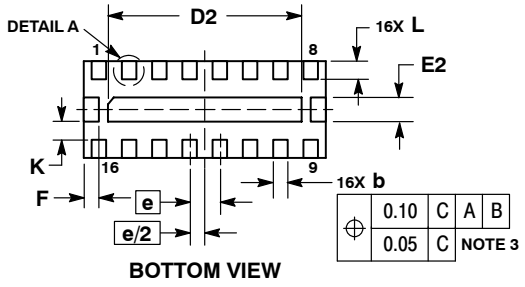


SCALE 4:1

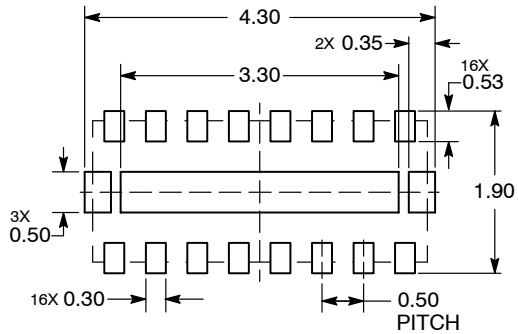


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	3.10	3.30
E	1.60 BSC	
E2	0.30	0.50
e	0.50 BSC	
F	0.25 REF	
K	0.30 REF	
L	0.20	0.40
L1	---	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WDFN16, 4X1.6, 0.5P**		**PAGE 1 OF 1**

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