High-Voltage Switcher for Low Power Offline SMPS

NCP1070, NCP1071, NCP1072, NCP1075, NCP1076, NCP1077

The NCP107x products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a PDIP−7 or SOT−223 package, the NCP107x offer a high level of integration, including soft−start, frequency−jittering, short−circuit protection, skip−cycle, a maximum peak current set point, ramp compensation, and a Dynamic Self−Supply (eliminating the need for an auxiliary winding).

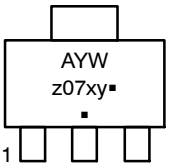
Unlike other monolithic solutions, the NCP107x is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (65, 100 or 130 kHz). When the output power demand diminishes, the IC automatically enters frequency foldback mode and provides excellent efficiency at light loads. When the power demand reduces further, it enters into a skip mode to reduce the standby consumption down to a no load condition.

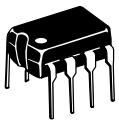
Protection features include: a timer to detect an overload or a short−circuit event, Overvoltage Protection with auto−recovery and AC input line voltage detection.

For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to reduce input power consumption below 50 mW at high line.

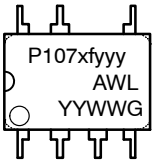
MARKING DIAGRAMS

SOT−223
ST SUFFIX
CASE 318E





PDIP−7
P SUFFIX
CASE 626A



Z	= 1 for Std product; V for Automotive
x	= Current Limit (0, 1, 2, 5, 6 or 7)
y	= Oscillator Frequency A (65 kHz), B (100 kHz), C (130 kHz)
yyy	= 065, 100, 130
f	= OFF phase in fault mode P (420 ms), B (210 ms)
A	= Assembly Location
WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 28 of this data sheet.

Features

- Built−in 700 V MOSFET with $R_{DS(on)}$ of 4.7 Ω (NCP1076/77) / 11 Ω (NCP1072/75) / 22 Ω (NCP1070/71)
- Large Creepage Distance Between High−voltage Pins
- Current−Mode Fixed Frequency Operation – 65 / 100 / 130 kHz
- Peak Current: NCP1070/72 with 250 mA, NCP1071 with 350 mA, NCP1075 with 450 mA, NCP1076 with 650 mA and NCP1077 with 800 mA
- Fixed Ramp Compensation
- Skip−Cycle Operation at Low Peak Currents Only: No Acoustic Noise!
- Dynamic Self−Supply: No Need for an Auxiliary Winding
- Internal 1 ms Soft−Start
- Auto−Recovery Output Short Circuit Protection with Timer−Based Detection
- Auto−Recovery Overvoltage Protection with Auxiliary Winding Operation
- Frequency Jittering for Better EMI Signature, Including Frequency Foldback Mode
- No Load Input Consumption < 50 mW
- Frequency Foldback to Improve Efficiency at Light Load
- Internal Temperature Shutdown
- These are Pb−Free Devices

Typical Applications

- Auxiliary / Standby Isolated Power Supplies White Goods / Smart Meter / E−Meter

PIN CONNECTIONS

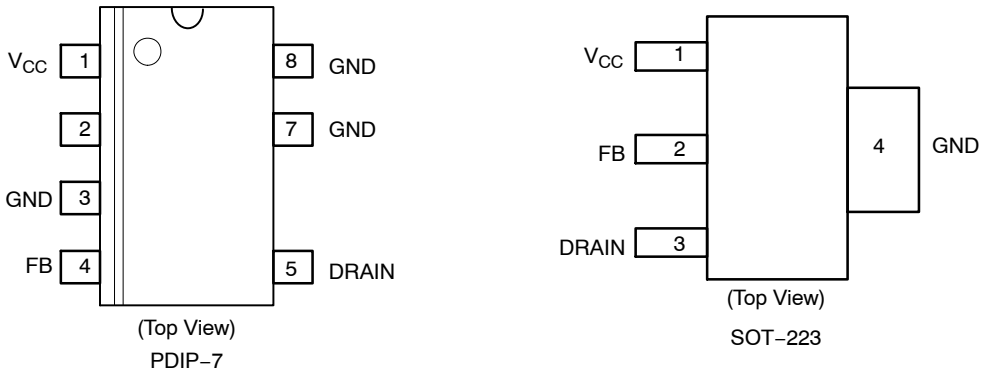


Figure 1. Pin Connections

INDICATIVE MAXIMUM OUTPUT POWER

	$R_{DS(on)}$ − I_{IPK}	230 Vac	85−265 Vac
NCP1070 / 1071	22 Ω − 350 mA	14 W	7.75 W
NCP1072 / 1075	11 Ω − 450 mA	19 W	10 W
NCP1076 / 1077	4.7 Ω − 800 mA	25 W	15 W

NOTE: Informative values only, with T_{amb} = 50°C, F_{SW} = 65 kHz, Self supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.

QUICK SELECTION TABLE

	NCP1070			NCP1071			NCP1072			NCP1075			NCP1076			NCP1077		
$R_{DS(on)}$ (Ω)	22						11						4.7					
Ipeak (mA)	250			350			250			450			650			800		
Freq (kHz)	65	100	130	65	100	130	65	100	130*	65	100	130	65	100	130	65	100	130

*130 kHz on demand only

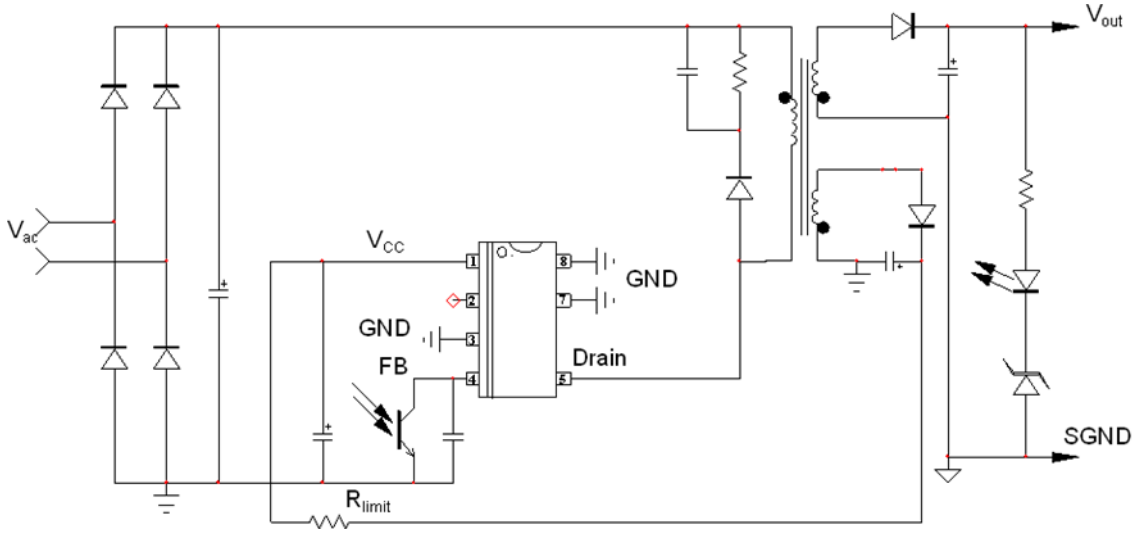


Figure 2. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin N°	Pin Name	Function	Pin Description
1	V_{CC}	Powers the internal circuitry	This pin is connected to an external capacitor. The V_{CC} includes an active shunt which serves as an auto−recovery over voltage protection.
2	NC		
3	GND	The IC Ground	
4	FB	Feedback signal input	By connecting an opto−coupler to this pin, the peak current set point is adjusted accordingly to the output power demand.
5	Drain	Drain connection	The internal drain MOSFET connection
6			This un−connected pin ensures adequate creepage distance
7	GND	The IC Ground	
8	GND	The IC Ground	

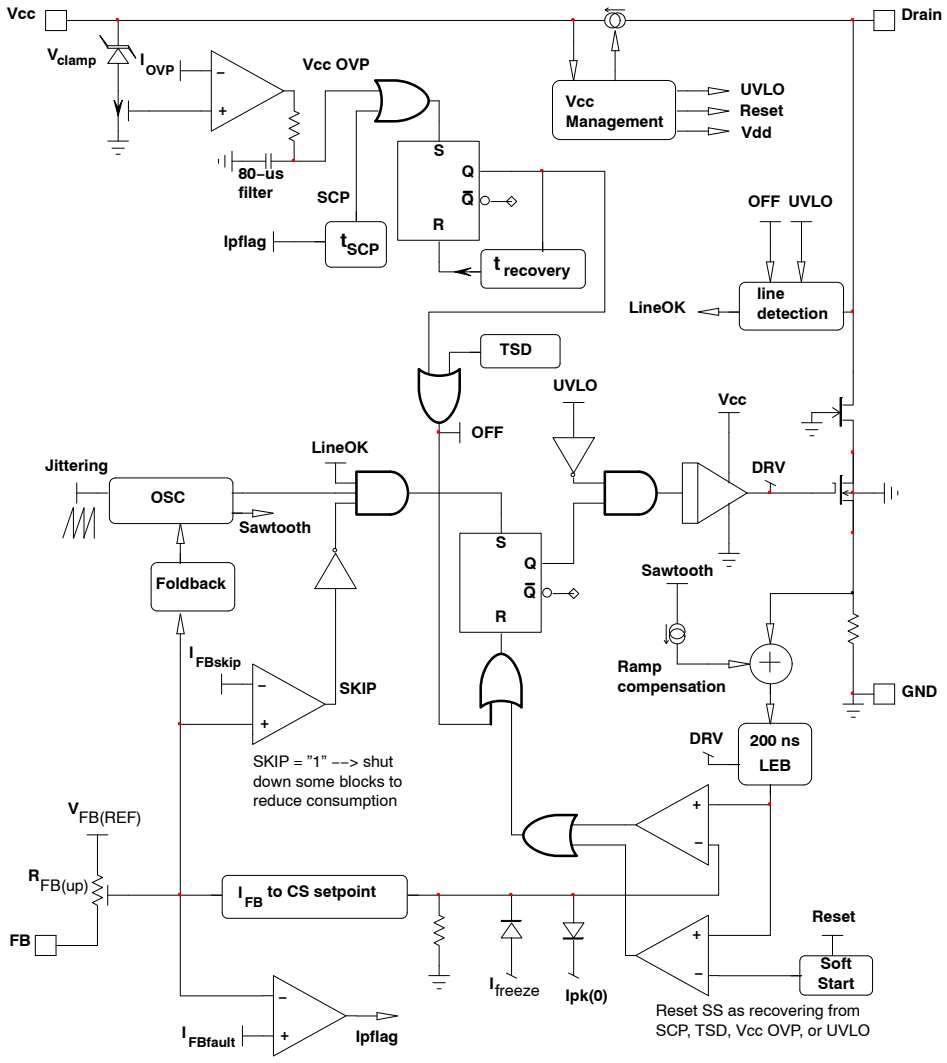


Figure 3. Simplified Internal Circuit Architecture

MAXIMUM RATINGS TABLE

Symbol	Rating		Value	Unit
V_{CC}	Power Supply Voltage on all pins, except Pin 5(Drain)		−0.3 to 10	V
BVdss	Drain voltage		−0.3 to 700	V
$I_{DS(PK)}$	Drain current peak during transformer saturation (T_J = 150°C, Note 3): NCP1070/71: NCP1072/75: NCP1076/77: Drain current peak during transformer saturation (T_J = 25°C, Note 3): NCP1070/71: NCP1072/75: NCP1076/77:		 480 870 2200 850 1500 3900	 mA mA mA mA mA mA
I_V_{CC}	Maximum Current into Pin 1 when Activating the 8.2 V Active Clamp		15	mA
$R_{\theta J-A}$	P Suffix, Case 626A	0.36 Sq. Inch	77	°C/W
	Junction−to−Air, 2.0 oz Printed Circuit Copper Clad	1.0 Sq. Inch	60	
$R_{\theta J-A}$	ST Suffix, Plastic Package Case 318E	0.36 Sq. Inch	74	°C/W
	Junction−to−Air, 2.0 oz Printed Circuit Copper Clad	1.0 Sq. Inch	55	
TJ_{MAX}	Maximum Junction Temperature		150	°C
	Storage Temperature Range		−60 to +150	°C
	ESD Capability, Human Body Model (All pins except HV)		2	kV
	ESD Capability, Machine Model		200	V
	ESD Capability, Charged Device Model		1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC JESD22−A114−F
   Machine Model Method 200 V per JEDEC JESD22−A115−A
   Charged Device Model 1000 V per JEDEC JESD22−C101E
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78
3. Maximum drain current $I_{DS(PK)}$ is obtained when the transformer saturates. It should not be mixed with short pulses that can be seen at turn on. Figure 4 below provides spike limits the device can tolerate.

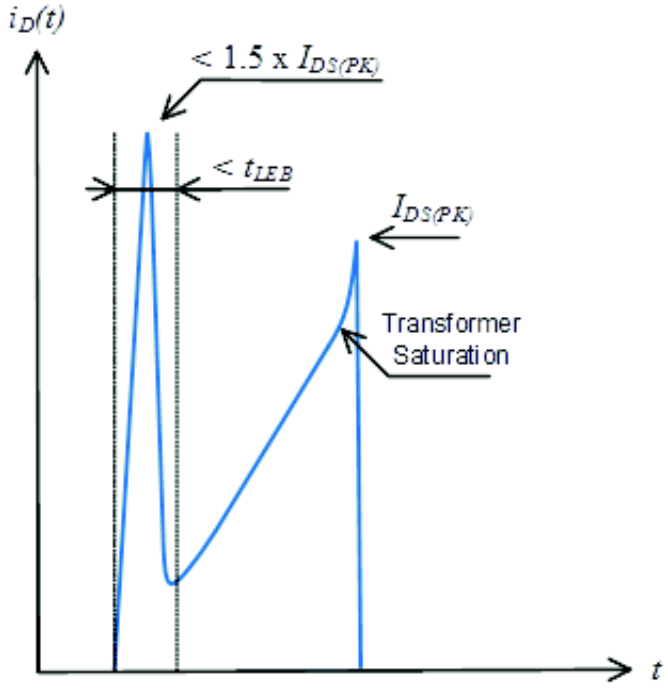


Figure 4. Spike Limits

ELECTRICAL CHARACTERISTICS

(For all NCP107X products except NCP1072P100BG: For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 8 V unless otherwise noted)
(For NCP1072P100BG: For typical values T_J = 25°C, for min/max values T_J = −55°C (Note 7) to +125°C, V_{CC} = 8 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
$V_{CC(on)}$	V_{CC} increasing level at which the switcher starts operation NCP1070/71/72/75 NCP1076/77	 1 1	 7.8 7.7	 8.2 8.1	 8.6 8.5	V
$V_{CC(min)}$	V_{CC} decreasing level at which the HV current source restarts	1	6.5	6.8	7.2	V
$V_{CC(off)}$	V_{CC} decreasing level at which the switcher stops operation (UVLO)	1	6.1	6.3	6.6	V
$V_{CC(reset)}$	V_{CC} voltage at which the internal latch is reset (guaranteed by design)	1		4		V
$V_{CC(clamp)}$	Offset voltage above $V_{CC(on)}$ at which the internal clamp activates NCP1070/71 NCP1072/75 NCP1076/77	 1 1 1	 110 130 130	 170 190 190	 300 300 300	mV
I_{CC1}	Internal IC consumption, Mosfet switching NCP1070/71/72/75 NCP1076/77	 1 1	 – –	 0.7 1.0	 1.0 1.3	mA
I_{CCskip}	Internal IC consumption, FB is 0 V (No switching on MOSFET)	1		360		μA
POWER SWITCH CIRCUIT						
$R_{DS(on)}$	Power Switch Circuit on−state resistance (Id = 50 mA) NCP1070/71 T_J = 25°C T_J = 125°C NCP1072/75 T_J = 25°C T_J = 125°C NCP1076/77 T_J = 25°C T_J = 125°C	5	 – – – – – –	 22 38 11 19 4.7 8.7	 32 55 16 24 6.9 10.75	Ω
BV_{DSS}	Power Switch Circuit & Startup breakdown voltage ($ID_{(off)}$ = 120 μA, T_J = 25°C)	5	700			V
$I_{DSS(off)}$	Power Switch & Startup breakdown voltage off−state leakage current T_J = 125°C (Vds = 700 V)	5		85		μA
 t_{on} t_{off}	Switching characteristics (R_L=50 Ω, V_{DS} set for I_{drain} = 0.7 x Ilim) Turn−on time (90% − 10%) Turn−off time (10% − 90%)	 5 5	 	 20 10	 	ns
INTERNAL START−UP CURRENT SOURCE						
I_{start1}	High−voltage current source, V = $V_{CC(on)}$ − 200 mV NCP1070/71/76/77 NCP1072/75	 5 5	 5.2 5	 9.2 9	 12.2 12	mA
I_{start2}	High−voltage current source, V_{CC} = 0 V	5		0.5		mA
V_{CCTH}	VCC Transient level for Istart1 to Istart2 toggling point	1	–	2.2	–	V
CURRENT COMPARATOR						
I_{IPK}	Maximum internal current setpoint at 50% duty cycle FB pin open, Tj = 25°C NCP1070 NCP1071 NCP1072 NCP1075 NCP1076 NCP1077		 – – – – – –	 250 350 250 450 650 800	 – – – – – –	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The final switch current is: $I_{IPK(0)}$ / (V_{in}/L_P + S_a) x V_{in}/L_P + V_{in}/L_P x t_{prop}, with S_a the built−in slope compensation, Vin the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
5. NCP1072 130 kHz on demand only.
6. Oscillator frequency is measured with disabled jittering.
7. For coldest temperature, QA sampling at −40°C in production and −55°C specification is Guaranteed by Characterization.

ELECTRICAL CHARACTERISTICS

(For all NCP107X products except NCP1072P100BG: For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 8 V unless otherwise noted)
(For NCP1072P100BG: For typical values T_J = 25°C, for min/max values T_J = −55°C (Note 7) to +125°C, V_{CC} = 8 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
CURRENT COMPARATOR						
$I_{IPK(0)}$	Maximum internal current setpoint at beginning of switching cycle FB pin open, Tj = 25°C					mA
	NCP1070		273	304	334	
	NCP1071		382	425	467	
	NCP1072		254	282	310	
	NCP1075		467	508	549	
	NCP1076		689	765	841	
	NCP1077		846	940	1034	
I_{IPKSW}	Final switch current with a primary slope of 200 mA/μs, F_{SW} =65 kHz (Note 4)					mA
	NCP1070		–	314	–	
	NCP1071		–	427	–	
	NCP1072		–	296	–	
	NCP1075		–	510	–	
	NCP1076		–	732	–	
	NCP1077		–	881	–	
I_{IPKSW}	Final switch current with a primary slope of 200 mA/μs, F_{SW} =100 kHz (Note 4)					mA
	NCP1070		–	309	–	
	NCP1071		–	415	–	
	NCP1072		–	293	–	
	NCP1075		–	500	–	
	NCP1076		–	706	–	
	NCP1077		–	845	–	
I_{IPKSW}	Final switch current with a primary slope of 200 mA/μs, F_{SW} =130 kHz					mA
	NCP1070		–	303	–	
	NCP1071		–	407	–	
	NCP1072 (Note 5)		–	291	–	
	NCP1075		–	493	–	
	NCP1076		–	684	–	
	NCP1077		–	814	–	
T_{SS}	Soft−start duration (guaranteed by design)	–	–	1	–	ms
T_{LEB}	Leading Edge Blanking Duration	–	–	200	–	ns
T_{prop}	Propagation delay from current detection to drain OFF state	–	–	100	–	ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillation frequency, 65 kHz version, Tj = 25°C (Note 6)	–	59	65	71	kHz
f_{OSC}	Oscillation frequency, 100 kHz version, Tj = 25°C (Note 6)	–	90	100	110	kHz
f_{OSC}	Oscillation frequency, 130 kHz version, Tj = 25°C (Note 5 et 6)	–	117	130	143	kHz
f_{jitter}	Frequency jittering in percentage of f_{OSC}	–	–	±6	–	%
f_{swing}	Jittering swing frequency	–	–	300	–	Hz
D_{max}	Maximum duty−cycle					%
	NCP1070/71/72/75 except NCP1072P100BG	–	62	68	72	
	NCP1076/77/72B & NCP1072P100BG	–	65	69	73	
FEEDBACK SECTION						
$I_{FBfault}$	FB current for which Fault is detected	4		−35		μA
$I_{FB100\%}$	FB current for which internal current set−point is 100% ($I_{IPK(0)}$)	4		−44		μA
$I_{FBFreeze}$	FB current for which internal current set−point is I_{Freeze}	4	–	−90	–	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The final switch current is: $I_{IPK(0)}$ / ($V_{in}/L_P + S_a$) x V_{in}/L_P + V_{in}/L_P x t_{prop}, with S_a the built−in slope compensation, Vin the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
5. NCP1072 130 kHz on demand only.
6. Oscillator frequency is measured with disabled jittering.
7. For coldest temperature, QA sampling at −40°C in production and −55°C specification is Guaranteed by Characterization.

ELECTRICAL CHARACTERISTICS

(For all NCP107X products except NCP1072P100BG: For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 8 V unless otherwise noted)
(For NCP1072P100BG: For typical values T_J = 25°C, for min/max values T_J = −55°C (Note 7) to +125°C, V_{CC} = 8 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
FEEDBACK SECTION						
$V_{FB(REF)}$	Equivalent pull−up voltage in linear regulation range (Guaranteed by design)	4		3.3		V
$R_{FB(up)}$	Equivalent feedback resistor in linear regulation range (Guaranteed by design)	4		19.5		kΩ
FREQUENCY FOLDBACK & SKIP						
I_{FBfold}	Start of frequency foldback feedback level	4	–	−68	–	μA
$I_{FBfold(end)}$	End of frequency foldback feedback level, $F_{sw} = F_{min}$	4	–	−100	–	μA
F_{min}	The frequency below which skip−cycle occurs	–	21	25	29	kHz
I_{FBskip}	The feedback level to enter skip mode	4	–	−120	–	μA
I_{Freeze}	Internal minimum current setpoint ($I_{FB} = I_{FBFreeze}$)					mA
	NCP1070	–	–	88	–	
	NCP1071		–	123	–	
	NCP1072		–	88	–	
	NCP1075		–	168	–	
	NCP1076		–	228	–	
	NCP1077		–	280	–	
RAMP COMPENSATION						
$S_{a(65)}$	The internal ramp compensation @ 65 kHz					mA/μs
	NCP1070	–	–	7	–	
	NCP1071		–	10	–	
	NCP1072		–	4.2	–	
	NCP1075		–	7.5	–	
	NCP1076		–	15	–	
	NCP1077		–	18	–	
$S_{a(100)}$	The internal ramp compensation @ 100 kHz					mA/μs
	NCP1070	–	–	11	–	
	NCP1071		–	15	–	
	NCP1072		–	6.5	–	
	NCP1075		–	11.5	–	
	NCP1076		–	23	–	
	NCP1077		–	28	–	
$S_{a(130)}$	The internal ramp compensation @ 130 kHz					
	NCP1070	–	–	14	–	
	NCP1071		–	20	–	
	NCP1072 (Note 5)		–	8.4	–	
	NCP1075		–	15	–	
	NCP1076		–	30	–	
	NCP1077		–	36	–	
PROTECTIONS						
t_{SCP}	Fault validation further to error flag assertion	–	40	53	–	ms
$t_{recovery}$	OFF phase in fault mode					ms
	NCP1070/1/2/5/6/7	–	–	420	–	
	NCP1072P100BG	–	–	210	–	
I_{OVP}	V_{CC} clamp current at which the switcher stops pulsing					mA
	NCP1070/71	1	6.2	8.7	11.2	
	NCP1072/75/76/77		6	8.5	11	
t_{OVP}	The filter of V_{CC} OVP comparator	–	–	80	–	μs

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4. The final switch current is: $I_{IPK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$, with S_a the built−in slope compensation, Vin the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
5. NCP1072 130 kHz on demand only.
6. Oscillator frequency is measured with disabled jittering.
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(For NCP1072P100BG: For typical values T_J = 25°C, for min/max values T_J = −55°C (Note 7) to +125°C, V_{CC} = 8 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
PROTECTIONS						
$V_{HV(EN)}$	The drain pin voltage above which allows MOSFET operate, which is detected after TSD, UVLO, SCP, or V_{CC} OVP mode.	5	72	91	110	V
TEMPERATURE MANAGEMENT						
TSD	Temperature shutdown (Guaranteed by design)	–	150			°C
	Hysteresis in shutdown (Guaranteed by design)	–		50		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The final switch current is: $I_{IPK(0)}$ / (V_{in}/L_P + S_a) x V_{in}/L_P + V_{in}/L_P x t_{prop}, with S_a the built−in slope compensation, Vin the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
5. NCP1072 130 kHz on demand only.
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TYPICAL CHARACTERISTICS

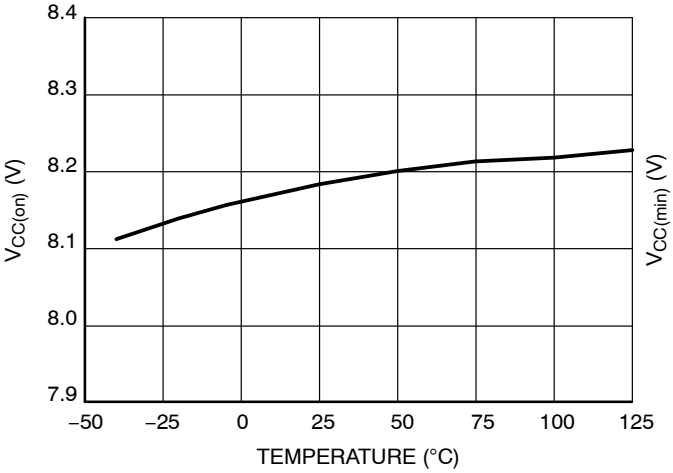


Figure 5. $V_{CC(on)}$ vs. Temperature

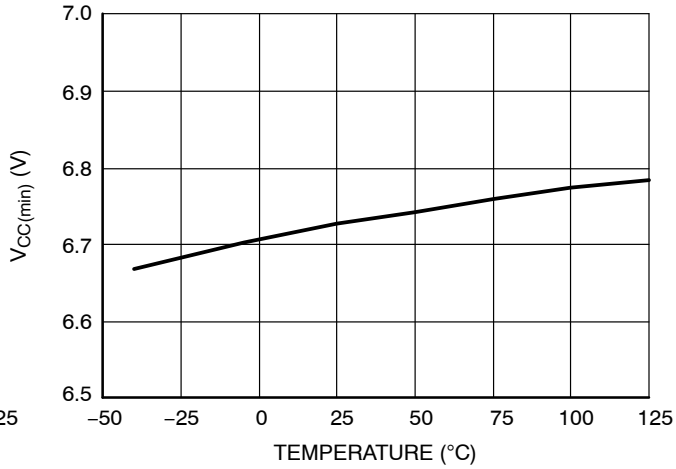


Figure 6. $V_{CC(min)}$ vs. Temperature

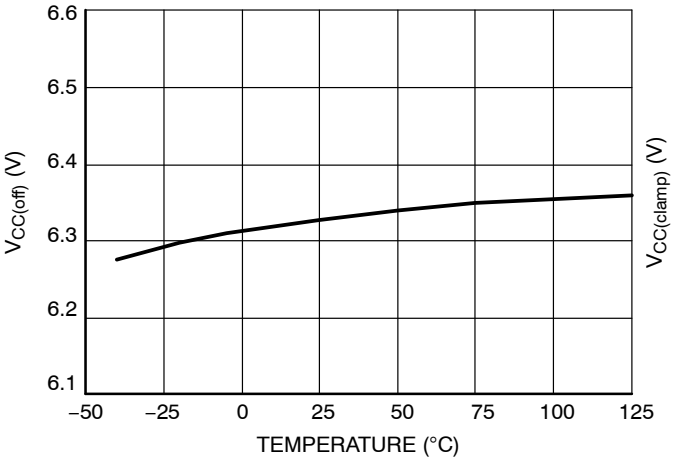


Figure 7. $V_{CC(off)}$ vs. Temperature

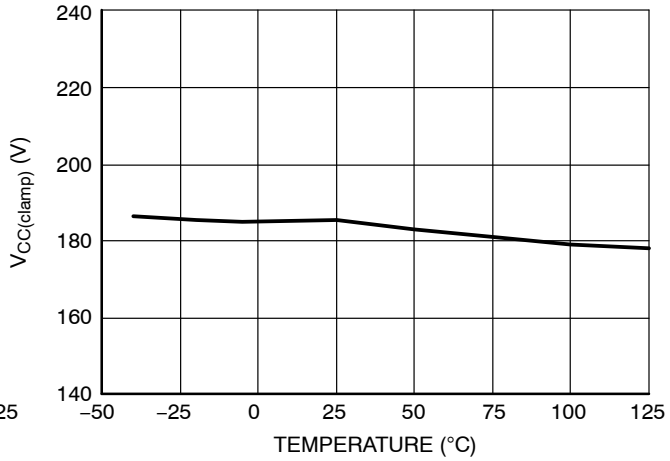


Figure 8. $V_{CC(clamp)}$ vs. Temperature

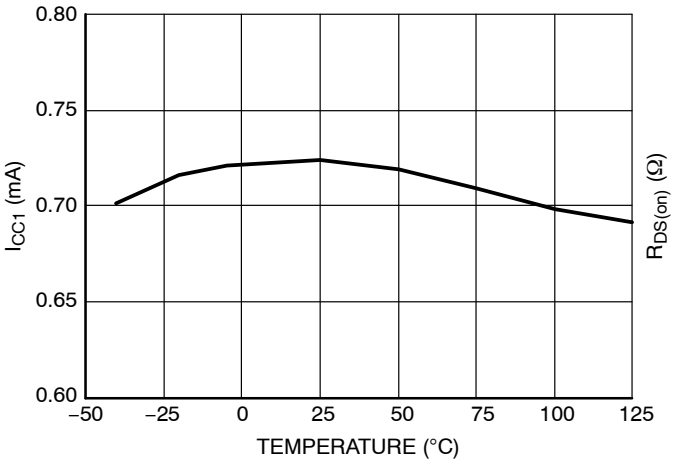


Figure 9. I_{CC1} vs. Temperature

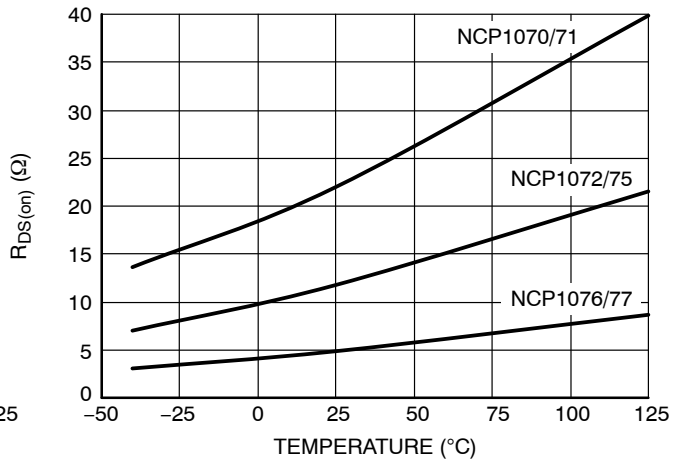


Figure 10. $R_{DS(on)}$ vs. Temperature

TYPICAL CHARACTERISTICS

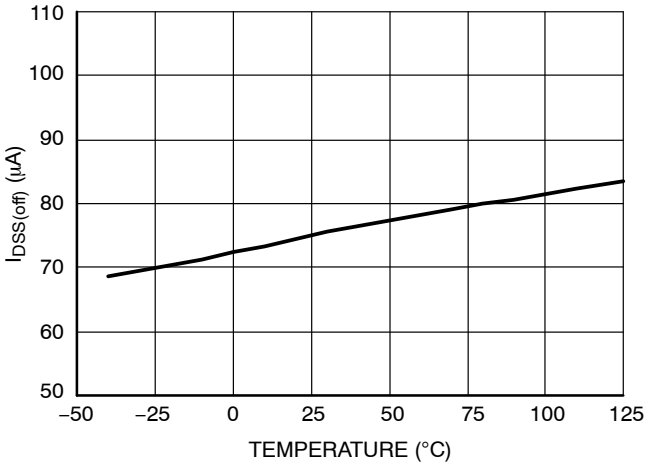


Figure 11. $I_{DSS(off)}$ vs. Temperature

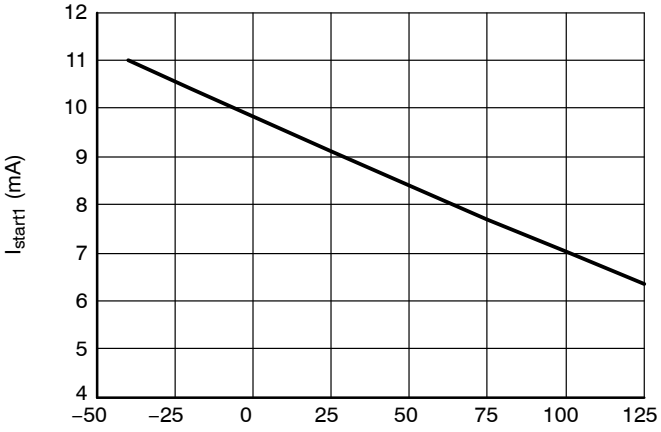


Figure 12. I_{start1} vs. Temperature

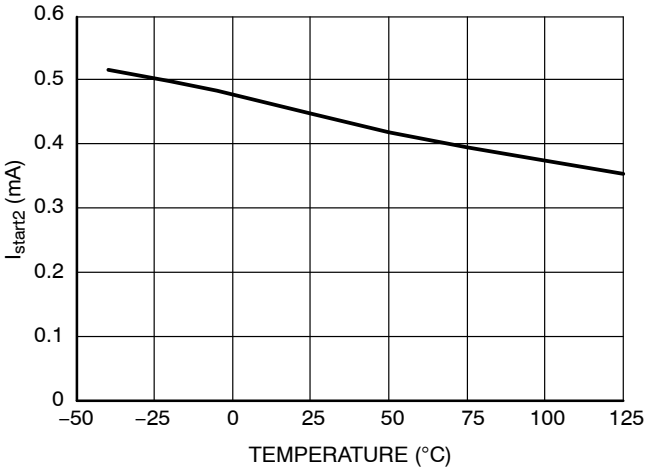


Figure 13. I_{start2} vs. Temperature

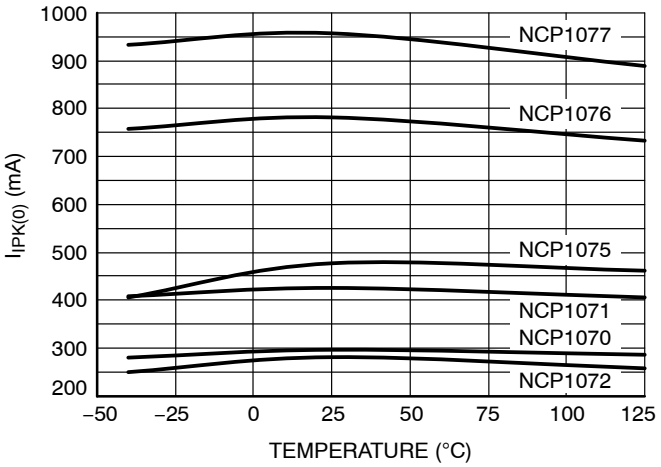


Figure 14. $I_{IPK(0)}$ vs. Temperature

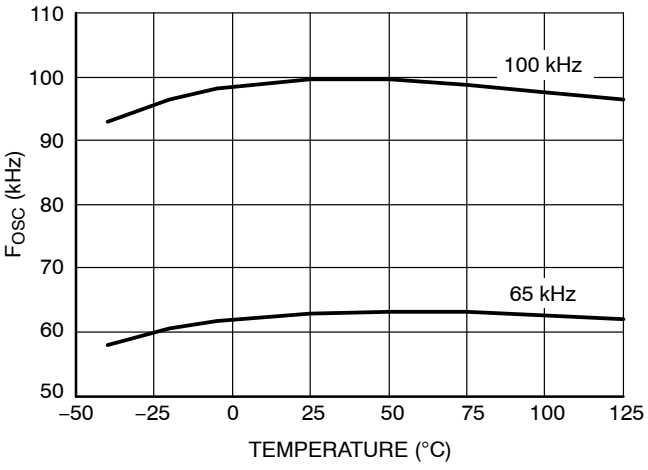


Figure 15. F_{OSC} vs. Temperature

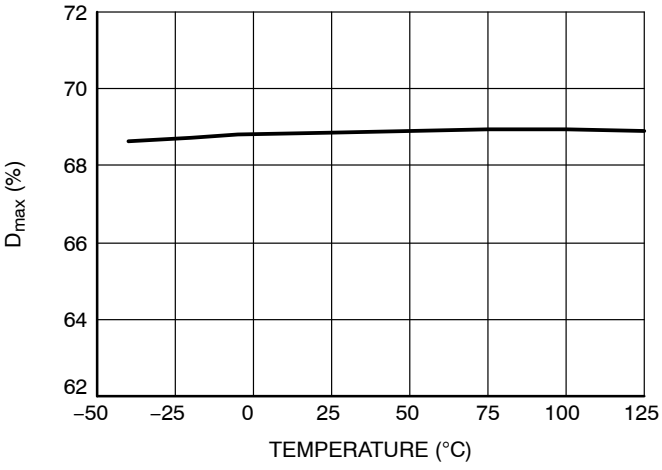


Figure 16. $D_{(max)}$ vs. Temperature

TYPICAL CHARACTERISTICS

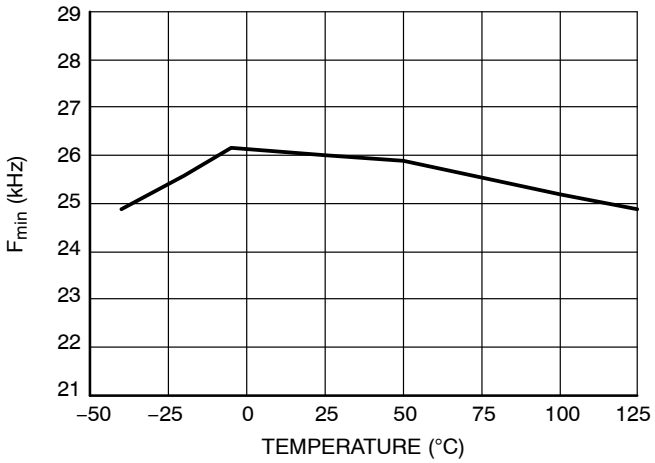


Figure 17. F_{min} vs. Temperature

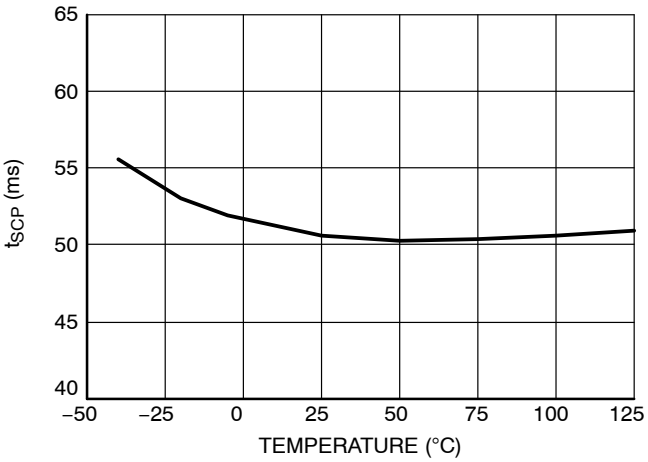


Figure 18. t_{SCP} vs. Temperature

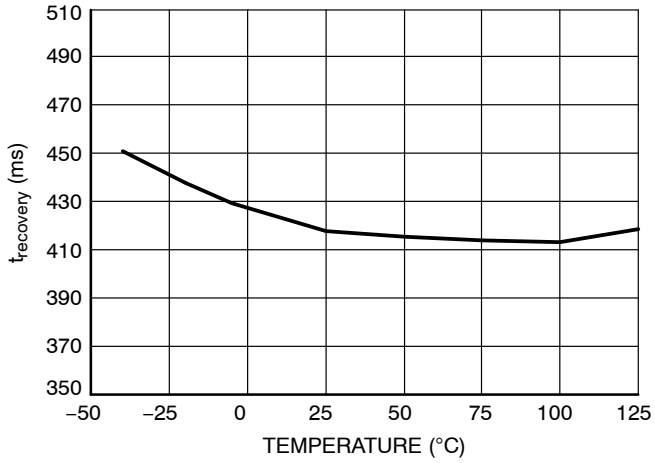


Figure 19. $t_{recovery}$ vs. Temperature

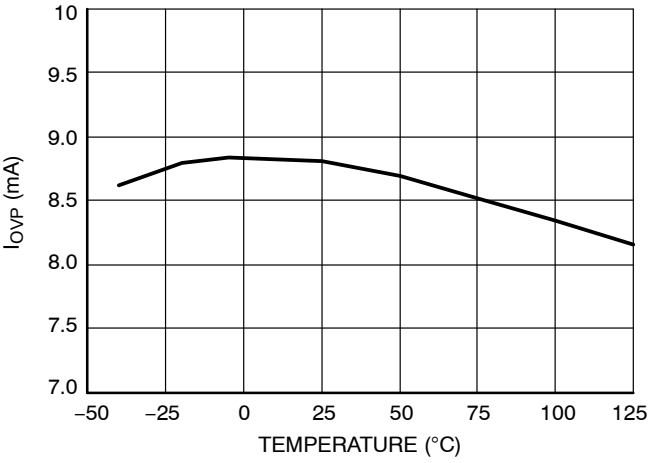


Figure 20. I_{OVP} vs. Temperature

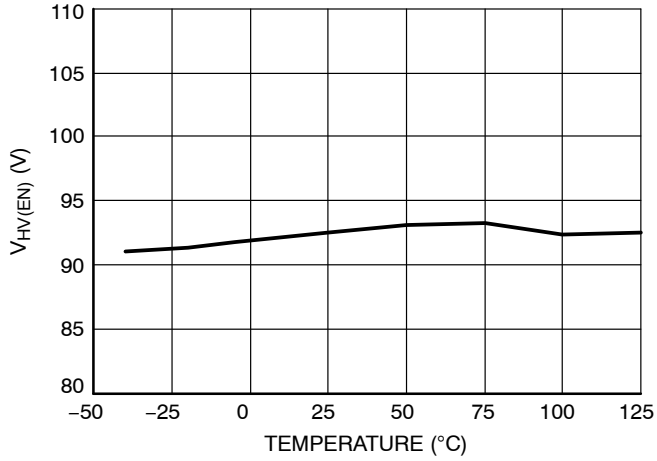


Figure 21. $V_{HV(EN)}$ vs. Temperature

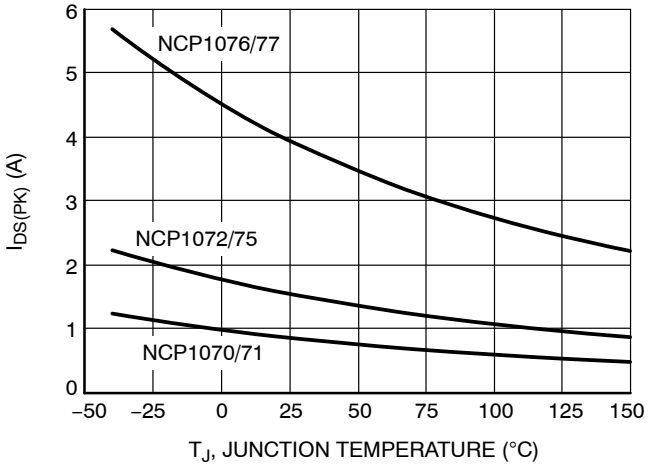


Figure 22. Drain Current Peak during Transformer Saturation vs. Junction Temperature

TYPICAL CHARACTERISTICS

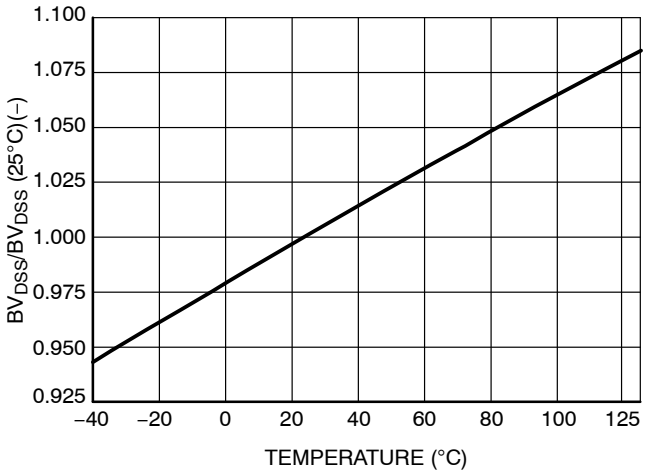


Figure 23. Breakdown Voltage vs. Temperature

APPLICATION INFORMATION

Introduction

The NCP107x offers a complete current−mode control solution. The component integrates everything needed to build a rugged and low−cost Switch−Mode Power Supply (SMPS) featuring low standby power. The Quick Selection Table on page 2 details the differences between references, mainly peak current setpoints and operating frequency.

- Current−mode operation: the controller uses current−mode control architecture.
- 700 V Power MOSFET: Due to **onsemi** Very High Voltage Integrated Circuit technology, the circuit hosts a high − voltage power MOSFET featuring a 22/11/4.7 Ω $R_{DS(on)}$ − T_J = 25°C. This value lets the designer build a power supply up to respectively 7.75 W, 10 W and 15 W operated on universal mains. An internal current source delivers the startup current, necessary to crank the power supply.
- Dynamic Self−Supply: Due to the internal high voltage current source, this device could be used in the application without the auxiliary winding to provide supply voltage.
- Short circuit protection: by permanently monitoring the feedback line activity, the IC is able to detect the presence of a short−circuit, immediately reducing the output power for a total system protection. A t_{SCP} timer is started as soon as the feedback current is below threshold, $I_{FB(fault)}$, which indicates the maximum peak current. If at the end of this timer the fault is still present, then the device enters a safe, auto−recovery burst mode, affected by a fixed timer recurrence, $t_{recovery}$. Once the short has disappeared, the controller resumes and goes back to normal operation.
- Built−in V_{CC} Over Voltage Protection: when the auxiliary winding is used to bias the V_{CC} pin (no DSS), an internal active clamp connected between V_{CC} and ground limits the supply dynamics to $V_{CC(clamp)}$. In case the current injected in this clamp exceeds a level of 6.0 mA (minimum), the controller immediately stops switching and waits a full timer period ($t_{recovery}$) before attempting to restart. If the fault is gone, the controller resumes operation. If the fault is still there, e.g. a broken opto−coupler, the controller protects the load through a safe burst mode.
- Line detection: An internal comparator monitors the drain voltage as recovering from one of the following situations:
  - Short Circuit Protection,
  - V_{CC} OVP is confirmed,
  - UVLO
  - TSD

  If the drain voltage is lower than the internal threshold ($V_{HV(EN)}$), the internal power switch is inhibited. This avoids operating at too low ac input. This is also called brown−in function in some fields.
- Frequency jittering: an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering remains active in frequency foldback mode.
- Soft−Start: a 1 ms soft−start ensures a smooth startup sequence, reducing output overshoots.
- Frequency foldback capability: a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback current information and when it reaches a level of I_{FBfold}, the oscillator then starts to reduce its switching frequency as the feedback current continues to increase (the power demand continues to reduce). It can go down to 25 kHz (typical) reached for a feedback level of $I_{FBfold(end)}$ (100 μA roughly). At this point, if the power continues to drop, the controller enters classical skip−cycle mode.
- Skip: if SMPS naturally exhibits a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un−needed switching cycles, the NCP107x drastically reduces the power wasted during light load conditions.

APPLICATION INFORMATION

Startup Sequence

When the power supply is first powered from the mains outlet, the internal current source is biased and charges up the V_{CC} capacitor from the drain pin. Once the voltage on this V_{CC} capacitor reaches the $V_{CC(on)}$ level, the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET if the bulk voltage is above $V_{HV(EN)}$ level. Figure 24 details the simplified internal circuitry.

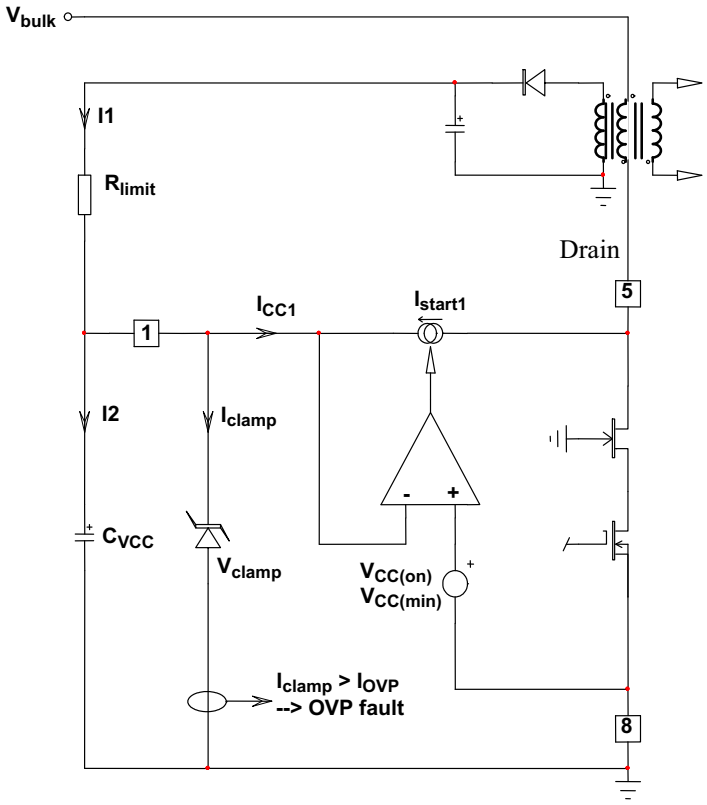


Figure 24. The Internal Arrangement of the Start−up Circuitry

Being loaded by the circuit consumption, the voltage on the V_{CC} capacitor goes down. When V_{CC} is below $V_{CC(min)}$ level, it activates the internal current source to bring V_{CC} toward $V_{CC(on)}$ level and stops again: a cycle takes place whose low frequency depends on the V_{CC} capacitor and the IC consumption. A 1.4 V ripple takes place on the V_{CC} pin whose average value equals $(V_{CC(on)} + V_{CC(min)})/2$. Figure 25 portrays a typical operation of the DSS.

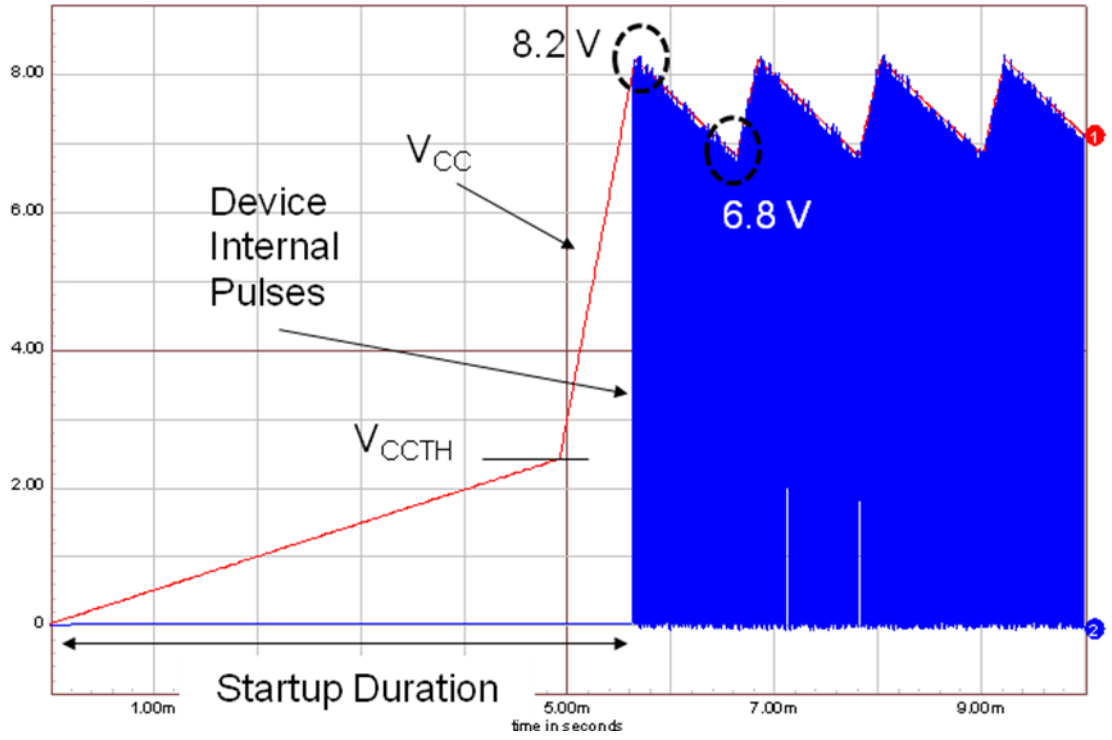


Figure 25. The Charge/Discharge Cycle Over a 1 μF V_{CC} Capacitor

As one can see, even if there is auxiliary winding to provide energy for V_{CC}, it happens that the device is still biased by DSS during start−up time or some fault mode when the voltage on auxiliary winding is not ready yet. The V_{CC} capacitor shall be dimensioned to avoid V_{CC} crosses $V_{CC(off)}$ level, which stops operation. The ΔV between $V_{CC(min)}$ and $V_{CC(off)}$ is 0.4 V. There is no current source to charge V_{CC} capacitor when driver is on, i.e. drain voltage is close to zero. Hence the V_{CC} capacitor can be calculated using

$$C_{VCC} \geq \frac{I_{CC1} D_{max}}{f_{OSC} \cdot \Delta V} \qquad \text{(eq. 1)}$$

Take the NCP1072 65 kHz device as an example. C_{VCC} should be above

$$\frac{0.8m \cdot 72\%}{59\ kHz \cdot 0.4}$$

A margin that covers the temperature drift and the voltage drop due to switching inside FET should be considered, and thus a capacitor above 0.1 μF is appropriate.

The V_{CC} capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see on Figure 24, an internal active zener diode, protects the switcher against lethal V_{CC} runaways. This situation can occur if the feedback loop optocoupler fails, for instance, and you would like to protect the converter against an over voltage event. In that case, the internal current increase incurred by the V_{CC} rapid growth triggers the over voltage protection (OVP) circuit and immediately stops the output pulses for $t_{recovery}$ duration (420 ms typically). Then a new start−up attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

Fault Condition – Short−Circuit on V_{CC}

In some fault situations, a short−circuit can purposely occur between V_{CC} and GND. In high line conditions (V_{HV} = 370 V_{DC}) the current delivered by the startup device will seriously increase the junction temperature. For instance, since I_{start1} equals 5 mA (the min corresponds to the highest T_j), the device would dissipate 370 x 5 m = 1.85 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, I_{start1} and I_{start2}. At power−up, as long as V_{CC} is below a 2.4 V level, the source delivers I_{start2} (around 500 μA typical), then, when V_{CC} reaches 2.4 V, the source smoothly transitions to I_{start1} and delivers its nominal value. As a result, in case of short−circuit between V_{CC} and GND, the power dissipation will drop to 370 x 500u = 185 mW. Figure 25 portrays this particular behavior.

The first startup period is calculated by the formula C x V = I x t, which implies a 1μ x 2.4 / 500u = 4.8 ms startup time for the first sequence. The second sequence is obtained by toggling the source to 8 mA with a delta V of $V_{CC(on)}$ − V_{CCTH} = 8.2 – 2.4 = 5.8 V, which finally leads to a second startup time of 1μ x 5.8 / 8m = 0.725 ms. The total startup time becomes 4.8m + 0.725m = 5.525 ms. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

Fault Condition – Output Short−Circuit

As soon as V_{CC} reaches $V_{CC(on)}$, drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the V_{CC} pin as the output voltage rises. During the start−sequence, the controller smoothly ramps up the peak drain current to maximum setting, i.e. I_{IPK}, which is reached after a typical period of 1 ms. When the output voltage is not regulated, the current coming through FB pin is below $I_{FBfault}$ level (35 μA typically), which is not only during the startup period but also anytime an overload occurs, an internal error flag is asserted, Ipflag, indicating that the system has reached its maximum current limit set point. The assertion of this flag triggers a fault counter t_{SCP} (53 ms typically). If at counter completion, Ipflag remains asserted, all driving pulses are stopped and the part stays off in $t_{recovery}$ duration (about 420 ms). A new attempt to re−start occurs and will last 53 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty−cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 26 depicts this particular mode:

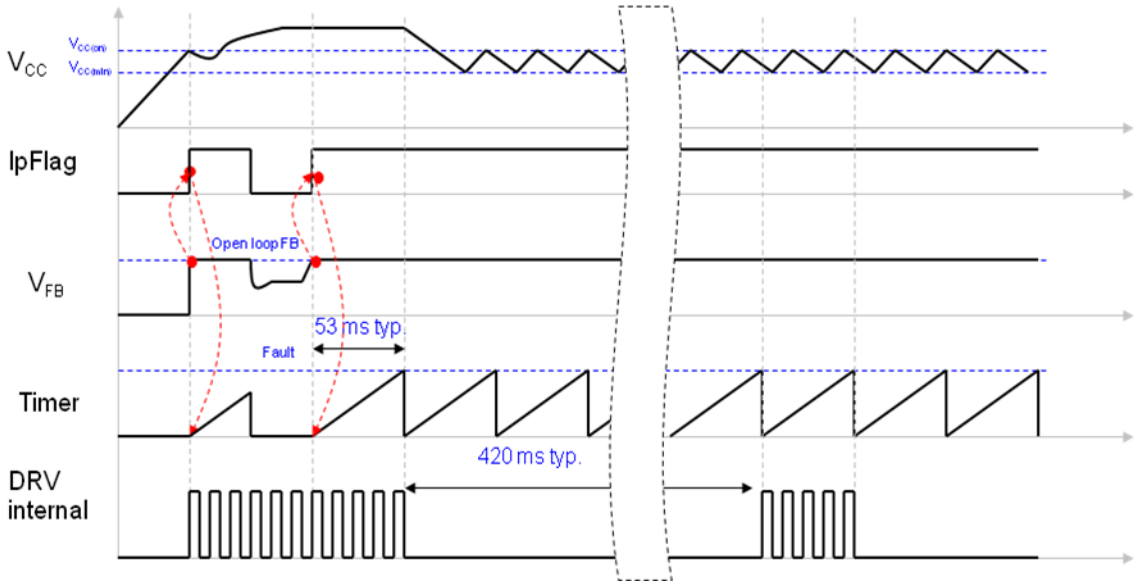


Figure 26. In Case of Short−Circuit or Overload, the NCP107X Protects Itself and the Power Supply Via a Low Frequency Burst Mode. The V_{CC} is Maintained by the Current Source and Self−supplies the Controller.

Auto−Recovery Over Voltage Protection

The particular NCP107X arrangement offers a simple way to prevent output voltage runaway when the optocoupler fails. As Figure 27 shows, an active zener diode monitors and protects the V_{CC} pin. Below its equivalent breakdown voltage, that is to say 8.4 V typical, no current flows in it. If the auxiliary V_{CC} pushes too much current inside the zener, then the controller considers an OVP situation and stops the internal drivers. When an OVP occurs, all switching pulses are permanently disabled. After $t_{recovery}$ delay, it resumes the internal drivers. If the failure symptom still exists, e.g. feedback opto−coupler fails, the device keeps the auto−recovery OVP mode.

Figure 27 shows that the insertion of a resistor (R_{limit}) between the auxiliary dc level and the V_{CC} pin is mandatory a) not to damage the internal 8.4 V zener diode during an overshoot for instance (absolute maximum current is 15 mA) b) to implement the fail−safe optocoupler protection (OVP) as offered by the active clamp. Please note that there cannot be bad interaction between the clamping voltage of the internal zener and $V_{CC(on)}$ since this clamping voltage is actually built on top of $V_{CC(on)}$ with a fixed amount of offset (200 mV typical). R_{limit} should be carefully selected to avoid triggering the OVP as we discussed, but also to avoid disturbing the V_{CC} in low / light load conditions. The below lines detail how to evaluate the R_{limit} value...

Self−supplying controllers in extremely low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (V_{nom}), this voltage can drop below 10 V (V_{stby}) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re−fueling rate of the V_{CC} capacitor is not enough to keep a proper auxiliary voltage. Figure 28 portrays a typical scope shot of a SMPS entering deep standby (output un−loaded). Thus, care must be taken when calculating R_{limit} 1) to not trigger the V_{CC} over current latch (by injecting 6 mA into the active clamp – always use the minimum value for worse case design) in normal operation but 2) not to drop too much voltage over R_{limit} when entering standby. Otherwise, the converter will enter dynamic self supply mode (DSS mode), which increases the power dissipation. Based on these recommendations, we are able to bound R_{limit} between two equations:

$$\frac{V_{nom} - V_{CC(clamp)}}{I_{trip}} \le R_{limit} \le \frac{V_{stby} - V_{CC(min)}}{I_{CCskip}} \quad \text{(eq. 2)}$$

Where:
V_{nom} is the auxiliary voltage at nominal load
V_{stby} is the auxiliary voltage when standby is entered
I_{trip} is the current corresponding to the nominal operation. It thus must be selected to avoid false tripping in overshoot conditions. Always use the minimum of the specification for a robust design, i.e. $I_{trip} < I_{OVP}$.
I_{CCskip} is the controller consumption during skip mode. This number decreases compared to normal operation since the part in standby does almost not switch. It is around 0.36 mA for the NCP1072 65 kHz version.
$V_{CC(min)}$ is the level above which the auxiliary voltage must be maintained to keep the controller away from the dynamic self supply mode (DSS mode), which is not a problem in itself if low standby power does not matter.

If a further improvement on standby efficiency is concerned, it is good to obtain V_{CC} around 8 V at no load condition in order not to re−activate the internal clamp circuit.

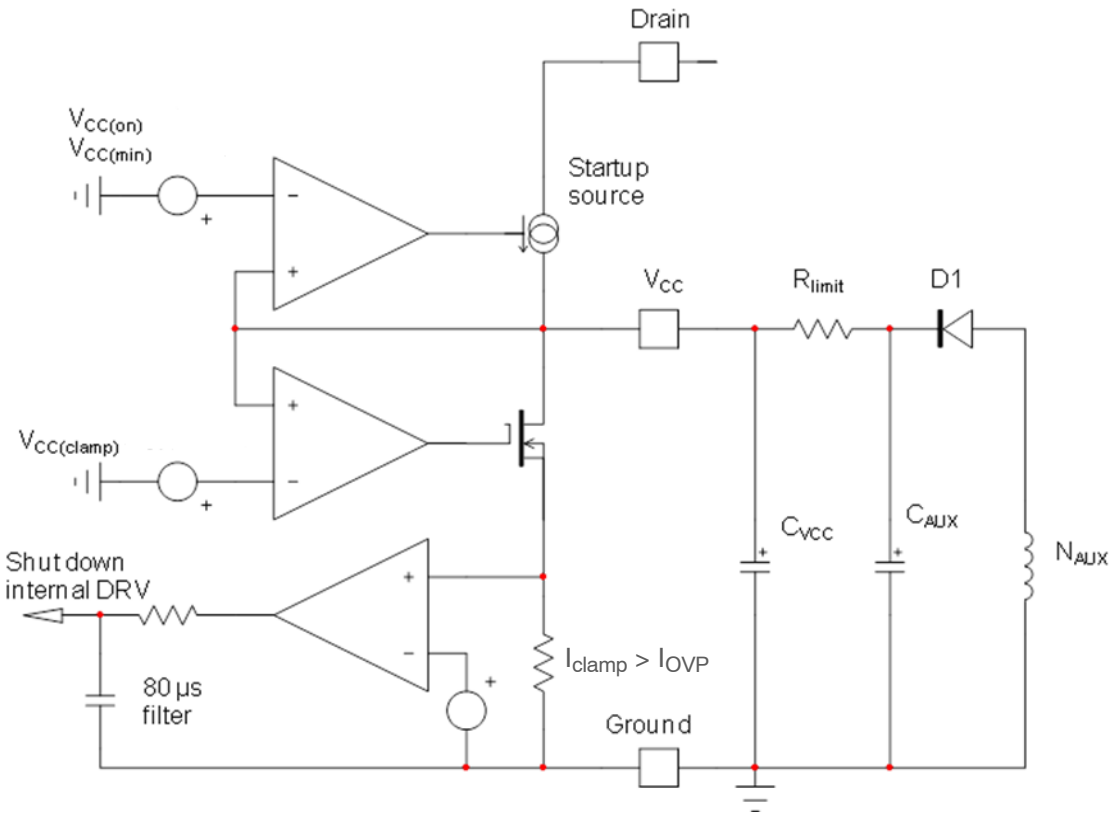


Figure 27. A More Detailed View of the NCP107x Offers Better Insight on How to Properly Wire an Auxiliary Winding

Since R_{limit} shall not bother the controller in standby, e.g. keep V_{CC} to above $V_{CC(min)}$ (7.2 V maximum), we purposely select a V_{nom} well above this value. As explained before, experience shows that a 40% decrease can be seen on auxiliary windings from nominal operation down to standby mode. Let's select a nominal auxiliary winding of 13 V to offer sufficient margin regarding 7.2 V when in standby (R_{limit} also drops voltage in standby...). Plugging the values in Equation 2 gives the limits within which R_{limit} shall be selected:

$$\frac{13 - 8.4}{6m} \le R_{limit} \le \frac{8 - 7.2}{0.36m}$$

that is to say: 0.77 kΩ < *Rlimit* < 2.2 kΩ.

If we design a 65 kHz power supply delivering 12V, then the ratio between auxiliary and power must be: 13 / 12 = 1.08. The OVP latch will activate when the clamp current exceeds 6 mA. This will occur when Vauxiliary grows−up to:

1. 8.4 + 0.77k x (6m + 0.8m) ≈ 13.6 V for the first boundary (R_{limit} = 0.77 kΩ)
2. 8.4 + 2.2k x (6m +0.8m) ≈ 23.4 V for the second boundary (R_{limit} = 2.2 kΩ)

Due to a 1.08 ratio between the auxiliary V_{CC} and the power winding, the OVP will be seen as a lower overshoot on the real output:

1. 13.6 / 1.08 ≈ 12.6 V
2. 23.4 / 1.08 ≈ 21.7 V

As one can see, tweaking the R_{limit} value will allow the selection of a given overvoltage output level. Theoretically predicting the auxiliary drop from nominal to standby is an

almost impossible exercise since many parameters are involved, including the converter time constants. Fine tuning of R_{limit} thus requires a few iterations and experiments on a breadboard to check the auxiliary voltage variations but also the output voltage excursion in fault. Once properly adjusted, the fail−safe protection will preclude any lethal voltage runaways in case a problem would occur in the feedback loop.

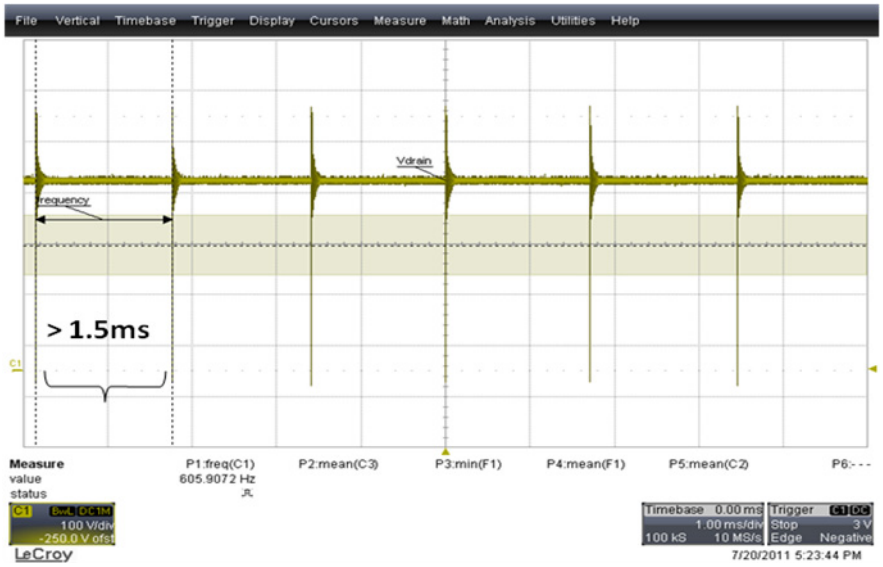


Figure 28. The Burst Frequency Becomes so Low That it is Difficult to Keep an Adequate Level on the Auxiliary V_{CC}...

Figure 29 describes the main signal variations when the part operates in auto−recovery OVP:

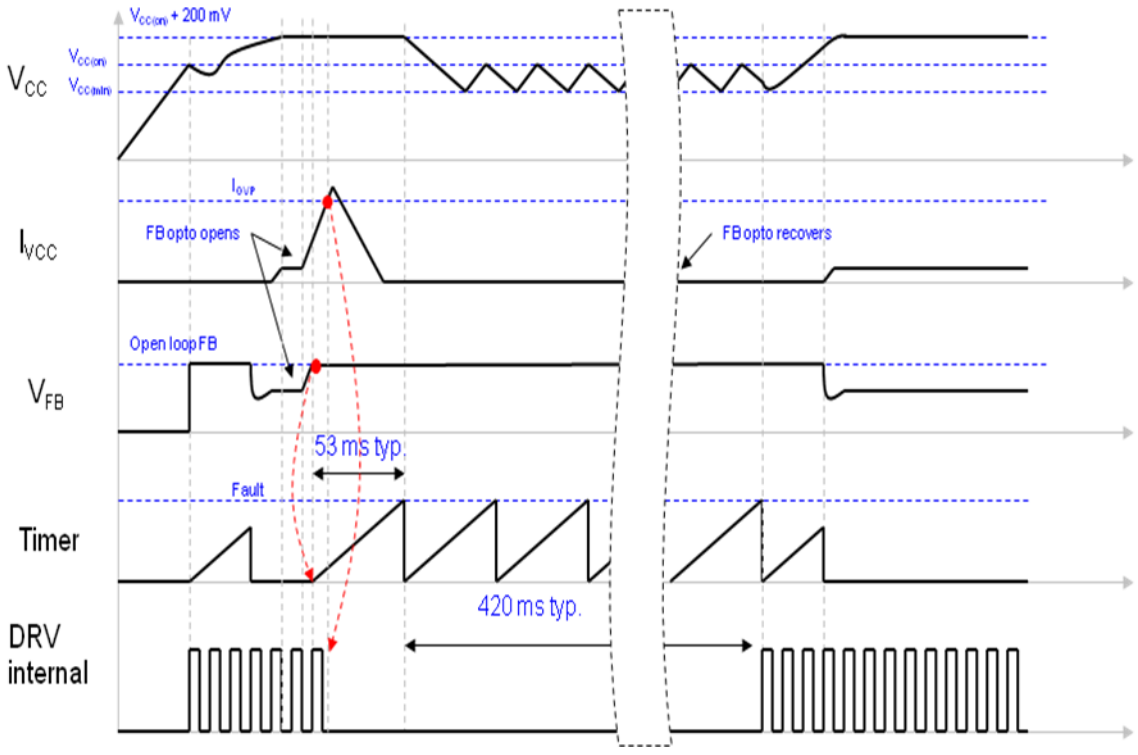


Figure 29. If the V_{CC} Current Exceeds a Certain Threshold, an Auto−Recovery Protection is Activated

Improving the precision in auto−recovery OVP

Given the OVP variations the internal trip current dispersion incur, it is sometimes more interesting to explore a different solution, improving the situation to the cost of a minimal amount of surrounding elements. Figure 30 shows that adding a simple zener diode on top of the limiting resistor, offers a better precision since what matters now is the internal $V_{CC(on)}$ breakdown plus the zener voltage. A resistor in series with the zener diodes keeps the maximum current in the V_{CC} pin below the maximum rating of 15 mA just before trip the OVP.

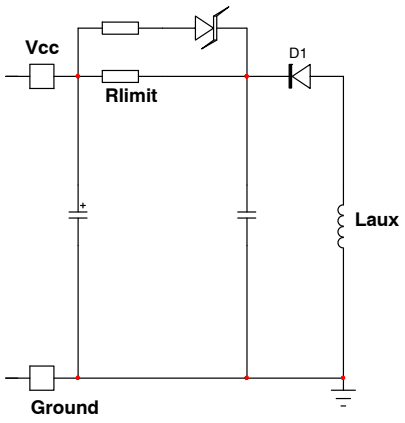


Figure 30. A Simple Zener Diode Added in Parallel

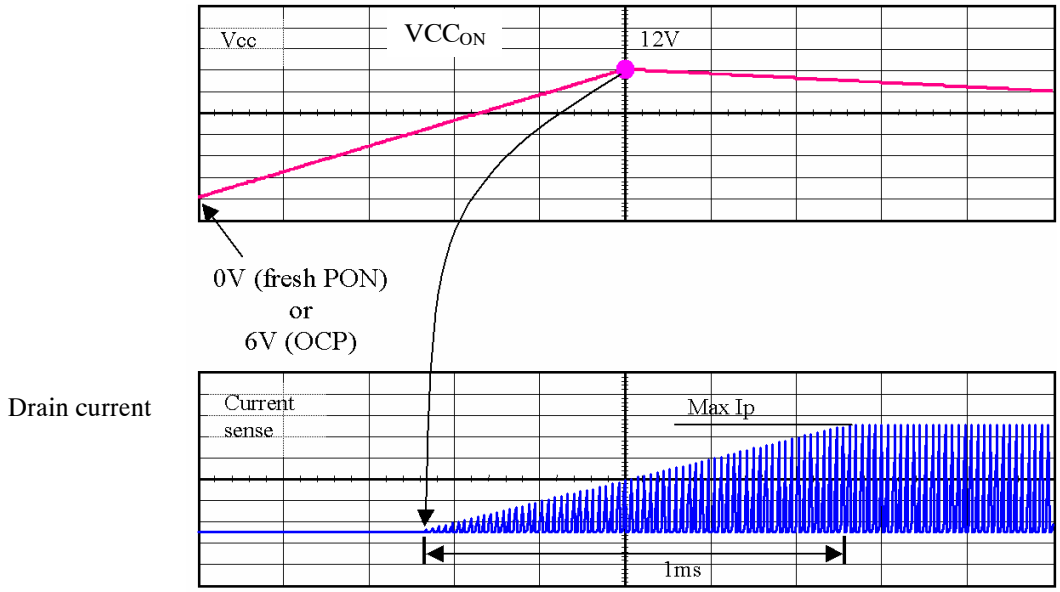


Figure 31. The 1 ms soft−start sequence

Soft−Start

The NCP107X features a 1 ms soft−start which reduces the power−on stress but also contributes to lower the output overshoot. Figure 31 shows a typical operating waveform. The NCP107X features a novel patented structure which offers a better soft−start ramp, almost ignoring the start−up pedestal inherent to traditional current−mode supplies:

Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP107X offers a ±6% deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 32 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

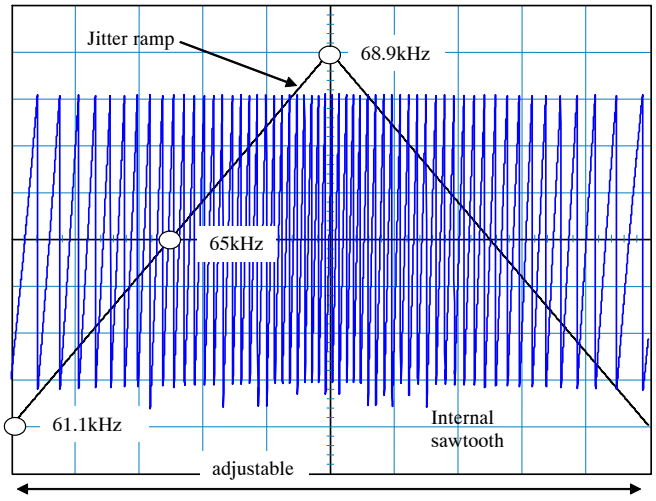


Figure 32. Modulation Effects on the Clock Signal by the Jittering Sawtooth

Line Detection

An internal comparator monitors the drain voltage as recovering from one of the following situations:

- Short Circuit Protection,
- V_{CC} OVP is confirmed,
- UVLO
- TSD

If the drain voltage is lower than the internal threshold $V_{HV(EN)}$ (91 Vdc typically), the internal power switch is inhibited. This avoids operating at too low ac input. This is also called brown−in function in some fields.

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires to change the traditional fixed−frequency type of operation. This device implements a switching frequency folback when the feedback current passes above a certain level, I_{FBfold}, set around 68 μA. At this point, the oscillator enters frequency foldback and reduces its switching frequency.

The internal peak current set−point is following the feedback current information until its level reaches the minimal freezing level point of I_{Freeze}. The only way to further reduce the transmitted power is to diminish the operating frequency down to F_{min} (25 kHz typically). This value is reached at a feedback current level of $I_{FBfold(end)}$. Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise−free performance in no−load conditions. Figures 33 and 34 depict the adopted scheme for the part.

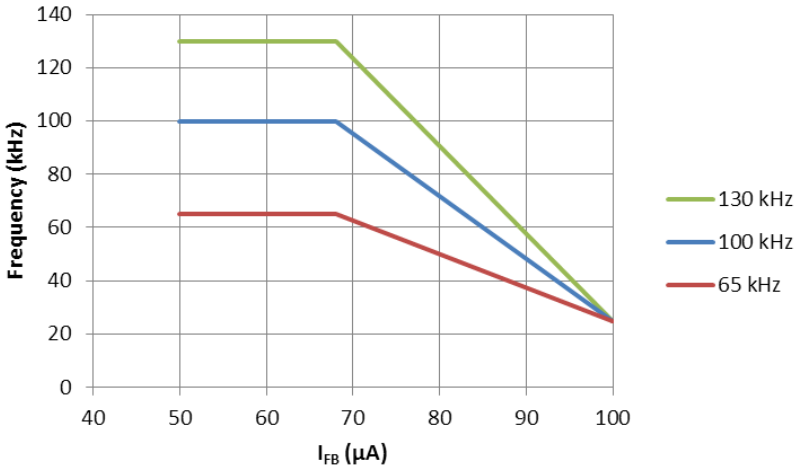


Figure 33. By Observing the Current on the Feedback Pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

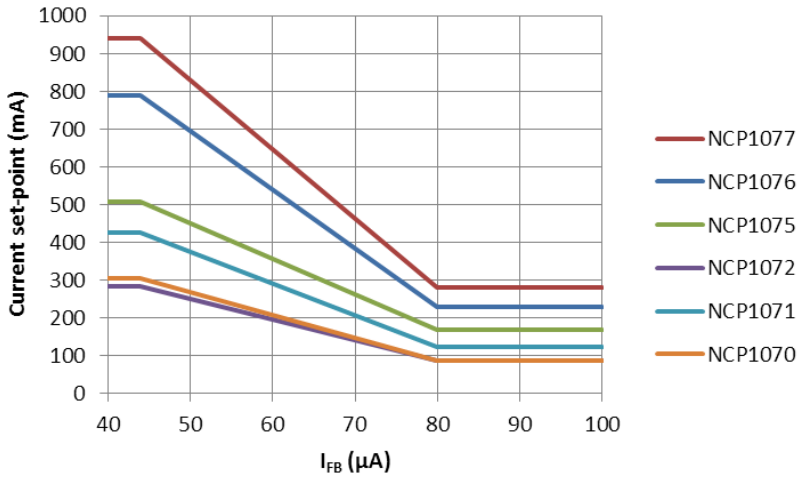


Figure 34. Ipk Set−point is Frozen at Lower Power Demand.

Feedback and Skip

Figure 35 depicts the relationship between feedback voltage and current. The feedback pin operates linearly as the absolute value of feedback current (I_{FB}) is above 40 µA. In this linear operating range, the dynamic resistance is 19.5 kΩ typically ($R_{FB(up)}$) and the effective pull up voltage is 3.3 V typically ($V_{FB(REF)}$). When I_{FB} is below 40 µA, the FB voltage will jump to close to 4.5 V.

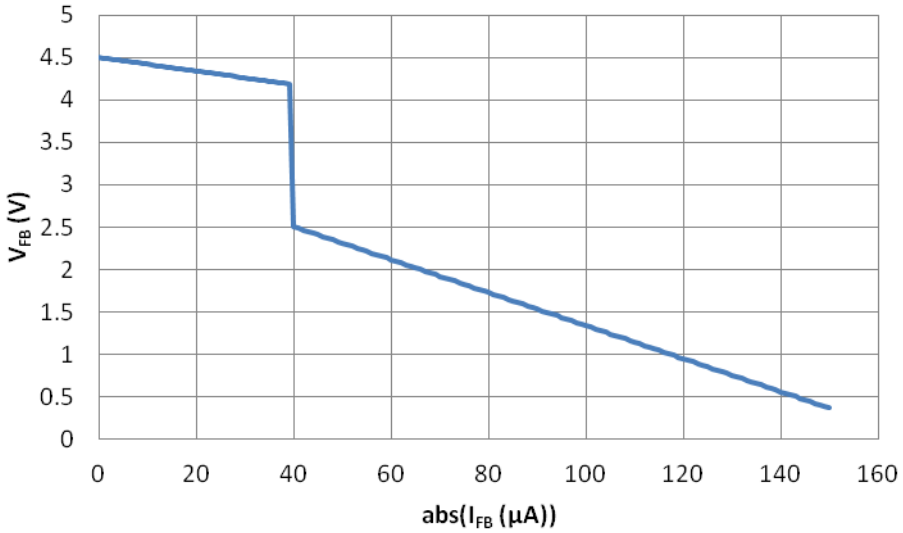


Figure 35. Feedback Voltage vs. Current

Figure 36 depicts the skip mode block diagram. When the FB current information reaches I_{FBskip}, the internal clock to set the flip−flop is blanked and the internal consumption of the controller is decreased. The hysteresis of internal skip comparator is minimized to lower the ripple of the auxiliary voltage for V_{CC} pin and V_{OUT} of power supply during skip mode. It easies the design of V_{CC} over load range.

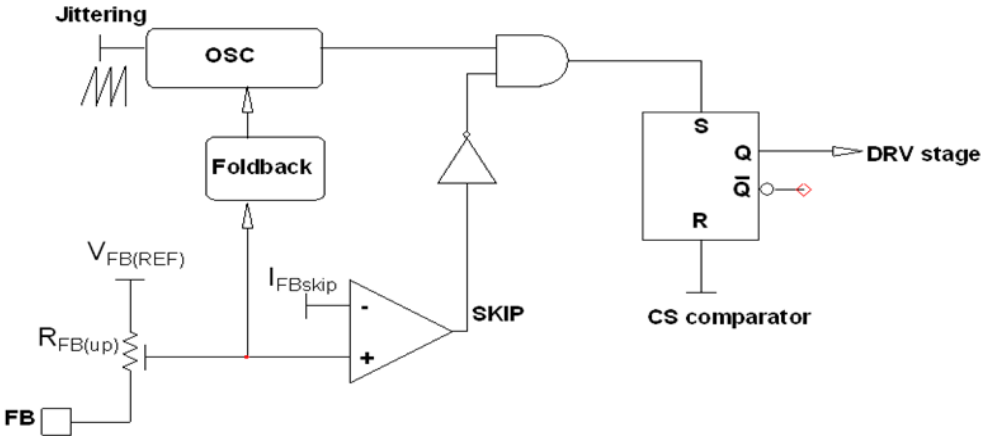


Figure 36. Skip Cycle Schematic

Ramp Compensation and Ipk Set−point

In order to allow the NCP107X to operate in CCM with a duty cycle above 50%, a fixed slope compensation is internally applied to the current−mode control.

Here we got a table of the ramp compensation, the initial current set point, and the final current set−point of different versions of switcher.

	Fsw	Sa	Ipk(Duty = 50%)	Ipk(0)
NCP1070	65 kHz	7 mA/μs	250 mA	304 mA
	100 kHz	11 mA/μs		
	130 kHz	14 mA/μs		
NCP1071	65 kHz	10 mA/μs	350 mA	425 mA
	100 kHz	15 mA/μs		
	130 kHz	20 mA/μs		
NCP1072	65 kHz	4.2 mA/μs	250 mA	282 mA
	100 kHz	6.5 mA/μs		
	130 kHz	8.4 mA/μs		
NCP1075	65 kHz	7.5 mA/μs	450 mA	508 mA
	100 kHz	11.5 mA/μs		
	130 kHz	15 mA/μs		
NCP1076	65 kHz	15 mA/μs	650 mA	765 mA
	100 kHz	23 mA/μs		
	130 kHz	30 mA/μs		
NCP1077	65 kHz	18 mA/μs	800 mA	940 mA
	100 kHz	28 mA/μs		
	130 kHz	36 mA/μs		

The Figure 37 depicts the variation of I_{PK} set−point vs. the power switcher duty ratio, which is caused by the internal ramp compensation.

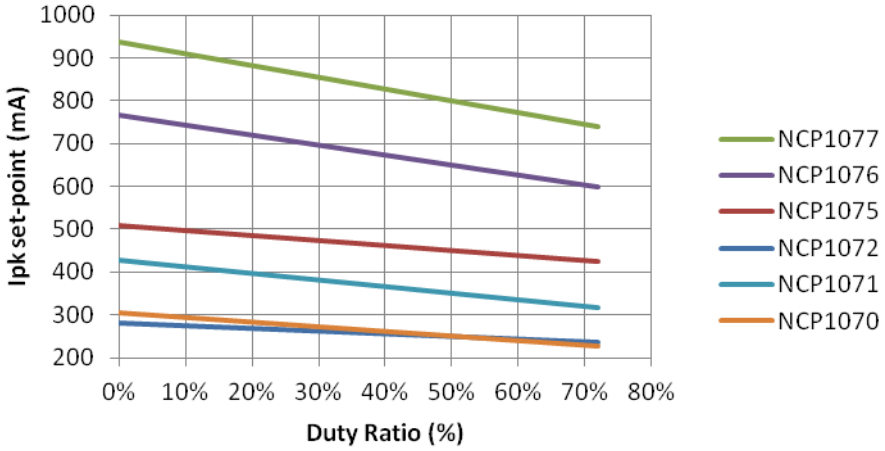


Figure 37. I_{PK} Set−point Varies with Power Switch On Time, Which is Caused by the Ramp Compensation

Design Procedure

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

V_{in} min = 90 Vac or 127 Vdc once rectified, assuming a low bulk ripple
V_{in} max = 265 Vac or 375 Vdc
V_{out} = 12 V
P_{out} = 10 W
Operating mode is CCM
η = 0.8

1. The lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation as shown by Figure 38. This condition sets the maximum voltage that can be reflected during t_{off}. As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

$$N(V_{out} + V_f) < V_{in,min} \qquad \text{(eq. 3)}$$

2. In our case, since we operate from a 127 V DC rail while delivering 12 V, we can select a reflected voltage of 120 Vdc maximum. Therefore, the turn ratio Np:Ns must be smaller than

$$\frac{V_{reflect}}{V_{out} + V_f} = \frac{120}{12 + 0.5} = 9.6$$

or Np:Ns < 9.6. Here we choose N = 8 in this case. We will see later on how it affects the calculation.

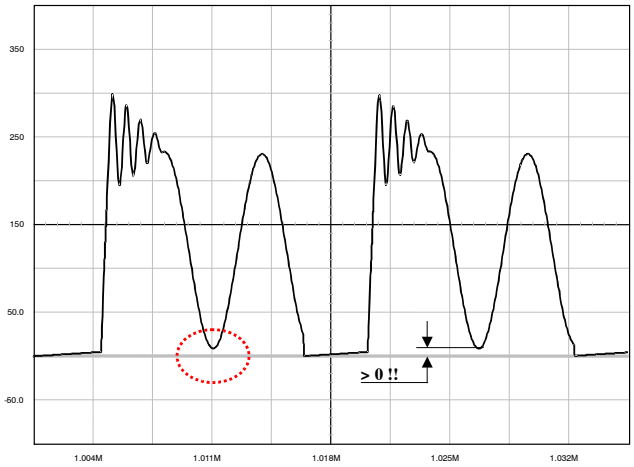


Figure 38. The Drain−Source Wave Shall Always be Positive

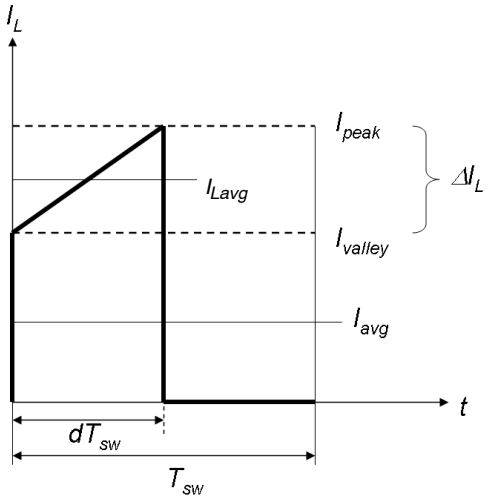


Figure 39. Primary Inductance Current Evolution in CCM

3. Lateral MOSFETs have a poorly doped body−diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

$$V_{drain,max} = V_{in} + N(V_{out} + V_f) + I_{peak}\sqrt{\frac{L_f}{C_{tot}}} \quad \text{(eq. 4)}$$

where L_f is the leakage inductance, C_{tot} the total capacitance at the drain node (which is increased by the capacitor you will wire between drain and source), N the N_P:N_S turn ratio, V_{out} the output voltage, V_f the secondary diode forward drop and finally, I_{peak} the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the V_{out} target is almost reached and I_{peak} is still pushed to the maximum. For this design, we have selected our maximum voltage around 650 V (at V_{in} = 375 Vdc). This voltage is given by the *RCD* clamp installed from the drain to the bulk voltage. We will see how to calculate it later on.

4. Calculate the maximum operating duty−cycle for this flyback converter operated in CCM:

$$d_{max} = \frac{N(V_{out} + V_f)}{N(V_{out} + V_f) + V_{in,min}} = \frac{1}{1 + \frac{V_{in,min}}{N(V_{out}+V_f)}} = 0.44 \quad \text{(eq. 5)}$$

5. To obtain the primary inductance, we have the choice between two equations:

$$L = \frac{(V_{in}d)^2}{f_{sw}KP_{in}} \quad \text{(eq. 6)}$$

where

$$K = \frac{\Delta I_L}{I_{Lavg}}$$

and defines the amount of ripple we want in CCM (see Figure 39).

- Small K: deep CCM, implying a large primary inductance, a low bandwidth and a large leakage inductance.
- Large K: approaching BCM where the rms losses are worse, but smaller inductance, leading to a better leakage inductance.

From Equation 6, a *K* factor of 1 (50% ripple), gives an inductance of:

$$L = \frac{(127 \times 0.44)^2}{65k \times 1 \times 12.75} = 3.8\ mH$$

$$\Delta I_L = \frac{V_{in,min} \cdot d_{max}}{LF_{SW}} = \frac{127 \times 0.44}{3.8 \times 65k}$$

$$= 223\ mA\ peak\text{−}to\text{−}peak$$

The peak current can be evaluated to be:

$$I_{peak} = \frac{I_{avg}}{d} + \frac{\Delta I_L}{2} = I_{peak} = \frac{98m}{0.44} + \frac{\Delta I_L}{2}$$

$$= 335\ mA$$

On I_L, I_{Lavg} can also be calculated:

$$I_{Lavg} = I_{peak} - \frac{\Delta I_L}{2} = 0.34 - 0.112 = 223\ mA$$

6. Based on the above numbers, we can now evaluate the conduction losses:

$$I_{d,rms} = \sqrt{d\left(I_{peak}^2 - I_{peak}\Delta I_L + \frac{\Delta I_L^2}{3}\right)}$$

$$= \sqrt{0.44\left(0.335^2 - 0.335 \cdot 0.223 + \frac{0.223^2}{3}\right)}$$

$$= 154\ mA$$

If we take the maximum $R_{ds(on)}$ for a 125°C junction temperature, i.e. 24 Ω, then conduction losses worse case are:

$$P_{cond} = I_{d,rms}^2 R_{DS(on)} = 570\ mW$$

7. Off−time and on−time switching losses can be estimated based on the following calculations:

$$P_{off} = \frac{I_{peak}(V_{bulk} + V_{clamp})t_{off}}{2T_{sw}}$$

$$= \frac{0.335 \times (127 + 120 \cdot 2) \times 10n}{2 \times 15.4\mu} \quad \text{(eq. 7)}$$

$$= 36\ mW$$

Where, assume the V_{clamp} is equal to two times of reflected voltage.

$$P_{on} = \frac{I_{valley}\left(V_{bulk} + N\left(V_{out} + V_f\right)\right)t_{on}}{6T_{sw}}$$

$$= \frac{0.111 \times (127 + 100) \times 20n}{6 \times 15.4\mu} \quad \text{(eq. 8)}$$

$$= 5.5\ \text{mW}$$

It is noted that the overlap of voltage and current seen on MOSFET during turning on and off duration is dependent on the snubber and parasitic capacitance seen from drain pin. Therefore the t_{off} and t_{on} in Equations 7 and 8 have to be modified after measuring on the bench.

8. The theoretical total power is then 0.570 + 0.036 + 0.0055 = 611 mW
9. If the NCP107X operates at DSS mode, then the losses caused by DSS mode should be counted as losses of this device on the following calculation:

$$P_{DSS} = I_{CC1} \cdot V_{in,max} = 1m \cdot 375 = 375\ \text{mW} \quad \text{(eq. 9)}$$

MOSFET protection

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BVdss which is 700 V. Figure 40a, b, c present possible implementations:

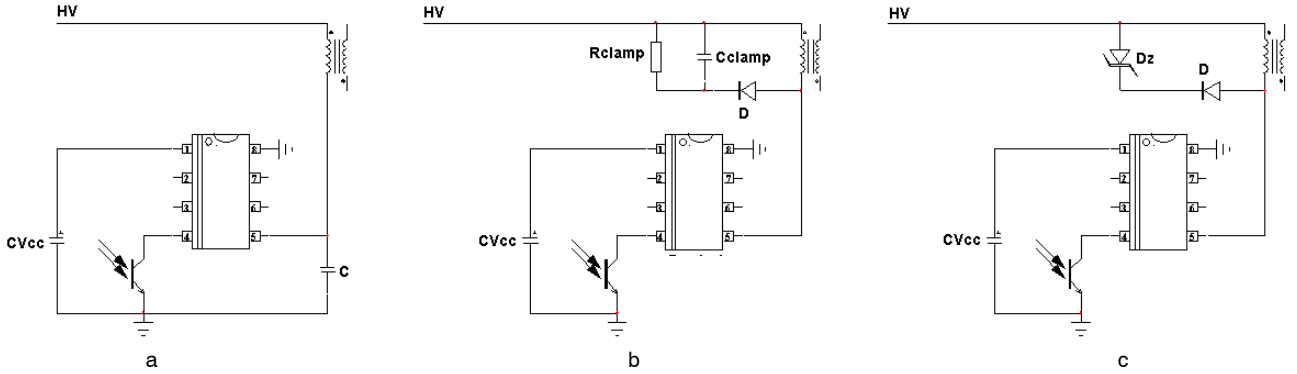


Figure 40. Different Options to Clamp the Leakage Spike

Figure 40*a*: the simple capacitor limits the voltage according to The lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation as shown by Figure 38. This condition sets the maximum voltage that can be reflected during t_{off}. As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation: Equation 3. This option is only valid for low power applications, e.g. below 5 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with Equation 4. Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses...

Figure 40*b*: the most standard circuitry is called the *RCD* network. You calculate R_{clamp} and C_{clamp} using the following formulae:

$$R_{clamp} = \frac{2\,V_{clamp}\left(V_{clamp} - \left(V_{out} + V_f\right)N\right)}{L_{leak}I_{peak}{}^2F_{sw}} \quad \text{(eq. 10)}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple}F_{sw}R_{clamp}} \quad \text{(eq. 11)}$$

V_{clamp} is usually selected 50−80 V above the reflected value N x (V_{out} + V_f). The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worse case occurs when I_{peak} and V_{in} are maximum and V_{out} is close to reach the steady−state value.

Figure 40*c*: this option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of zener. A 5 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. Select the zener or TVS clamping level between 40 to 80 V above the reflected output voltage when the supply is heavily loaded.

Power Dissipation and Heatsinking

The NCP107X welcomes two dissipating terms, the DSS current−source (when active) and the MOSFET. Thus, $P_{tot} = P_{DSS} + P_{MOSFET}$. It is mandatory to properly manage the heat generated by losses. If no precaution is taken, risks exist to trigger the internal thermal shutdown (TSD). To help dissipating the heat, the PCB designer must foresee large copper areas around the package. Take the PDIP−7 package as an example, when surrounded by a surface greater than 1.0 cm^2 of 35 μm copper, it becomes possible to drop its thermal resistance junction−to−ambient, $R_{\theta JA}$ down to 75°C/W and thus dissipate more power. The maximum power the device can thus evacuate is:

$$P_{max} = \frac{T_{Jmax} - T_{ambmax}}{R_{\theta JA}} \quad \text{(eq. 12)}$$

which gives around 930 mW for an ambient of 50°C and a maximum junction of 120°C. If the surface is not large enough, assuming the $R_{\theta JA}$ is 100°C/W, then the maximum power the device can evacuate becomes 700 mW. Figure 41 gives a possible layout to help drop the thermal resistance.

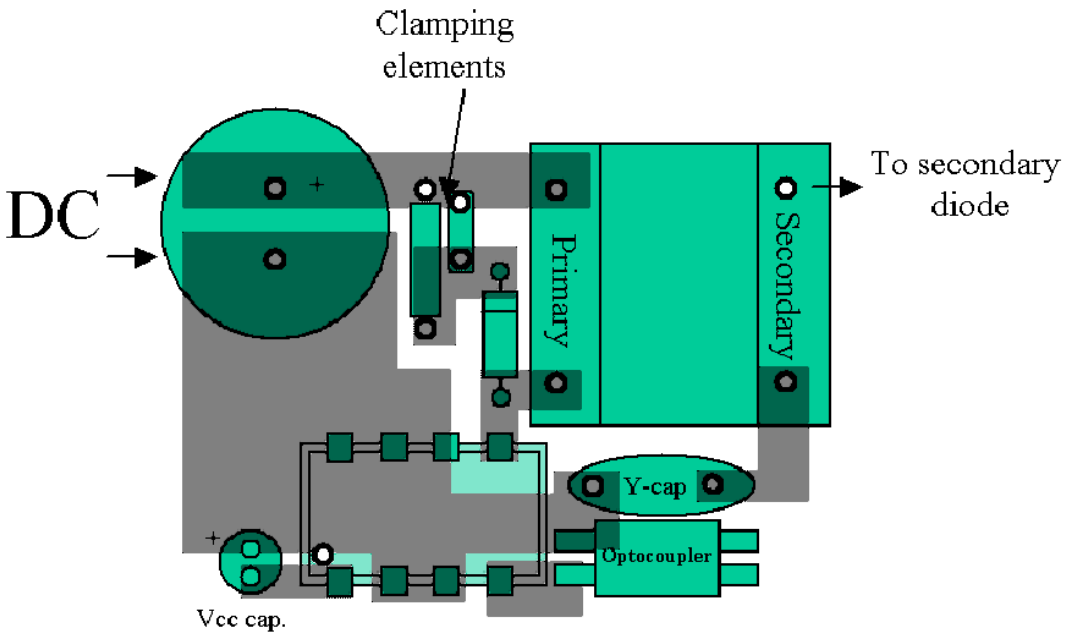


Figure 41. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction−to−Ambient

A 10 W NCP1075 based Flyback Converter Featuring Low Standby Power

Figure 43 depicts a typical application showing a NCP1075−65 kHz operating in a 10 W converter. To leave more room for the MOSFET, it is recommended to disable the DSS by shorting the J3. In this application, the feedback is made via a NCP431 whose low bias current (50 μA) helps to lower the no load standby power.

Measurements have been taken from a demonstration board implementing the diagram in Figure 43 and the following results were achieved with auxiliary winding to bias the device:

	100 Vac	115 Vac	230 Vac	265 Vac
No load consumption with auxiliary winding	26 mW	28 mW	38 mW	45 mW

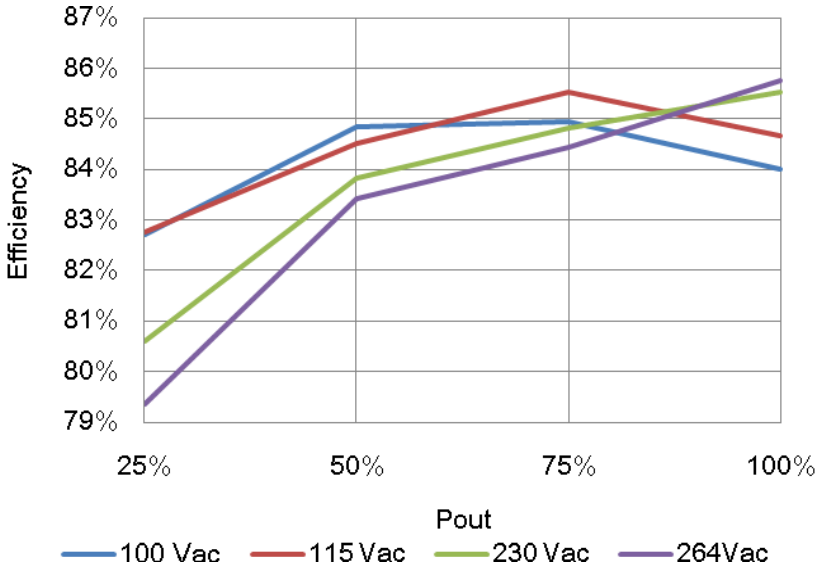


Figure 42. V_{out} = 12 V

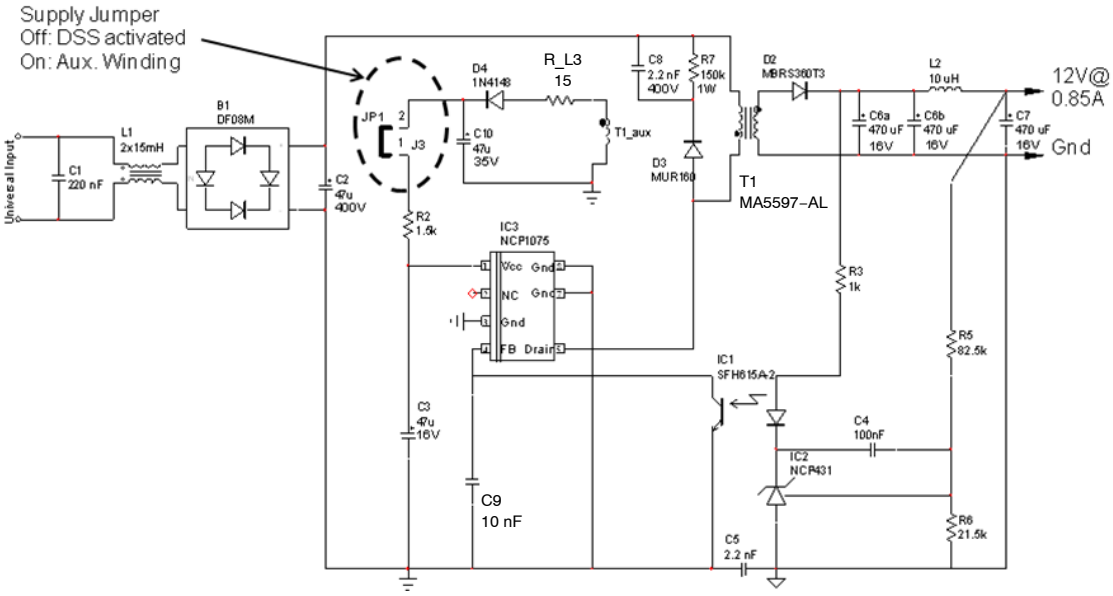


Figure 43. A 12 V – 0.85 A Universal Mains Power Supply

ORDERING INFORMATION

Device	Frequency	$R_{DS(on)}$ (Ω)	Ipk (mA)	Package Type	Shipping†
NCP1071STBT3G	100 kHz	22	350	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1072STAT3G	65 kHz	11	250	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1072STBT3G	100 kHz	11	250		4000 / Tape & Reel
NCP1072P100BG	100 kHz	11	250	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1075STAT3G	65 kHz	11	450	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1075STBT3G	100 kHz	11	450		4000 / Tape & Reel
NCP1075STCT3G	130 kHz	11	450		4000 / Tape & Reel
NCP1075P065G	65 kHz	11	450	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1075P100G	100 kHz	11	450		50 Units / Rail
NCP1076STAT3G	65 kHz	4.7	650	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1076STBT3G	100 kHz	4.7	650		4000 / Tape & Reel
NCP1076STCT3G	130 kHz	4.7	650		4000 / Tape & Reel
NCP1076P065G	65 kHz	4.7	650	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1076P100G	100 kHz	4.7	650		50 Units / Rail
NCP1077STAT3G	65 kHz	4.7	800	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1077STBT3G	100 kHz	4.7	800		4000 / Tape & Reel
NCP1077STCT3G	130 kHz	4.7	800		4000 / Tape & Reel
NCP1077P100G	100 kHz	4.7	800	PDIP−7 (Pb−Free)	50 Units / Rail

DISCONTINUED (Note 8)

Device	Frequency	$R_{DS(on)}$ (Ω)	Ipk (mA)	Package Type	Shipping†
NCP1070STAT3G	65 kHz	22	250	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1070STBT3G	100 kHz	22	250		4000 / Tape & Reel
NCP1070STCT3G	130 kHz	22	250		4000 / Tape & Reel
NCP1070P065G	65 kHz	22	250	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1070P100G	100 kHz	22	250		50 Units / Rail
NCP1070P130G	130 kHz	22	250		50 Units / Rail
NCP1071STAT3G	65 kHz	22	350	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1071STCT3G	130 kHz	22	350	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1071P065G	65 kHz	22	350	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1071P100G	100 kHz	22	350		50 Units / Rail
NCP1071P130G	130 kHz	22	350		50 Units / Rail
NCP1072P065G	65 kHz	11	250	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1072P100G	100 kHz	11	250		50 Units / Rail
NCP1075P130G	130 kHz	11	450	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1076P130G	130 kHz	4.7	650	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1077P065G	65 kHz	4.7	800	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1077P130G	130 kHz	4.7	800	PDIP−7 (Pb−Free)	50 Units / Rail

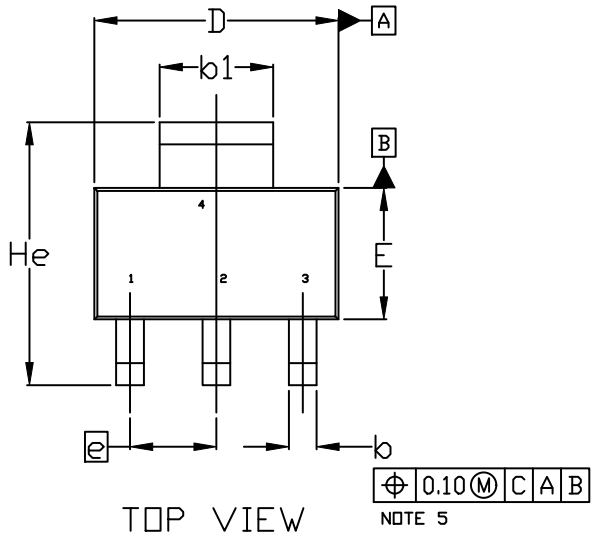
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

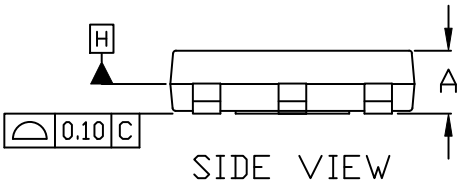
8. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

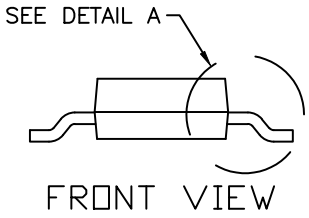
SCALE 1:1

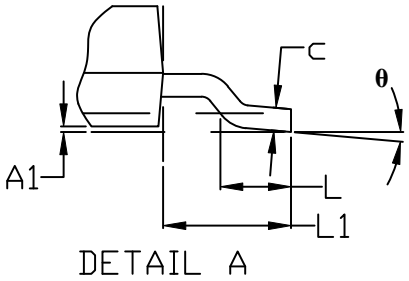
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



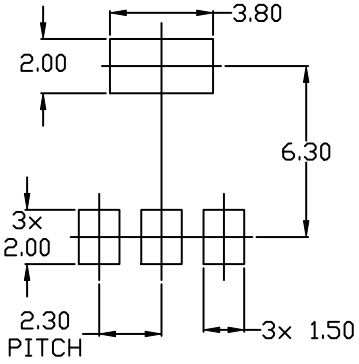






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

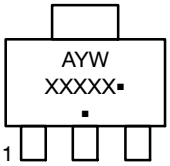
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

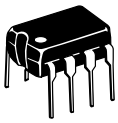
GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

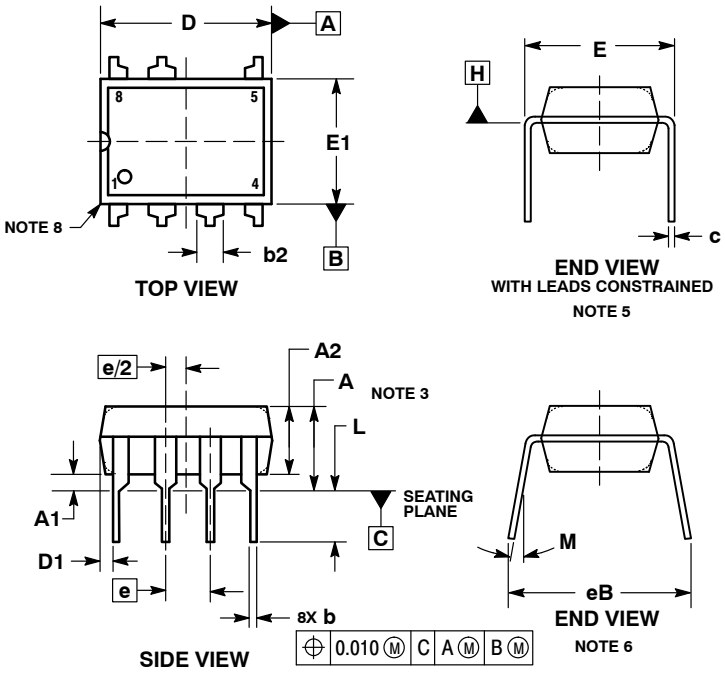
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C

DATE 22 APR 2015

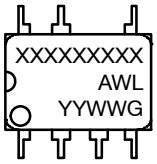
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**PDIP−7 (PDIP−8 LESS PIN 6)**		**PAGE 1 OF 1**

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