

Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO247-4, 1200 V, 150 mohm

UF3C120150K4S

Description

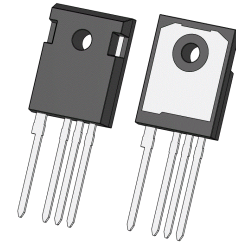
This SiC cascode JFET co-packages onsemi's high performance F3 SiC fast JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits very fast switching using a 4-terminal TO247-4 package and the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.

Features

- Typical On-resistance $R_{DS(on),typ}$ of 150 m Ω
- Maximum Operating Temperature of 175 °C
- Excellent Reverse Recovery
- Low Gate Charge
- Low Intrinsic Capacitance
- ESD Protected, HBM Class 2
- TO-247-4 Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

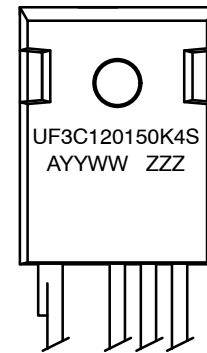
Typical Applications

- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating



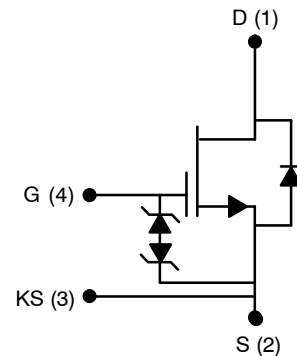
TO247-4 15.90x20.96x5.03, 5.44P
CASE 340AN

MARKING DIAGRAM



UF3C120150K4S = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1200	V
Gate-source Voltage	V_{GS}	DC	-25 to +25	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25\text{ }^{\circ}\text{C}$	18.4	A
		$T_C = 100\text{ }^{\circ}\text{C}$	13.8	A
Pulsed Drain Current (Note 2)	I_{DM}	$T_C = 25\text{ }^{\circ}\text{C}$	38	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	$L = 15\text{ mH}$, $I_{AS} = 2\text{ A}$	30	mJ
Power Dissipation	P_{tot}	$T_C = 25\text{ }^{\circ}\text{C}$	166.7	W
Maximum Junction Temperature	$T_{J, max}$		175	$^{\circ}\text{C}$
Operating and Storage Temperature	T_J , T_{STG}		-55 to 175	$^{\circ}\text{C}$
Max. Lead Temperature for Soldering, 1/8" from Case for 5 seconds	T_L		250	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J, max}$.
2. Pulse width t_p limited by $T_{J, max}$.
3. Starting $T_J = 25\text{ }^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.7	0.9	$^{\circ}\text{C/W}$

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ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-source Breakdown Voltage	BV _{DS}	V _{GS} = 0 V, I _D = 1 mA	1200	–	–	V
Total Drain Leakage Current	I _{DSS}	V _{DS} = 1200 V, V _{GS} = 0 V, T _J = 25 °C	–	2	50	μA
		V _{DS} = 1200 V, V _{GS} = 0 V, T _J = 175 °C	–	17	–	
Total Gate Leakage Current	I _{GSS}	V _{DS} = 0 V, T _J = 25 °C, V _{GS} = –20 V / +20 V	–	4	20	μA
Drain-source On-resistance	R _{DS(on)}	V _{GS} = 12 V, I _D = 5 A, T _J = 25 °C	–	150	180	mΩ
		V _{GS} = 12 V, I _D = 5 A, T _J = 125 °C	–	250	–	
		V _{GS} = 12 V, I _D = 5 A, T _J = 175 °C	–	330	–	
Gate Threshold Voltage	V _{G(th)}	V _{DS} = 5 V, I _D = 10 mA	3.5	4.4	5.5	V
Gate Resistance	R _G	f = 1 MHz, open drain	–	4.6	–	Ω

TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current (Note 1)	I _S	T _C = 25 °C	–	–	18.4	A
Diode Pulse Current (Note 2)	I _{S, pulse}	T _C = 25 °C	–	–	38	A
Forward Voltage	V _{FSD}	V _{GS} = 0 V, I _S = 5 A, T _J = 25 °C	–	1.46	2	V
		V _{GS} = 0 V, I _S = 5 A, T _J = 175 °C	–	2	–	
Reverse Recovery Charge	Q _{rr}	V _{DS} = 800 V, I _S = 13 A, V _{GS} = –5 V, R _{G, EXT} = 22 Ω, di/dt = 1700 A/μs, T _J = 25 °C	–	67	–	nC
Reverse Recovery Time	t _{rr}		–	24	–	ns
Reverse Recovery Charge	Q _{rr}	V _{DS} = 800 V, I _S = 13 A, V _{GS} = –5 V, R _{G, EXT} = 22 Ω, di/dt = 1700 A/μs, T _J = 150 °C	–	64	–	nC
Reverse Recovery Time	t _{rr}		–	24	–	ns

TYPICAL PERFORMANCE – DYNAMIC

Input Capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 100 kHz	–	738	–	pF
Output Capacitance	C _{oss}		–	58	–	
Reverse Transfer Capacitance	C _{rss}		–	1.8	–	
Effective Output Capacitance, Energy Related	C _{oss(er)}	V _{DS} = 0 V to 800 V, V _{GS} = 0 V	–	34	–	pF
Effective Output Capacitance, Time Related	C _{oss(tr)}		–	68	–	pF
C _{oss} Stored Energy	E _{oss}	V _{DS} = 800 V, V _{GS} = 0 V	–	10.8	–	μJ
Total Gate Charge	Q _G	V _{DS} = 800 V, I _D = 13 A, V _{GS} = –5 V to 12 V	–	25.7	–	nC
Gate-drain Charge	Q _{GD}		–	6	–	
Gate-source Charge	Q _{GS}		–	10	–	
Turn-on Delay Time	t _{d(on)}	V _{DS} = 800 V, I _D = 13 A, Gate Driver = –5 V to +12 V, Turn-on R _{G, EXT} = 8.5 Ω, Turn-off R _{G, EXT} = 22 Ω, Inductive Load, FWD: same device with V _{GS} = –5 V, R _G = 22 Ω, T _J = 25 °C	–	21	–	ns
Rise Time	t _r		–	8	–	
Turn-off Delay Time	t _{d(off)}		–	26	–	
Fall Time	t _f		–	8	–	
Turn-on Energy	E _{ON}		–	170	–	μJ
Turn-off Energy	E _{OFF}		–	26	–	
Total Switching Energy	E _{TOT}		–	196	–	

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ELECTRICAL CHARACTERISTICS ($T_J = +25\text{ }^{\circ}\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 800\text{ V}$, $I_D = 13\text{ A}$, Gate Driver = 5 V to $+12\text{ V}$, Turn-on $R_{G,EXT} = 8.5\text{ }\Omega$, Turn-off $R_{G,EXT} = 22\text{ }\Omega$, Inductive Load, FWD: same device with $V_{GS} = -5\text{ V}$, $R_G = 22\text{ }\Omega$, $T_J = 150\text{ }^{\circ}\text{C}$	–	18	–	ns
Rise Time	t_r		–	6	–	
Turn-off Delay Time	$t_{d(off)}$		–	26	–	
Fall Time	t_f		–	7	–	
Turn-on Energy	E_{ON}		–	152	–	μJ
Turn-off Energy	E_{OFF}		–	26	–	
Total Switching Energy	E_{TOTAL}		–	178	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS

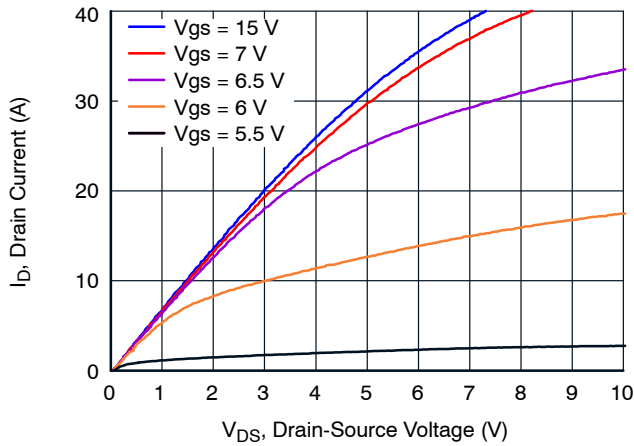


Figure 1. Typical Output Characteristics
at $T_J = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

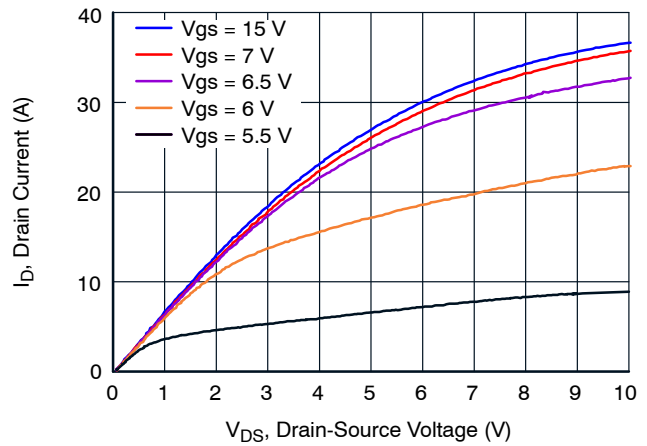


Figure 2. Typical Output Characteristics
at $T_J = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

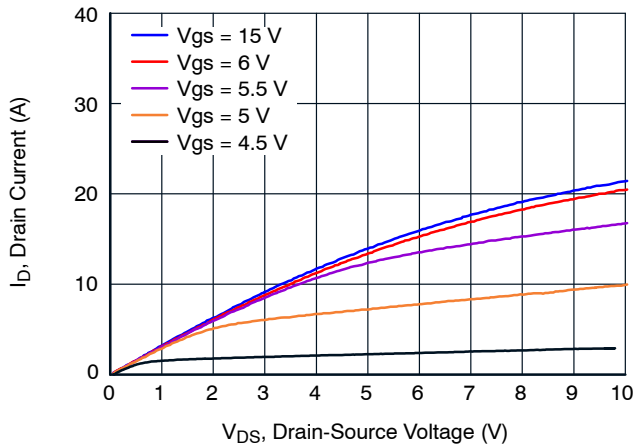


Figure 3. Typical Output Characteristics
at $T_J = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

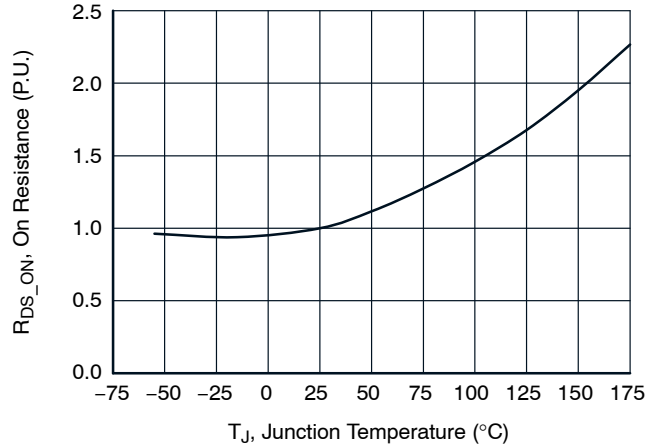


Figure 4. Normalized On-Resistance vs. Temperature at $V_{GS} = 12\text{ V}$ and $I_D = 5\text{ A}$

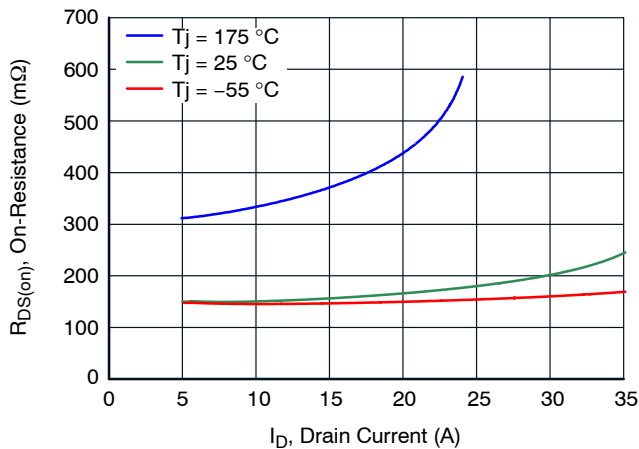


Figure 5. Typical Drain-Source On-Resistances
at $V_{GS} = 12\text{ V}$

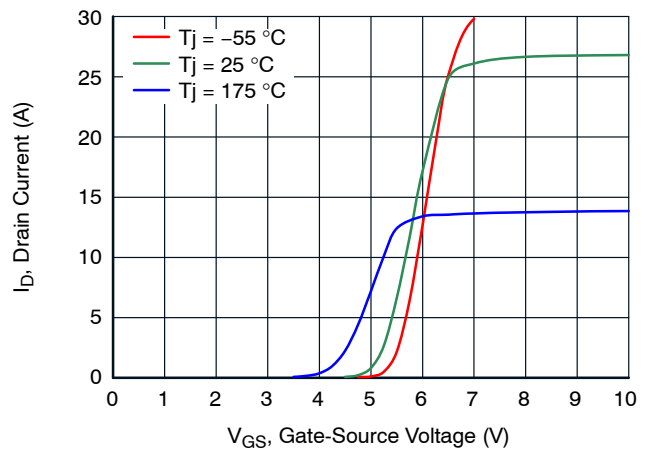


Figure 6. Typical Transfer Characteristics
at $V_{DS} = 5\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

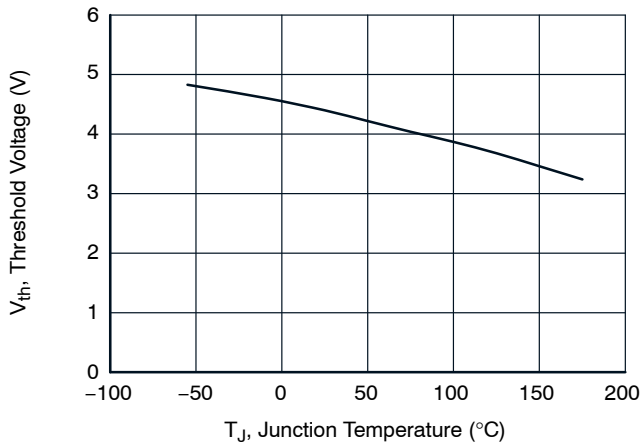


Figure 7. Threshold Voltage vs. Junction Temperature at $V_{DS} = 5\text{ V}$ and $I_D = 10\text{ mA}$

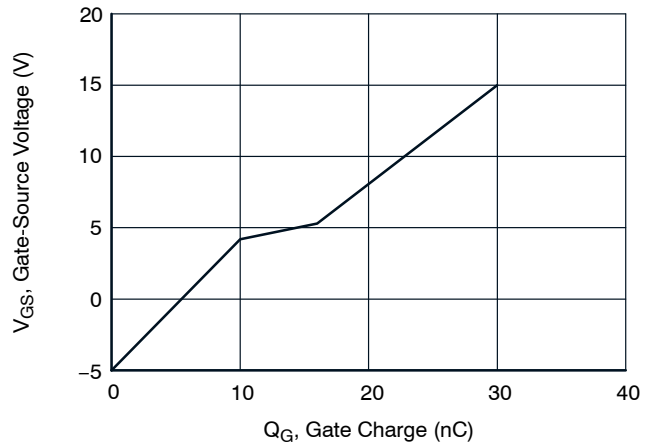


Figure 8. Typical Gate Charge at $V_{DS} = 800\text{ V}$ and $I_D = 13\text{ A}$

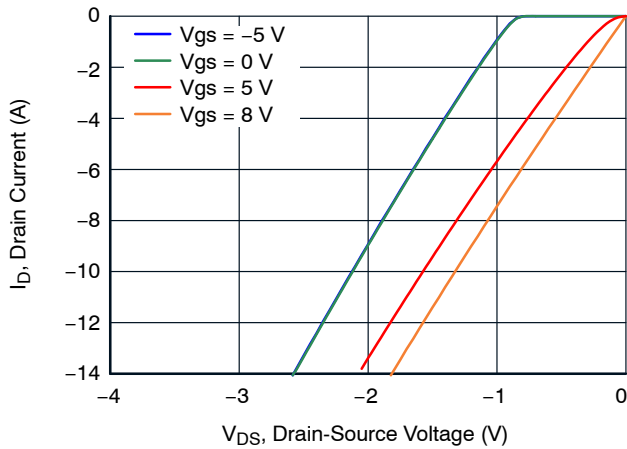


Figure 9. 3rd Quadrant Characteristics at $T_J = -55\text{ }^{\circ}\text{C}$

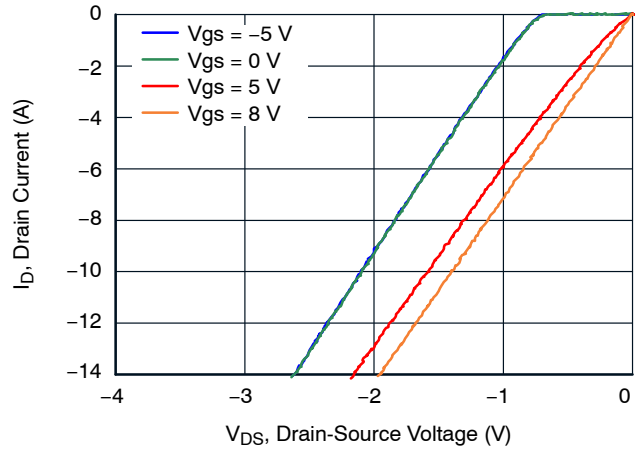


Figure 10. 3rd Quadrant Characteristics at $T_J = 25\text{ }^{\circ}\text{C}$

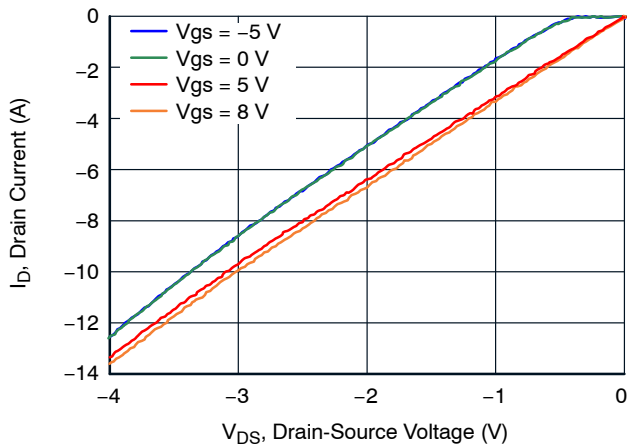


Figure 11. 3rd Quadrant Characteristics at $T_J = 175\text{ }^{\circ}\text{C}$

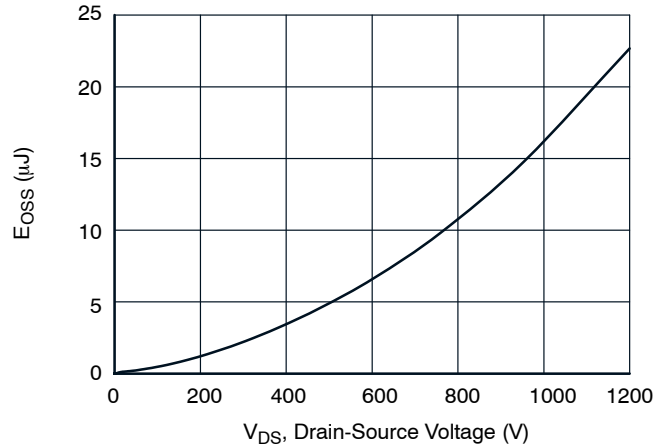


Figure 12. Typical Stored Energy in C_{OSS} at $V_{GS} = 0\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

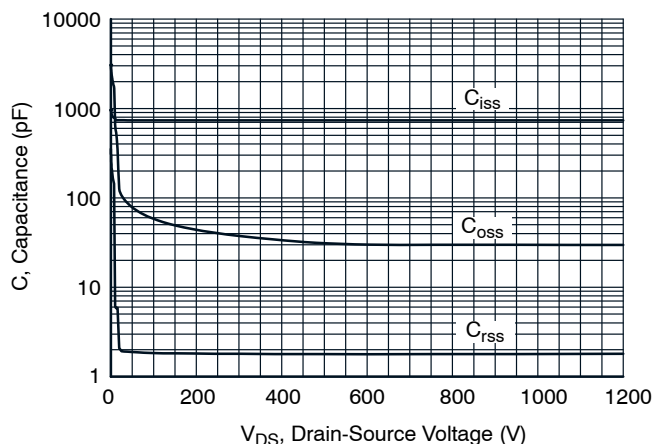


Figure 13. Typical Capacitances at $f = 100 \text{ kHz}$ and $V_{GS} = 0 \text{ V}$

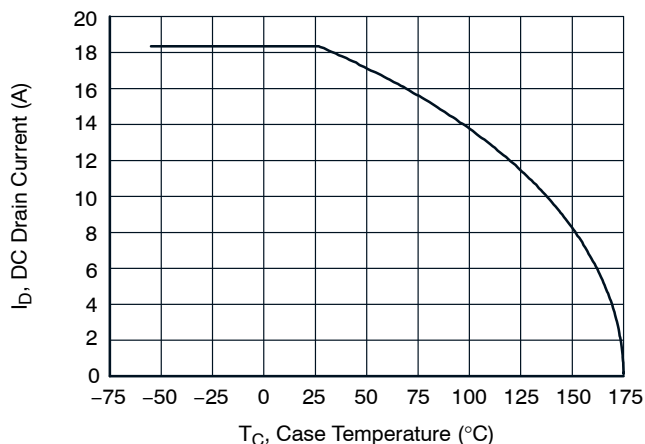


Figure 14. DC Drain Current Derating

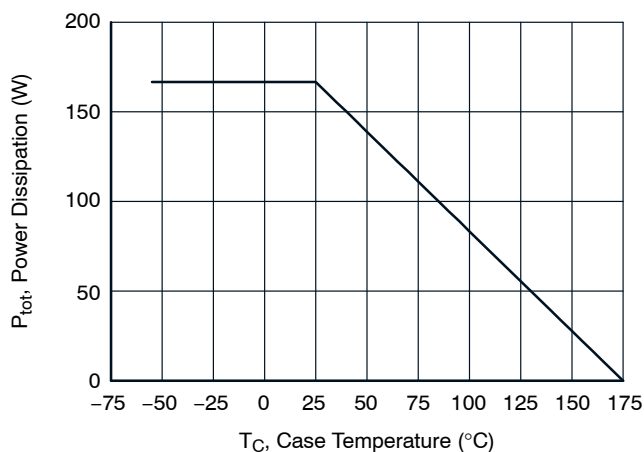


Figure 15. Total Power Dissipation

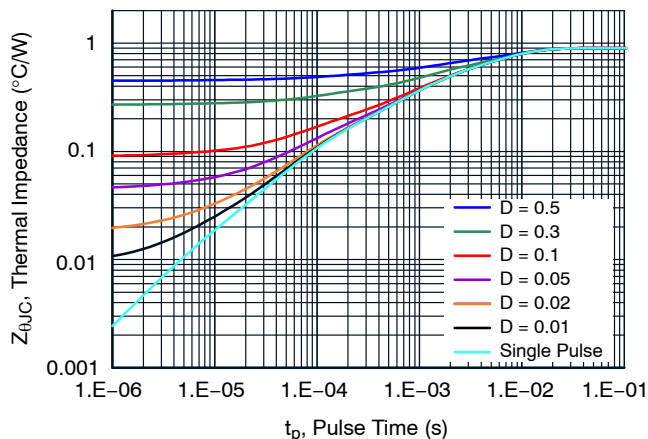


Figure 16. Maximum Transient Thermal Impedance

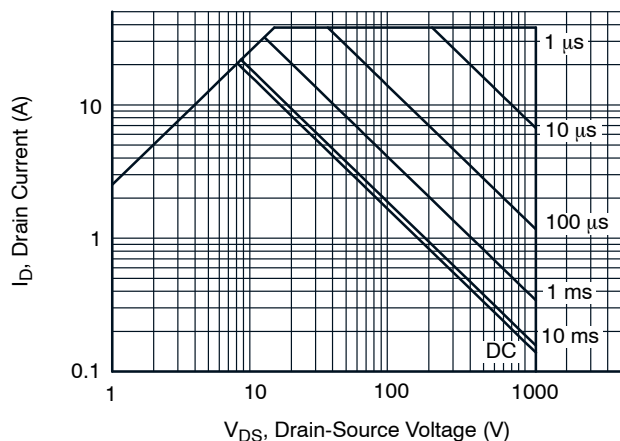


Figure 17. Safe Operation Area at $T_C = 25 \text{ }^\circ\text{C}$, $D = 0$, Parameter t_p

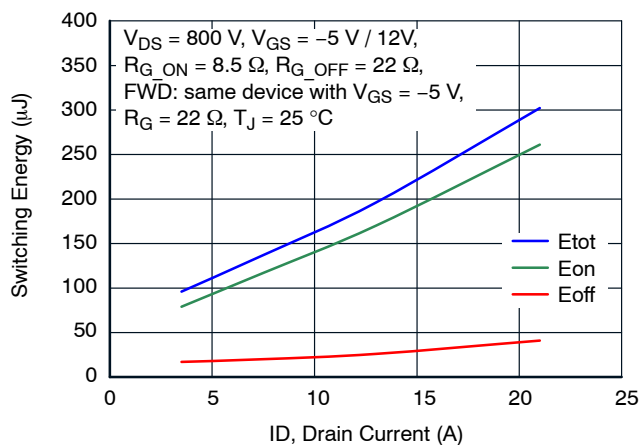
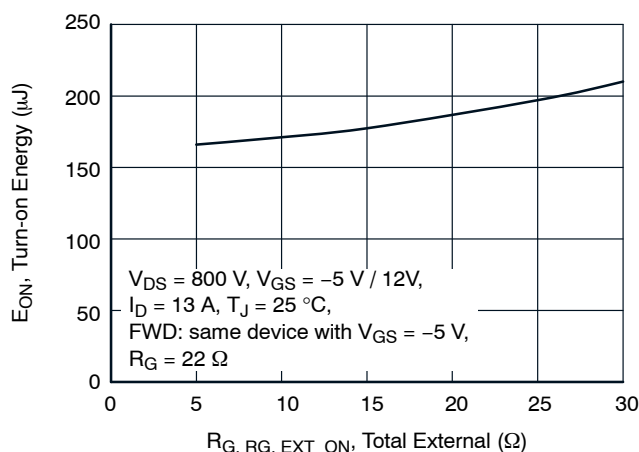
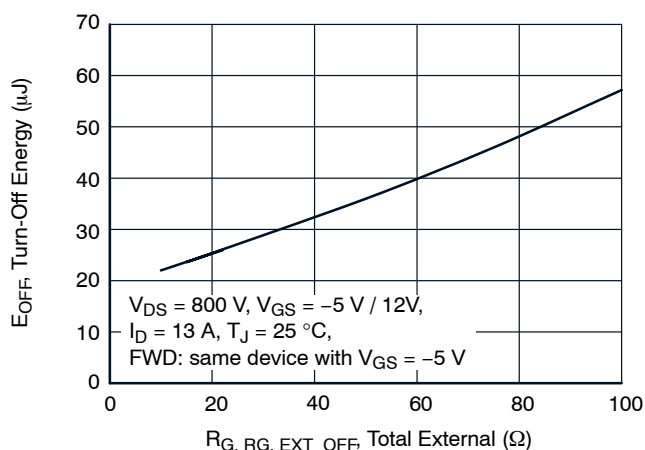


Figure 18. Clamped Inductive Switching Energy vs. Drain Current at $T_J = 25 \text{ }^\circ\text{C}$

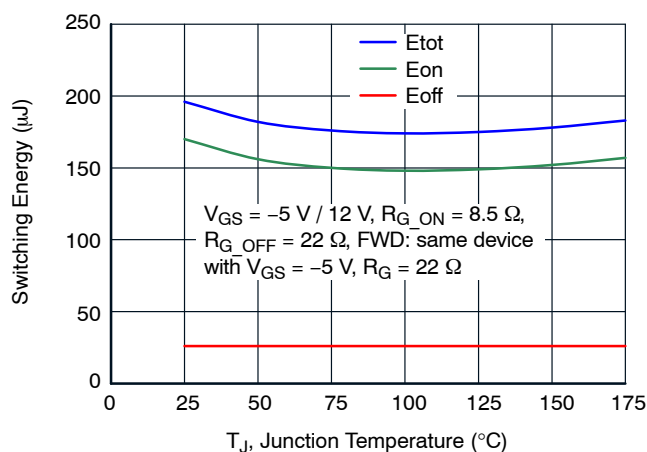
TYPICAL PERFORMANCE DIAGRAMS (continued)



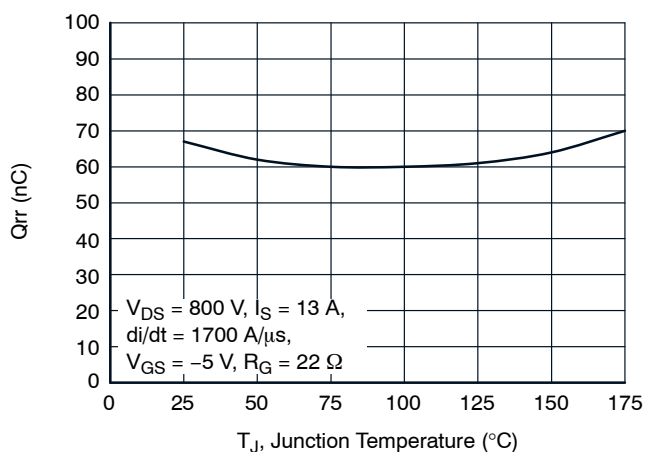
**Figure 19. Clamped Inductive Switching
Turn-on Energy vs. R_{G, EXT_ON}**



**Figure 20. Clamped Inductive Switching
Turn-off Energy vs. R_{G, EXT_OFF}**



**Figure 21. Clamped Inductive Switching Energy
vs. Junction Temperature at $V_{DS} = 800$ V, and $I_D = 13$ A**



**Figure 22. Reverse Recovery Charge Q_{rr}
vs. Junction Temperature**

APPLICATIONS INFORMATION

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction

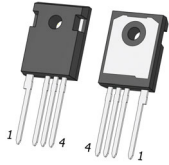
capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see **onsemi's** SiC product website link: <https://www.onsemi.com/products/discrete-power-modules/silicon-carbide-sic>

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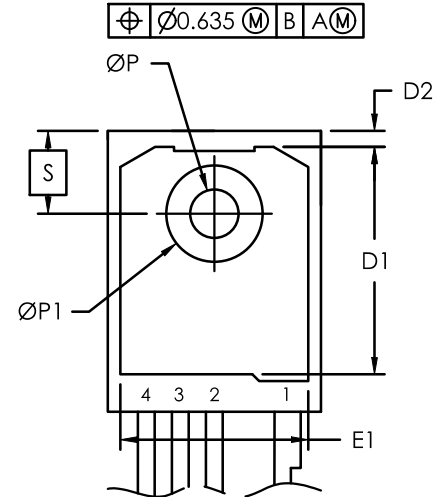
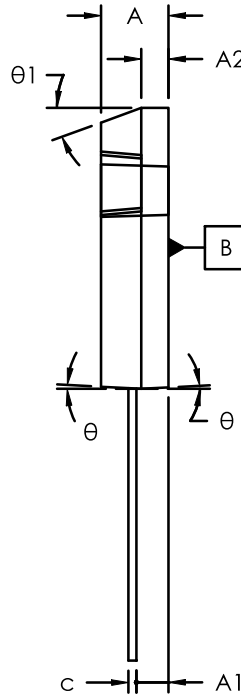
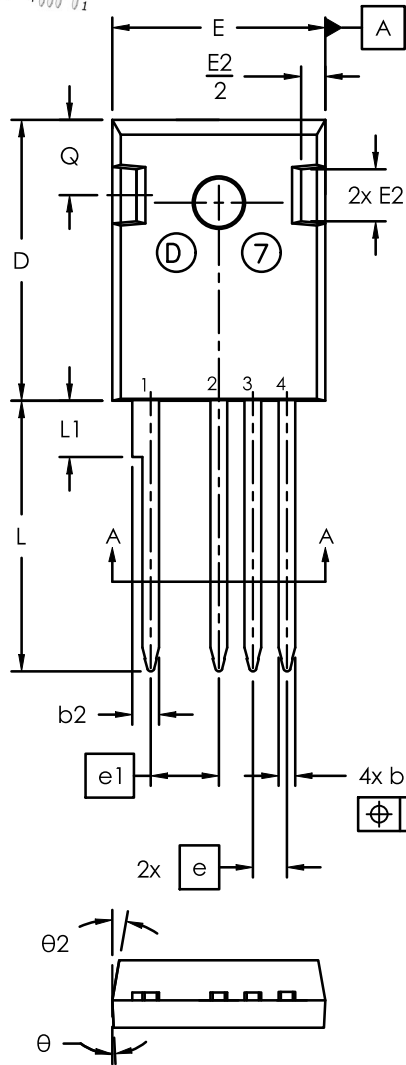
ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UF3C120150K4S	UF3C120150K4S	TO247-4 15.90x20.96x5.03, 5.44P	600 Units / Tube



TO247-4 15.90x20.96x5.03, 5.44P
CASE 340AN
ISSUE D

DATE 14 APR 2025



SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	—	—
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

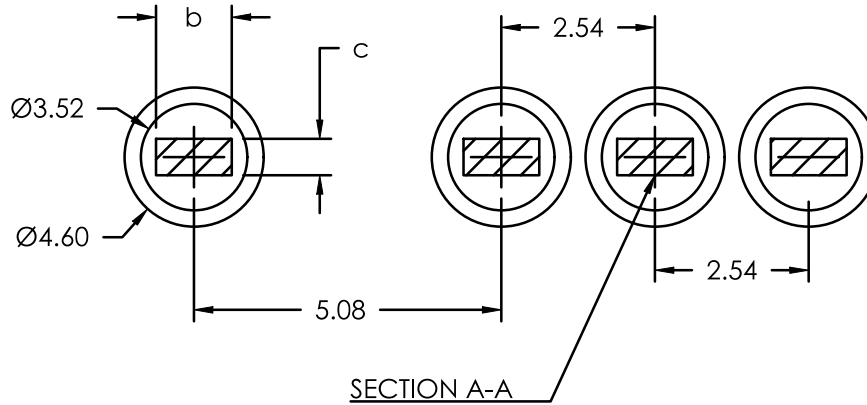
NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

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