Inverting Converter, Switching Regulator - Buck Boost, ON/OFF Function

1.5 A

NCP3064, NCP3064B, NCV3064

The NCP3064 Series is a higher frequency upgrade to the popular MC33063A and MC34063A monolithic DC−DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step−Down and Step−Up and Voltage−Inverting applications with a minimum number of external components. The ON/$\overline{\text{OFF}}$ pin provides a low power shutdown mode.

Features

- Input Voltage Range from 3.0 V to 40 V
- Logic Level Shutdown Capability
- Low Power Standby Mode, Typical 100 μA
- Output Switch Current to 1.5 A
- Adjustable Output Voltage Range
- 150 kHz Frequency Operation
- Precision 1.5% Reference
- Internal Thermal Shutdown Protection
- Cycle−by−Cycle Current Limiting
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These are Pb−Free Devices

Applications

- Step−Down, Step−Up and Inverting supply applications
- High Power LED Lighting
- Battery Chargers

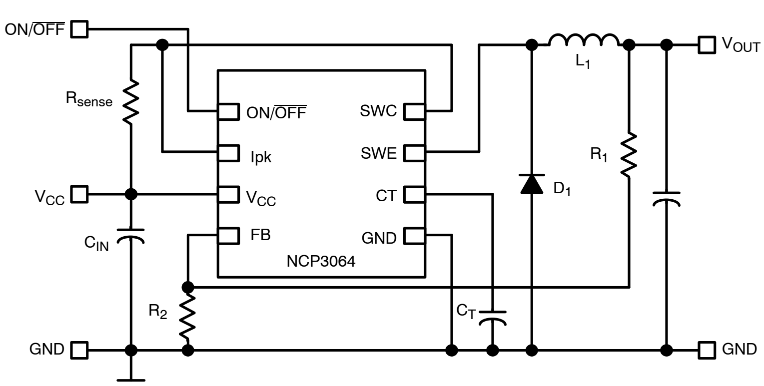
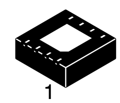
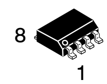


Figure 1. Typical Buck Application Circuit

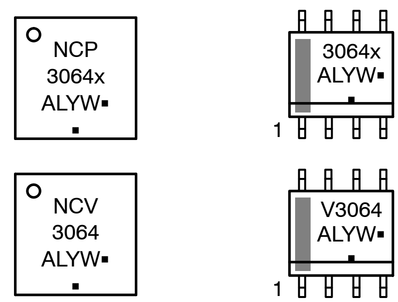


DFN8
MN SUFFIX
CASE 488AF



SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAMS



NCP3064/3064	=	Specific Device Code
x	=	B
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

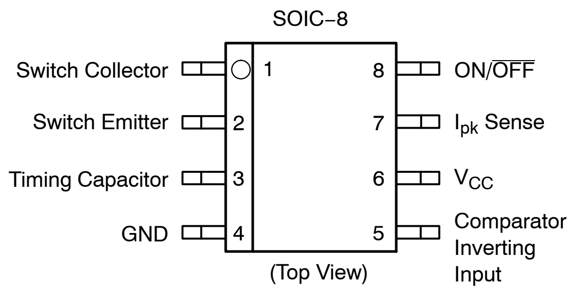
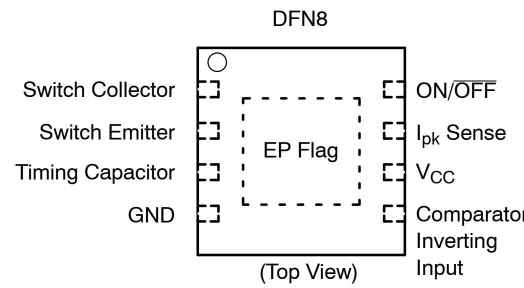


Figure 2. Pin Connections



NOTE: EP Flag must be tied to GND Pin 4 on PCB

Figure 3. Pin Connections

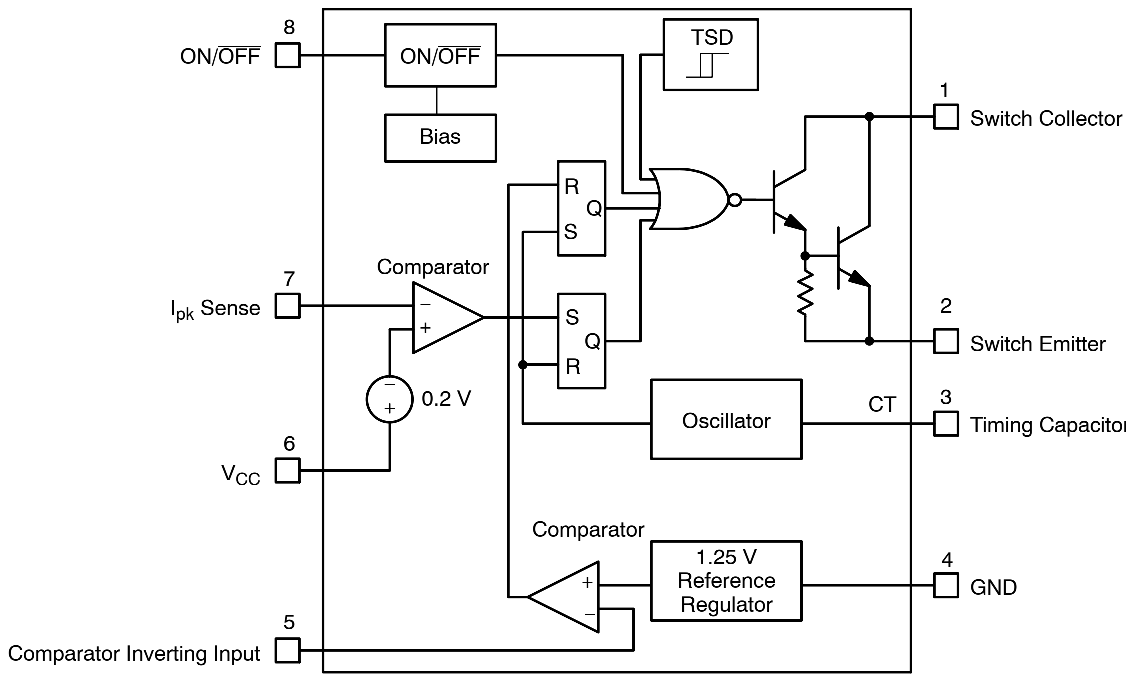


Figure 4. Block Diagram

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	Switch Collector	Internal Darlington switch collector
2	Switch Emitter	Internal Darlington switch emitter
3	Timing Capacitor	Timing Capacitor Oscillator Input, Timing Capacitor
4	GND	Ground pin for all internal circuits
5	Comparator Inverting Input	Inverting input pin of internal comparator
6	V_{CC}	Voltage supply
7	I_{pk} Sense	Peak Current Sense Input to monitor the voltage drop across an external resistor to limit the peak current through the circuit
8	ON/$\overline{\text{OFF}}$	ON/$\overline{\text{OFF}}$ Pin. Pulling this pin to High level turns the device in Operating. To switch into mode with low current consumption this pin has to be in Low level or floating.

MAXIMUM RATINGS (measured vs. Pin 4, unless otherwise noted)

Rating	Symbol	Value	Unit
V_{CC} (Pin 6)	V_{CC}	−0.3 to 42	V
Comparator Inverting Input (Pin 5)	V_{CII}	−0.3 to V_{CC}	V
Darlington Switch Emitter (Pin 2) (Transistor OFF)	V_{SWE}	−0.6 to V_{CC}	V
Darlington Switch Collector (Pin 1)	V_{SWC}	−0.3 to 42	V
Darlington Switch Collector to Emitter (Pins 1 and 2)	V_{SWCE}	−0.3 to 42	V
Darlington Switch Peak Current	I_{SW}	1.5	A
I_{pk} Sense Voltage (Pin 7)	V_{IPK}	−0.3 to (V_{CC} + 0.3 V)	V
Timing Capacitor Pin Voltage (Pin 3)	V_{TC}	−0.2 to +1.4	V
Moisture Sensitivity Level	MSL	1	
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions	T_{SLD}	260	°C
ON/$\overline{\text{OFF}}$ Pin Voltage	$V_{ON/\overline{OFF}}$	(−0.3 to 25) < V_{CC}	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTIC

Rating		Symbol	Value	Unit
SOIC−8 (Note 5)	Thermal Resistance Junction−to−Air Thermal Resistance Junction−to−Case	$R_{\theta JA}$ $R_{\theta JC}$	180 45	°C/W
DFN−8 (Note 5)	Thermal Resistance Junction−to−Air Thermal Resistance Junction−to−Case	$R_{\theta JA}$ $R_{\theta JC}$	78 14	°C/W
Storage temperature range		T_{STG}	−65 to +150	°C
Maximum junction temperature		$T_{J\ MAX}$	+150	°C
Operation Junction Temperature Range (Note 3)	NCP3064 NCP3064B, NCV3064	T_J	0 to +70 −40 to +125	°C

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1 through 8:
   Human Body Model 2000 V per AEC Q100−002; 003 or JESD22/A114; A115
   Machine Model Method 200 V
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. The relation between junction temperature, ambient temperature and Total Power dissipated in IC is $T_J = T_A + R_{\Theta} \cdot P_D$.
4. The pins which are not defined may not be loaded by external signals.
5. 1 oz copper, 1 in^2 copper area.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, −40°C < T_J < +125°C for NCP3064B and NCV3064, 0°C < T_J < +70°C for NCP3064 unless otherwise specified)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
OSCILLATOR						
f_{OSC}	Frequency	(V_{Pin} 5 = 0 V, CT = 2.2 nF, T_J = 25°C)	110	150	190	kHz
I_{DISCHG} / I_{CHG}	Discharge to Charge Current Ratio	(Pin 7 to V_{CC}, T_J = 25°C)	5.5	6.0	6.5	–
I_C	Capacitor Charging Current	(Pin 7 to V_{CC}, T_J = 25°C)	–	275	–	μA
I_{DISCH}	Capacitor Discharging Current	(Pin 7 to V_{CC}, T_J = 25°C)	–	1.65	–	mA
V_{IPK}	Current Limit Sense Voltage	(T_J = 25°C)	165	200	235	mV
OUTPUT SWITCH (Note 6)						
V_{SWCE}	Darlington Switch Collector to Emitter Voltage Drop	(I_{SW} = 1.0 A, T_J = 25°C) (Note 6)	–	1.0	1.3	V
$I_{C(OFF)}$	Collector Off−State Current	(V_{CE} = 40 V)	–	1.0	10	μA
COMPARATOR						
V_{TH}	Threshold Voltage	T_J = 25°C	–	1.25	–	V
		NCP3064	−1.5	–	+1.5	%
		NCP3064B, NCV3064	−1.5	–	+1.5	%
REG_{LiNE}	Threshold Voltage Line Regulation	(V_{CC} = 3.0 V to 40 V)	−6.0	2.0	6.0	mV
$I_{CII\ in}$	Input Bias Current	(V_{in} = V_{th})	−1000	−100	1000	nA
ON/OFF FEATURE						
V_{IH}	ON/$\overline{\text{OFF}}$ Pin Logic Input Level High V_{OUT} = Nominal Output Voltage	T_J = 25°C T_J = −40°C to +125°C	2.2 2.4	– –	– –	V
V_{IL}	ON/$\overline{\text{OFF}}$ Pin Logic Input Level Low V_{OUT} = 0 V	T_J = 25°C T_J = −40°C to +125°C	– –	– –	1.0 0.8	V
I_{IH}	ON/$\overline{\text{OFF}}$ Pin Input Current ON/$\overline{\text{OFF}}$ Pin = 5 V (ON)	T_J = 25°C	–	15	–	μA
I_{IL}	ON/$\overline{\text{OFF}}$ Pin Input Current ON/$\overline{\text{OFF}}$ Pin = 0 V (OFF)	T_J = 25°C	–	1.0	–	μA
TOTAL DEVICE						
I_{CC}	Supply Current	(V_{CC} = 5.0 V to 40 V, CT = 2.2 nF, Pin 7 = V_{CC}, V_{Pin} 5 > V_{th}, Pin 2 = GND, remaining pins open)	–	–	7.0	mA
I_{STBY}	Standby Quiescent Current	ON/$\overline{\text{OFF}}$ Pin = 0 V (OFF) T_J = 25°C T_J = −40°C to +125°C	 – –	 85 –	 100 100	μA
T_{SHD}	Thermal Shutdown Threshold		–	160	–	°C
T_{SHDHYS}	Hysteresis		–	10	–	°C

6. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
7. The V_{IPK} (Sense) Current Limit Sense Voltage is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope. See the Operating Description section for details.

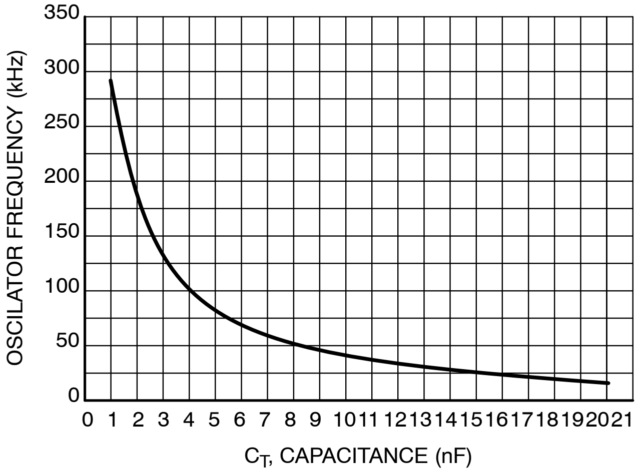


Figure 5. Oscillator Frequency vs. Timing Capacitor C_T

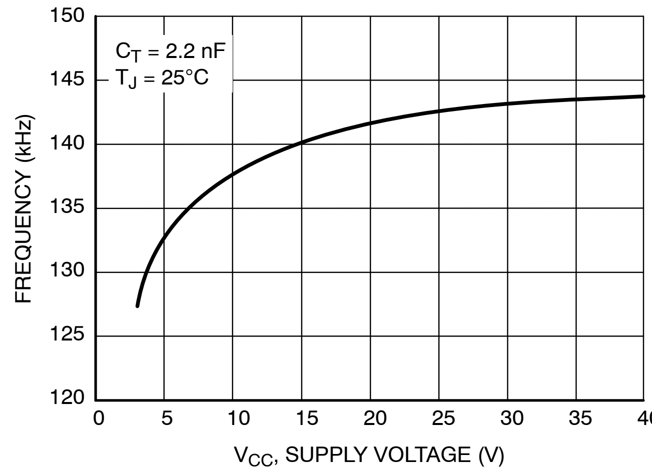


Figure 6. Oscillator Frequency vs. Supply Voltage

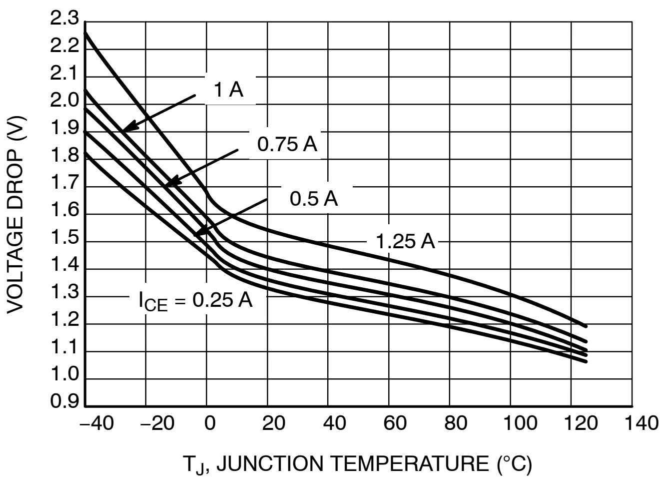


Figure 7. Emitter Follower Configuration Output Darlington Switch Voltage Drop vs. Temperature

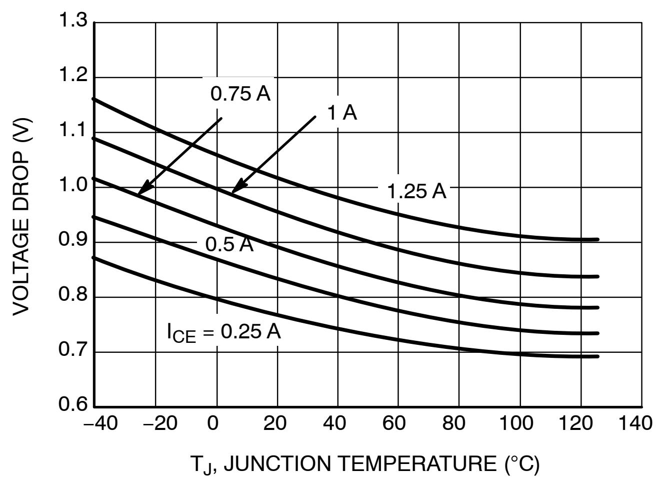


Figure 8. Common Emmitter Configuration Outp Darlington Switch Voltage Drop vs. Temperatur

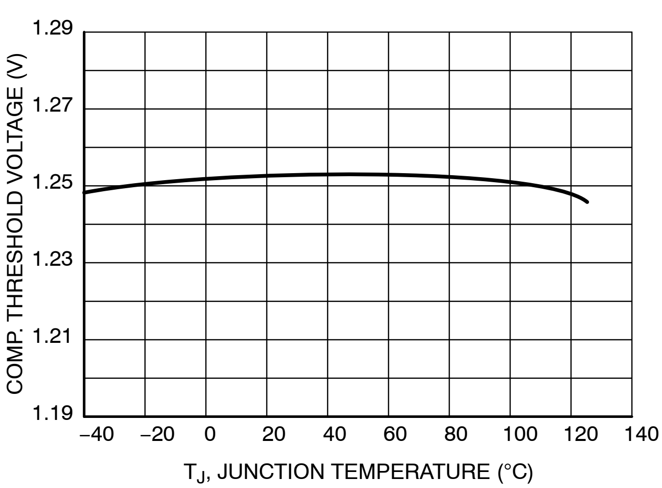


Figure 9. Comparator Threshold Voltage vs. Temperature

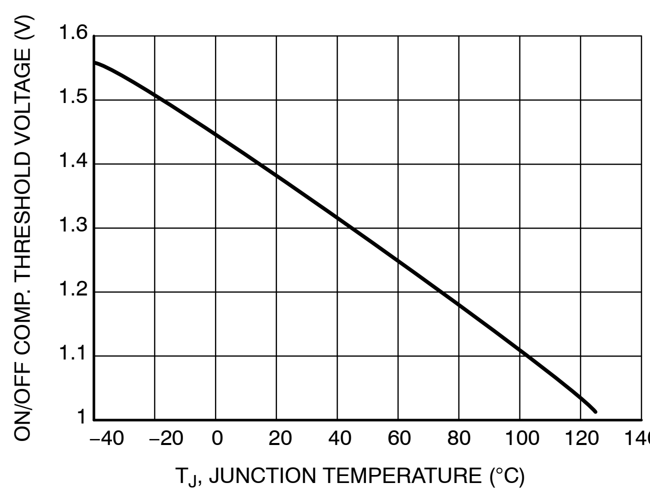


Figure 10. ON/OFF Comparator Threshold Voltage vs. Temperature

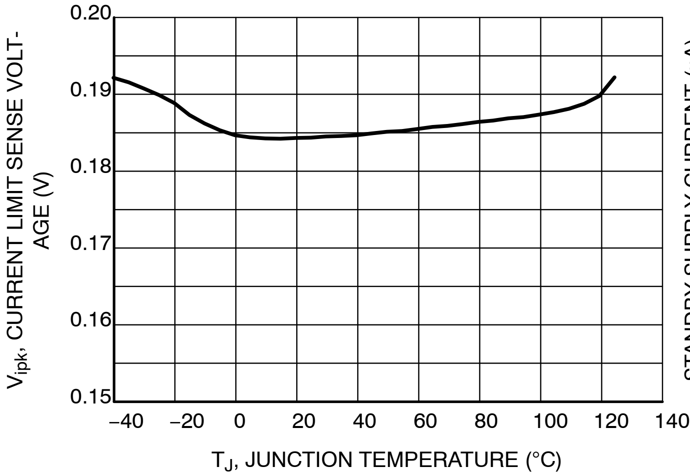


Figure 11. Current Limit Sense Voltage vs. Temperature

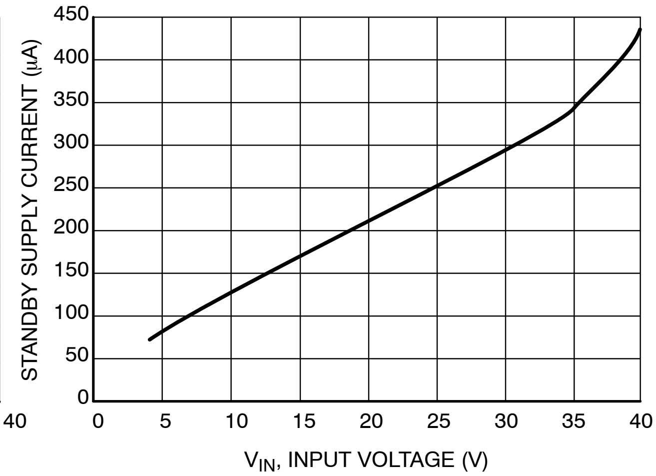


Figure 12. Standby Current vs. Supply Voltage

INTRODUCTION

The NCP3064 is a monolithic power switching regulator optimized for dc to dc converter applications. The combination of its features enables the system designer to directly implement step−up, step−down, and voltage−inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for industrial markets. A representative block diagram is shown in Figure 4.

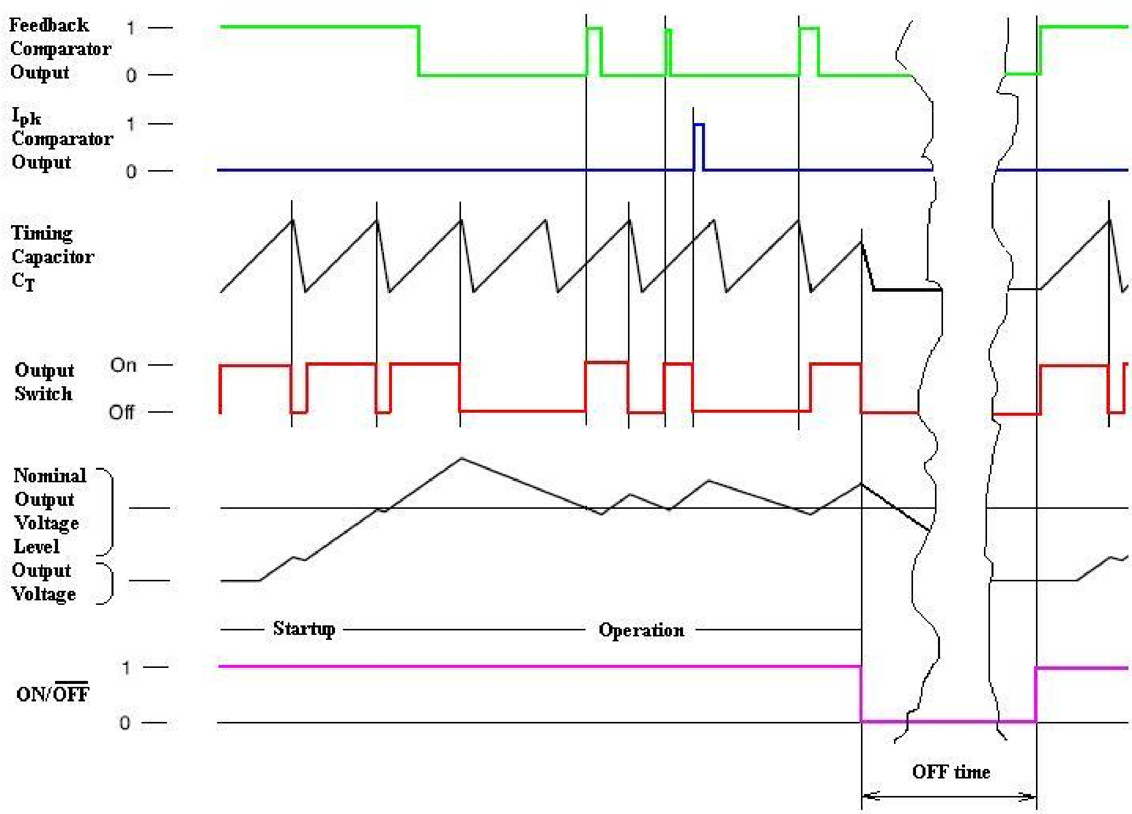
Operating Description

The NCP3064 is a hysteric, dc−dc converter that uses a gated oscillator to regulate output voltage. In general, this mode of operation is some what analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 13. The output voltage waveform shown is for a step−down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the output switch next cycle turning on is inhibited. The feedback comparator will enable the switching immediately when the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be enabled for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and off−time of the output switch are programmed by the value selected for the timing capacitor C_T. Capacitor C_T is charged and discharged by a 1 to 6 ratio internal current source and sink, generating a positive going sawtooth waveform at Pin 3. This ratio sets the maximum $t_{ON}/(t_{ON} + t_{OFF})$ of the switching converter as 6/(6 + 1) or 0.857 (typical).

The oscillator peak and valley voltage difference is 500 mV typically. To calculate the C_T capacitor value for the required oscillator frequency, use the equation found in Figure 15. An Excel® based design tool can be found at www.onsemi.com on the NCP3064 product page.



Peak Current Sense Comparator

With a voltage ripple gated converter operating under normal conditions, output switch conduction is initiated by the Voltage Feedback comparator and terminated by the oscillator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Ipk Current Sense comparator will protect the Darlington output Switch. The switch current is converted to a voltage by inserting a fractional Ω resistor, R_{SC}, in series with V_{CC} and the Darlington output switch. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 200 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle−by−cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on−time during a given oscillator cycle.

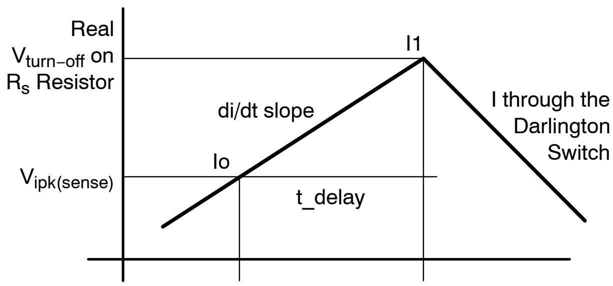


Figure 14. Current Sense Waveform

The $V_{IPK(Sense)}$ Current Limit Sense Voltage threshold is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope.

Real $V_{turn-off}$ on R_{sc} resistor

$V_{turn\_off} = V_{ipk(sense)} + R_s*(t_{delay}*di/dt)$

Typical I_{pk} comparator response time t_{delay} is 350 ns. The di/dt current slope is growing with voltage difference on the inductor pins and with decreasing inductor value. It is recommended to check the real max peak current in the application at worst conditions to be sure that the maximum peak current will never get over the 1.5 A Darlington Switch Current maximum rating.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the Output Switch is disabled. The temperature sensing circuit is designed with 10°C hysteresis. The Switch is enabled again when the chip temperature decreases to at least 150°C threshold. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heat−sinking.

Output Switch

The output switch is designed in a Darlington configuration. This allows the application designer to operate at all conditions at high switching speed and low voltage drop. The Darlington Output Switch is designed to switch a maximum of 40 V collector to emitter voltage and current up to 1.5 A

ON/$\overline{\text{OFF}}$ Function

The ON/$\overline{\text{OFF}}$ function disables switching and puts the part into a low power consumption mode. A PWM signal up to 1 kHz can be used to pulse the ON/$\overline{\text{OFF}}$ and control the output. Pulling this pin below the threshold voltage (~1.4 V) or leaving it open turns the regulator off and has a standby current <100 μA. Pulling this pin above 1.4 V (up to 25 V max) allows the regulator to run in normal operation. If the ON/$\overline{\text{OFF}}$ feature is not needed, the ON/$\overline{\text{OFF}}$ pin can be connected to the input voltage V_{CC}, provided that this voltage does not exceed 25 V.

APPLICATIONS

Figures 16, 20 and 24 show the simplicity and flexibility of the NCP3064. Two main converter topologies are demonstrated with actual test data shown below the circuit diagrams.

Figure 15 gives the relevant design equations for the key parameters. Additionally, a complete application design aid for the NCP3064 can be found at www.onsemi.com.

It is possible to create applications with external transistors. This solution helps to increase output current and helps with efficiency, still keeping the cost of materials low. Another advantage of using the external transistor is higher operating frequency, which can go up to 250 kHz. Smaller size of the output components such as inductor and capacitor can be used then.

(See Notes 8, 9, 10)	Step−Down	Step−Up	Voltage−Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in} - V_{SWCE} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{SWCE}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{SWCE}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$C_T = \frac{381.6 \cdot 10^{-6}}{f_{osc}} - 343 \cdot 10^{-12}$		
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk\ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.20}{I_{pk\ (Switch)}}$	$\frac{0.20}{I_{pk\ (Switch)}}$	$\frac{0.20}{I_{pk\ (Switch)}}$
L	$\left(\frac{V_{in} - V_{SWCE} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{SWCE}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{SWCE}}{\Delta I_L}\right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on} I_{out}}{C_O} + \Delta I_L \cdot ESR$	$\approx \frac{t_{on} I_{out}}{C_O} + \Delta I_L \cdot ESR$
V_{out}	$V_{TH}\left(\frac{R1}{R2} + 1\right)$	$V_{TH}\left(\frac{R1}{R2} + 1\right)$	$V_{TH}\left(\frac{R1}{R2} + 1\right)$

8. V_{SWCE} − Darlington Switch Collector to Emitter Voltage Drop, refer to Figures 7, 5, 8 and 9.
9. V_F − Output rectifier forward voltage drop. Typical value for 1N5819 Schottky barrier rectifier is 0.4 V.
10. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio.

Figure 15. Design Equations

The Following Converter Characteristics Must Be Chosen:

V_{in} − Nominal operating input voltage.

V_{out} − Desired output voltage.

I_{out} − Desired output current.

ΔI_L − Desired peak−to−peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\ (Switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.

f − Maximum output switch frequency.

$V_{ripple(pp)}$ − Desired peak−to−peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

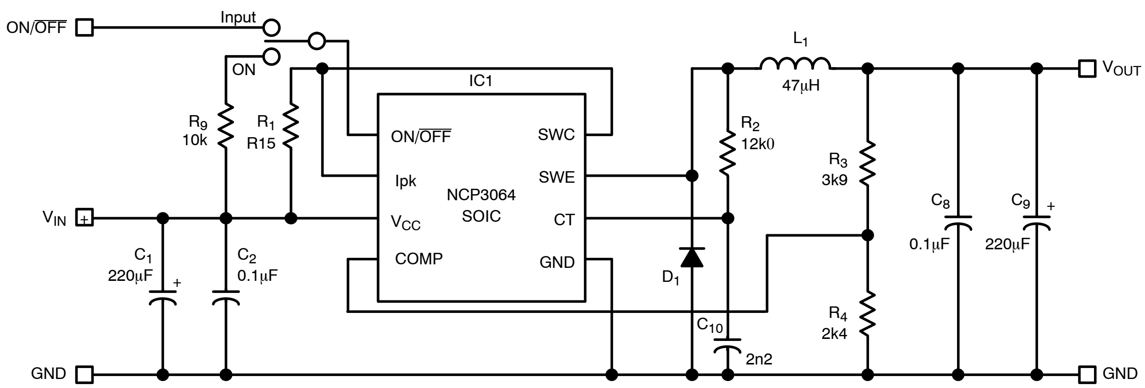


Figure 16. Typical Buck Application Schematic

Table 1. TESTED PARAMETERS

Parameter	Input Voltage (V)	Output Voltage (V)	Input Current (A)	Output Current (A)
Value	10 – 16	3.3	Max. 0.6 A	Max. 1.25

Table 2. BILL OF MATERIAL

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
R1	1	Resistor	0.15Ω	1%	1206	Susumu	RL1632R-R150-F
R2	1	Resistor	12k	1%	1206	ROHM	MCR18EZHF1202
R3	1	Resistor	3k9	1%	1206	ROHM	MCR18EZHF3901
R4	1	Resistor	2k4	1%	1206	ROHM	MCR18EZHF4701
R9	1	Resisitor	10k	1%	1206	ROHM	MCR18EZHF1002
C1	1	Capacitor	220µF/35V	20%	F	PANASONIC	EEEFP1V221AP
C2, C8	2	Capacitor	100nF	10%	1206	Kemet	C1206C104K5RACTU
C9	1	Capacitor	220µF/6V	20%	F8	SANYO	6SVP220M
C10	1	Capacitor	2.2nF	10%	1206	Kemet	C1206C222K5RACTU
L1	1	Inductor	47µH	20%	DO3316	CoilCraft	DO3316P-473MLB
D1	1	Diode	MBRS230	–	SMB	ON Semiconductor	MBRS230LT3G
IC	1	Switching Regulator	NCP3064	–	SOIC8	ON Semiconductor	NCP3064DR2G

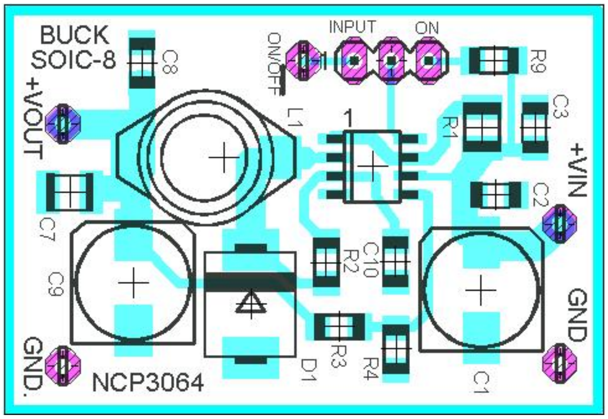


Figure 17. Buck Demoboard Layout

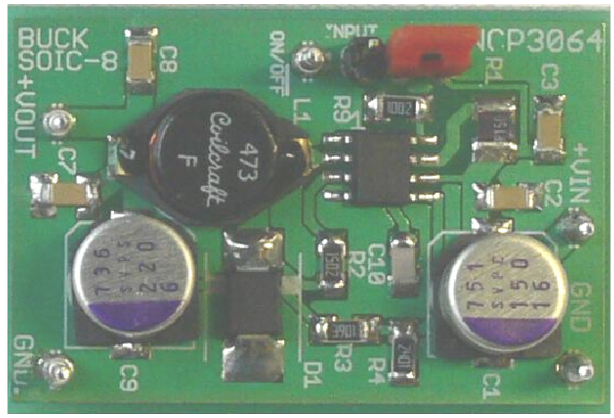


Figure 18. Buck Demoboard Photo

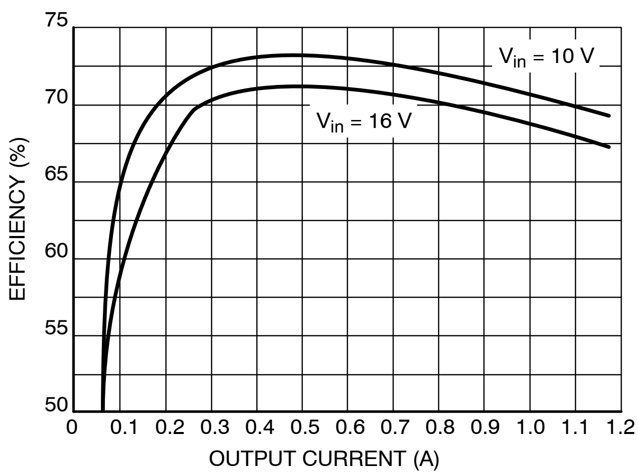


Figure 19. Efficiency vs. Output Current for Buck Demoboard

Table 3. TEST RESULTS

Line Regulation	V_{in} = 9 V to 12 V, V_{out} = 3.3 V, I_{out} = 800 mA	8 mV
Load Regulation	V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 800 mA	10 mV
Output Ripple	V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 100 mA to 800 mA	< 85 mV Peak - Peak
Efficiency	V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 500 mA	70%

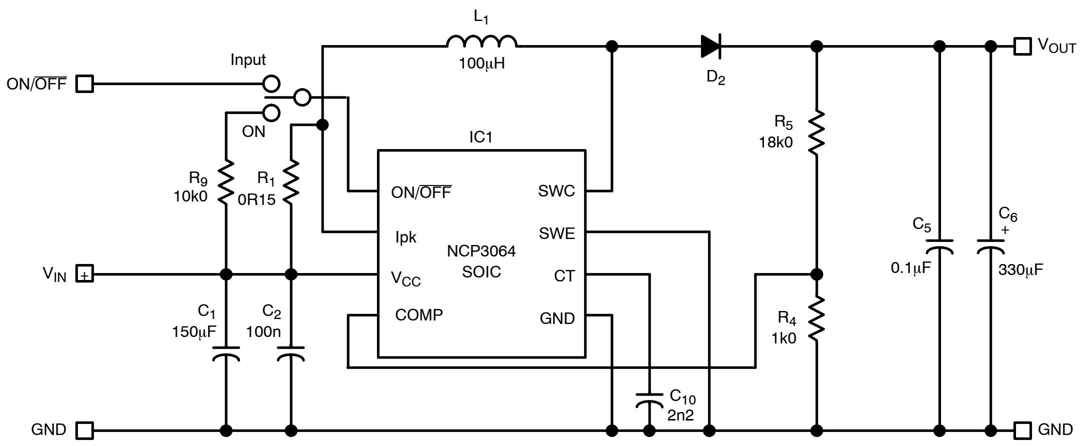


Figure 20. Typical Boost Application Schematic

Table 4. TESTED PARAMETERS

Parameter	Input Voltage (V)	Output Voltage (V)	Input Current (A)	Output Current (A)
Value	10 – 16	24	Max. 1.25	Max. 0.6

Table 5. BILL OF MATERIAL

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
R1	1	Resistor	0.15Ω	1%	1206	Susumu	RL1632R-R150-F
R5	1	Resistor	18k	1%	1206	ROHM	MCR18EZHF1802
R6	1	Resistor	1k	1%	1206	ROHM	MCR18EZHF1001
R9	1	Resisitor	10k	1%	1206	ROHM	MCR18EZHF1002
C1	1	Capacitor	150µF/16V	20%	F8	SANYO	6SVP150M
C2, C5	2	Capacitor	100nF	10%	1206	Kemet	C1206C104K5RACTU
C6	1	Capacitor	330µF/25V	20%	SMD	Panasonic	EEE-FK1E331GP
C10	1	Capacitor	2.2nF	10%	1206	Kemet	C1206C222K5RACTU
L2	1	Inductor	100µH	20%	DO3316	CoilCraft	DO3316P-104MLB
D2	1	Diode	MBRS230	–	SMB	ON Semiconductor	MBRS230LT3G
IC	1	Switching Regulator	NCP3064	–	SOIC8	ON Semiconductor	NCP3064DR2G

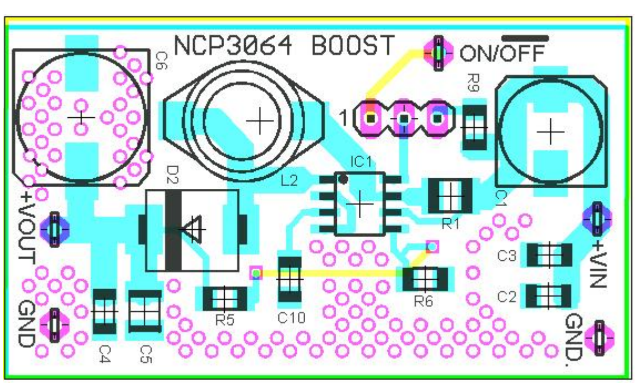


Figure 21. Boost Demoboard Layout

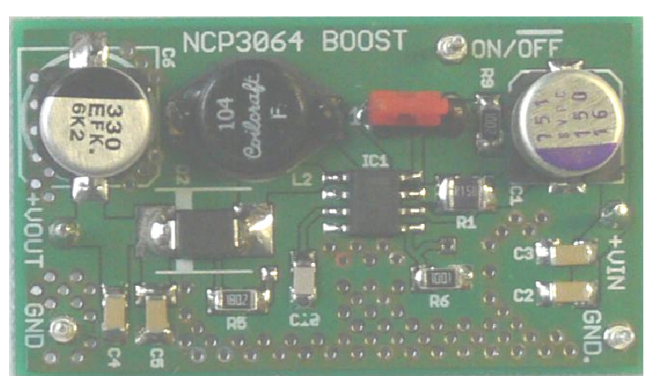


Figure 22. Boost Demoboard Photo

Table 6. TEST RESULTS

Line Regulation	V_{in} = 9 V to 15 V, V_{out} = 24 V, I_{out} = 250 mA	3 mV
Load Regulation	V_{in} = 12 V, V_{out} = 24 V, I_{out} = 50 to 350 mA	5 mV
Output Ripple	V_{in} = 12 V, V_{out} = 24 V, I_{out} = 50 to 350 mA	< 350 mV Peak - Peak
Efficiency	V_{in} = 12 V, V_{out} = 24 V, I_{out} = 200 mA	86%

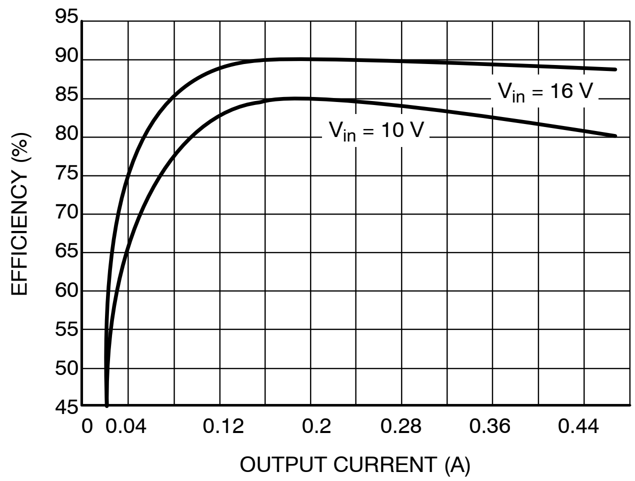


Figure 23. Efficiency vs. Output Current Current for Boost Demoboard

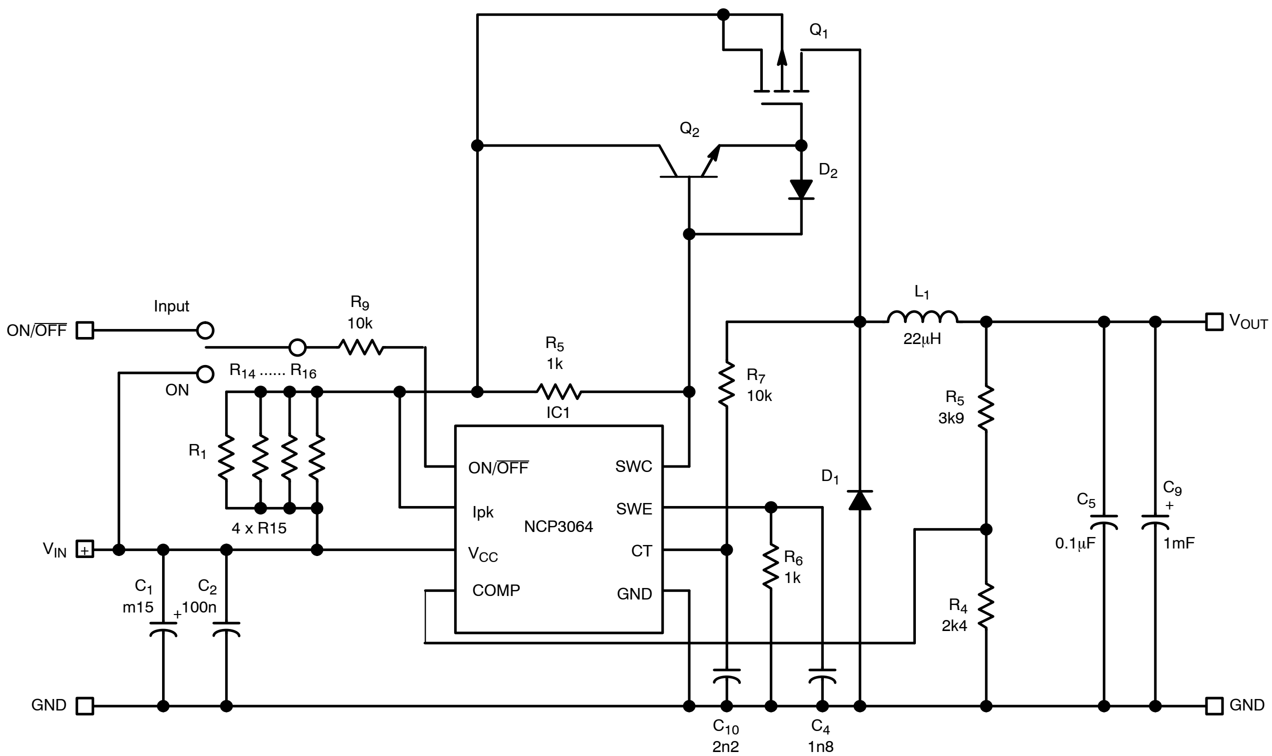


Figure 24. Typical Buck with External Transistor Application Schematic

Table 7. TESTED PARAMETERS

Parameter	Input Voltage (V)	Output Voltage (V)	Input Current (A)	Output Current (A)
Value	10 – 16	3.3	Max. 1.25	Max. 3

Table 8. BILL OF MATERIAL

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
R1, R14, R15, R16	4	Resistor	0.15R	1%	1206	Susumu	RL1632R-R150-F
R5, R6	2	Resistor	1k	1%	1206	ROHM	MCR18EZHF1001
R3	1	Resistor	3k9	1%	1206	ROHM	MCR18EZHF3901
R4	1	Resistor	2k4	1%	1206	ROHM	MCR18EZHF2401
R7;R9	2	Resistor	10k	1%	1206	ROHM	MCR18EZHF1002
C1	1	Capacitor	270μF	20%	10 x 16	PANASONIC	EEUFC1V271
C4	1	Capacitor	1n8	10%	1206	Kemet	C1206C182K5RACTU
C2, C8	2	Capacitor	100nF	10%	1206	Kemet	C1206C104K5RACTU
C9	1	Capacitor	1mF	20%	F8	SANYO	4SA1000M
C10	1	Capacitor	2.2nF	10%	1206	Kemet	C1206C222K5RACTU
Q1	1	Transistor	MMSF7P03	–	SOIC8	ON Semiconductor	MMSF7P03HDR2G
Q2	1	Transistor NPN	MMBT489L	–	SOT-23	ON Semiconductor	MMBT489LT1G
D2	1	Diode	MBR130T	–	SOD-123	ON Semiconductor	MBR130T1G
IC1	1	Switching Regulator	NCP3064	–	SOIC8	ON Semiconductor	NCP3064DR2G
D1	1	Diode	MBRS330T	–	SMC	ON Semiconductor	MBRS330T3G
L1	1	Inductor	22μH	20%	Coilcraft	Coilcraft	DO5040H-223MLB

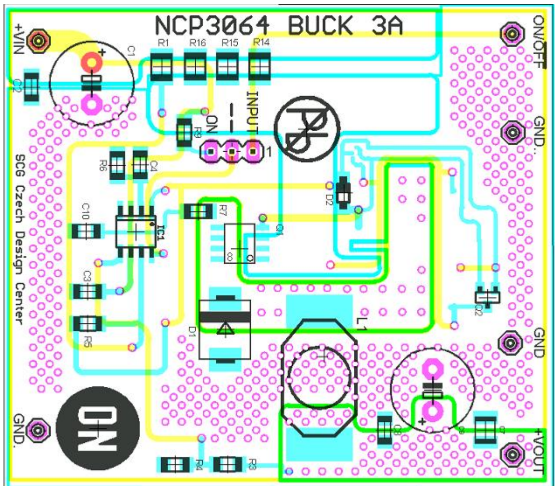


Figure 25. Buck Demoboard with External PMOS Transistor Layout

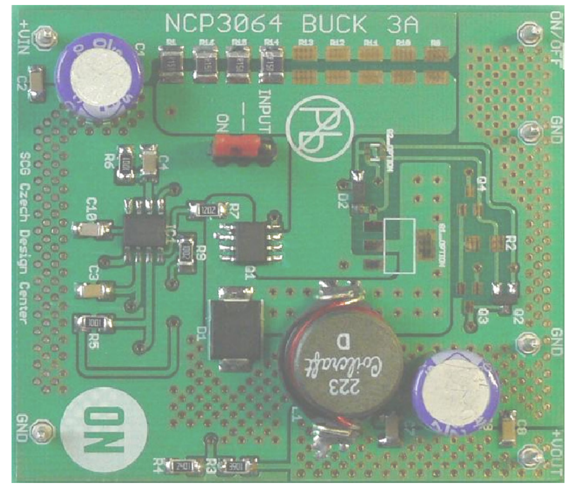


Figure 26. Buck Demoboard with External PMOS Transistor Photo

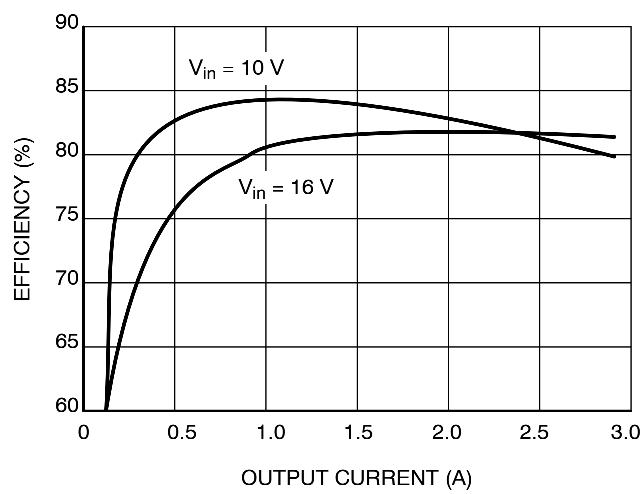


Figure 27. Efficiency vs. Output Current Current for Buck Demoboard with External PMOS Transistor

Table 9. TEST RESULTS

Line Regulation	V_{in} = 9 V to 15 V, V_{out} = 3.3 V, I_{out} = 2 A	8 mV
Load Regulation	V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 0.5 to 3.0 A	10 mV
Output Ripple	V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 0.5 to 3.0 A	< 300 mV Peak - Peak
Efficiency	V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 2 A	82%

The picture in Figure 24. Typical Buck Application Schematic shows typical configuration with external PMOS transistor. Resistor R7 connected between timing capacitor TC Pin and SWE Pin provides a pulse feedback voltage. The pulse feedback approach increases the operating ffrequency by up to 50%. Figure 28, Oscillator Frequency vs. Timing Capacitor with Pulse Feedback, shows the impact to the oscillator frequency at buck converter for V_{in} = 12 V and V_{out} = 3.3 V with pulse feedback resistor R_7 = 10 kΩ. It also creates more regular switching waveforms with constant operating frequency which results in lower ripple voltage and improved efficiency.

If the application allows ON/$\overline{\text{OFF}}$ pin to be biased by voltage and the power supply is not connected to Vcc pin at the same time, then it is recommended to limit ON/$\overline{\text{OFF}}$ current by resistor with value 10 kΩ to protect the NCP3064 device. This situation is mentioned in Figure 29, ON/$\overline{\text{OFF}}$ Serial Resistor Connection.

This resistor shifts the ON/$\overline{\text{OFF}}$ threshold by about 200 mV to higher value, but the TTL logic compatibility is kept in full range of input voltage and operating temperature range.

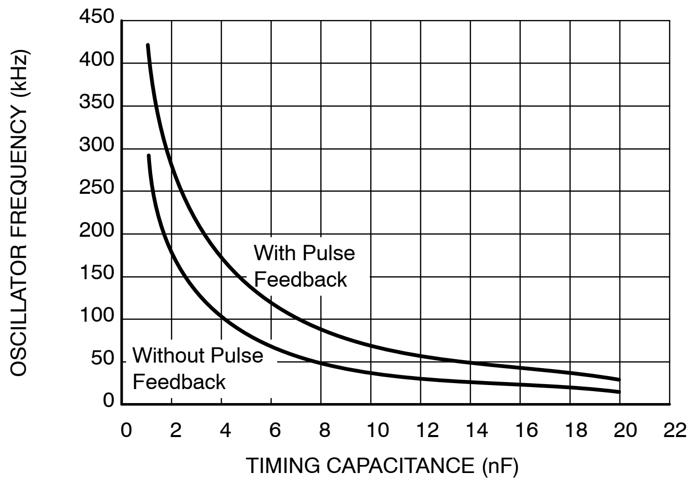


Figure 28. Oscillator Frequency vs. Timing Capacitor with Pulse Feedback

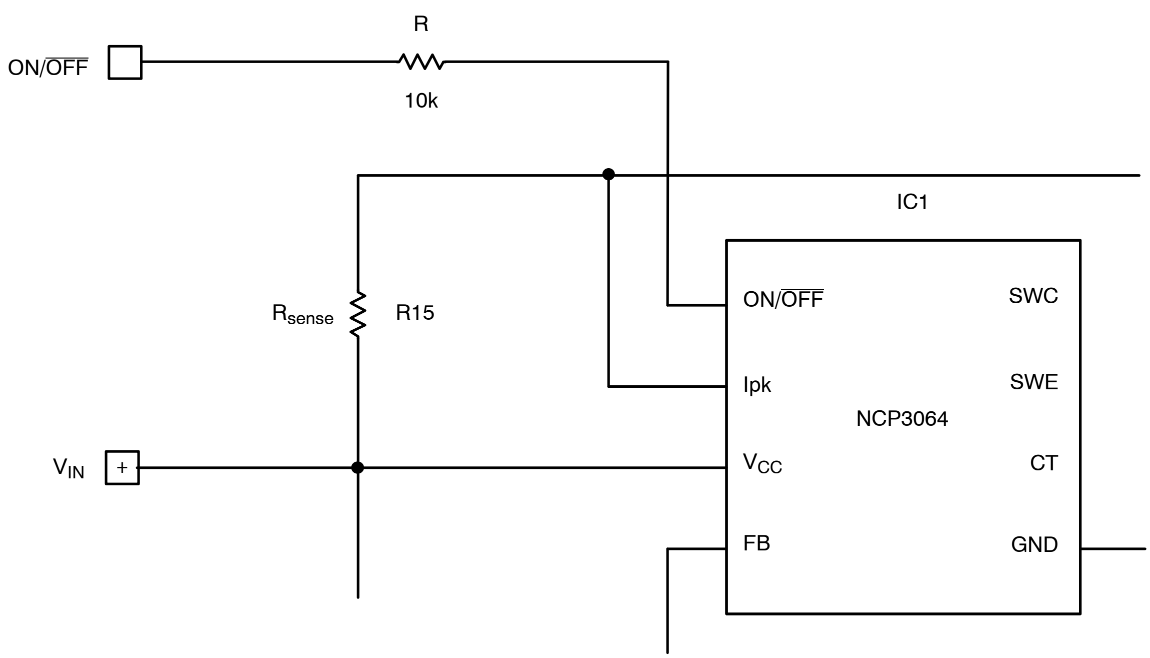
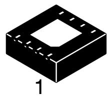


Figure 29. ON/$\overline{\text{OFF}}$ Serial Resistor Connection

ORDERING INFORMATION

Device	Package	Shipping†
NCP3064MNTXG	DFN−8 (Pb−Free)	4000 Units / Tape & Reel
NCP3064BMNTXG	DFN−8 (Pb−Free)	4000 Units / Tape & Reel
NCP3064DR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCP3064BDR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCV3064MNTXG*	DFN−8 (Pb−Free)	4000 Units / Tape & Reel
NCV3064DR2G*	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel

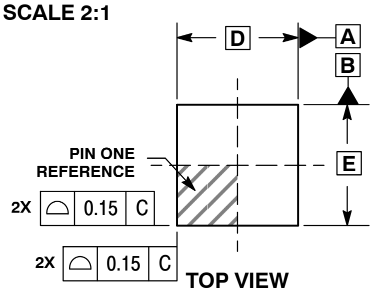
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements.



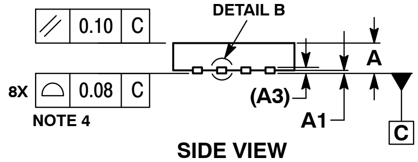
SCALE 2:1

DFN8, 4x4
CASE 488AF
ISSUE C

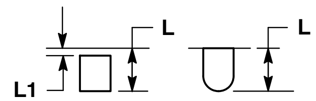
DATE 15 JAN 2009



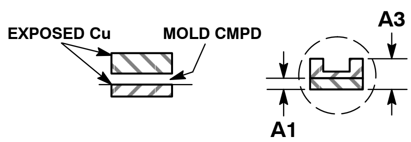
TOP VIEW



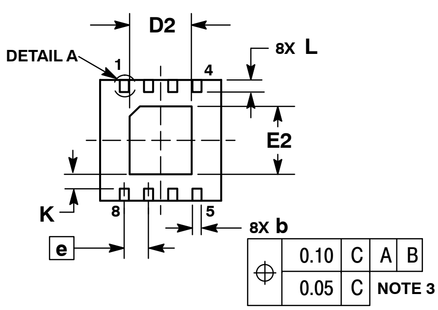
SIDE VIEW



DETAIL A
OPTIONAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

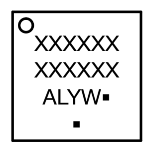


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

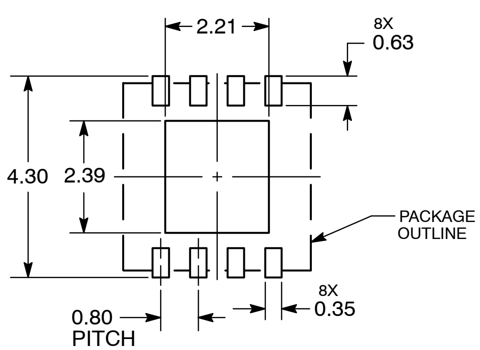
GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

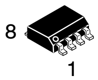
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

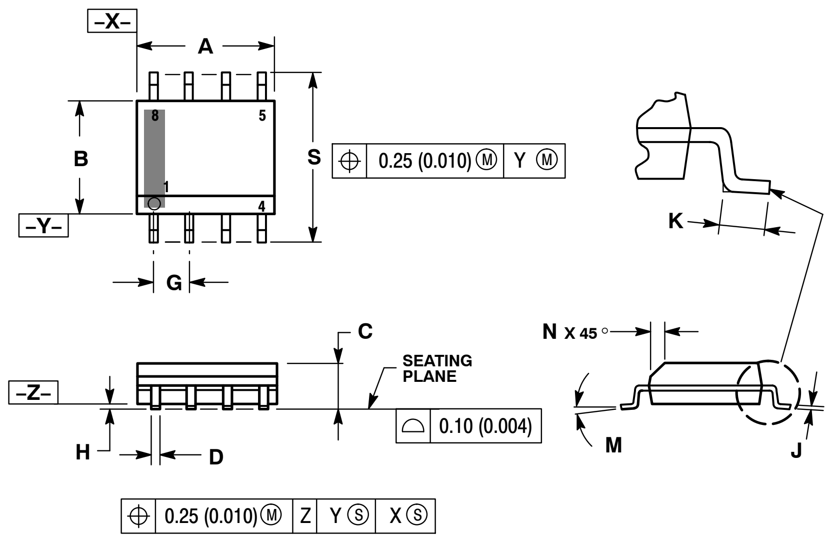
DOCUMENT NUMBER:	98AON15232D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DFN8, 4X4, 0.8P	PAGE 1 OF 1



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

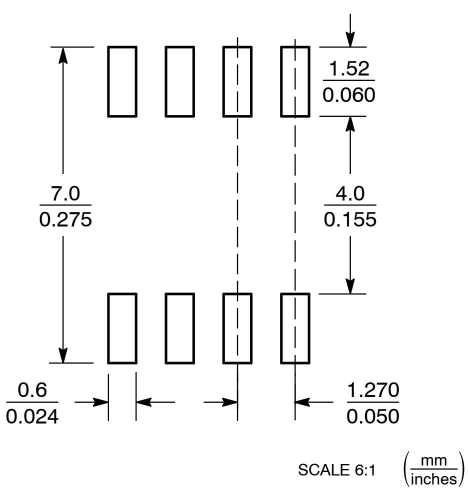
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

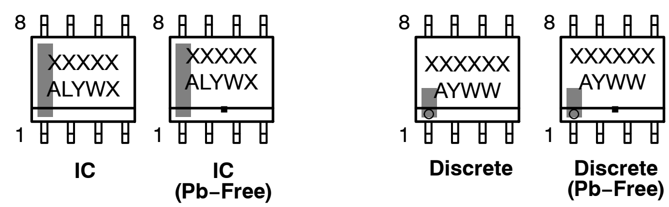
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 2 OF 2**

ADDITIONAL INFORMATION