

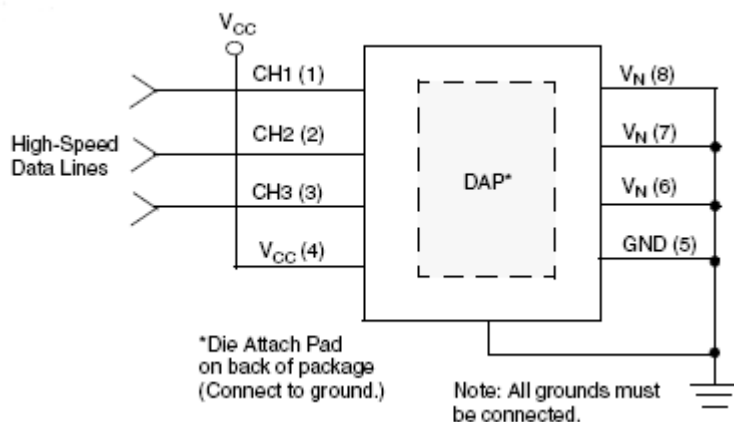
# CM1241

## 4-Channel Low Capacitance Dual-Voltage ESD Protection Array

### Features

- 3 Channels of Low Voltage ESD Protection
- 1 Channel of High Voltage ESD Protection
- Provides ESD Protection to IEC61000-4-2 Level 4:  
±8 kV Contact Discharge (Pins 1-3)  
±15 kV Contact Discharge (Pin 4)
- Low Channel Input Capacitance
- Minimal Capacitance Change with Temperature and Voltage
- High Voltage Zener Diode Protects Supply Rail
- No Need for External Bypass Capacitors
- Each I/O Pin Can Withstand Over 1000 ESD Strikes\*
- These Devices are Pb-Free and are RoHS Compliant

### TYPICAL APPLICATION



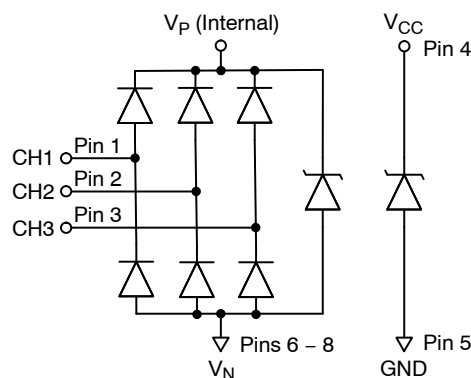
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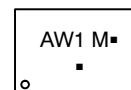


WDFN-8  
D4 SUFFIX  
CASE 511BF

### BLOCK DIAGRAM



### MARKING DIAGRAM



AW1 = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device      | Package          | Shipping†        |
|-------------|------------------|------------------|
| CM1241-04D4 | WDFN-8 (Pb-Free) | 3000/Tape & Reel |

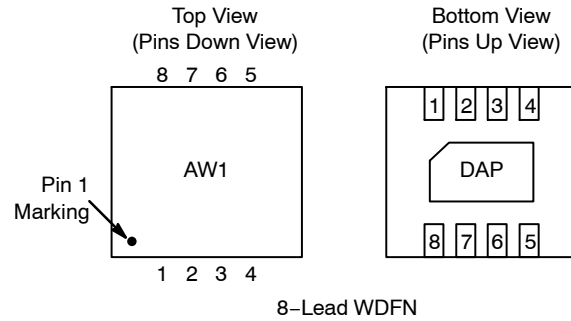
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

\*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

Table 1. PIN DESCRIPTIONS

| 4-Channel, 8-Lead, WDFN-8 Package |                 |                    |                                |
|-----------------------------------|-----------------|--------------------|--------------------------------|
| Pin                               | Name            | Type               | Description                    |
| 1                                 | CH1             | I/O                | LV Low-capacitance ESD Channel |
| 2                                 | CH2             | I/O                | LV Low-capacitance ESD Channel |
| 3                                 | CH3             | I/O                | LV Low-capacitance ESD Channel |
| 4                                 | V <sub>CC</sub> | HV V <sub>DD</sub> | HV ESD Channel                 |
| 5                                 | GND             |                    | Ground                         |
| 6                                 | V <sub>N</sub>  |                    | Negative Voltage Supply Rail   |
| 7                                 | V <sub>N</sub>  |                    | Negative Voltage Supply Rail   |
| 8                                 | V <sub>N</sub>  |                    | Negative Voltage Supply Rail   |
| DAP                               | GND             |                    | Die Attach Pad (Ground)        |

PACKAGE / PINOUT DIAGRAMS



## SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameter                                             | Rating      | Units |
|-------------------------------------------------------|-------------|-------|
| DC Voltage on Low-voltage Pins                        | 6.0         | V     |
| DC Voltage on High-voltage Pins (V <sub>CC</sub> pin) | 14.5        | V     |
| Operating Temperature Range                           | -40 to +85  | °C    |
| Storage Temperature Range                             | -65 to +150 | °C    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

| Parameter                   | Rating     | Units |
|-----------------------------|------------|-------|
| Operating Temperature Range | -40 to +85 | °C    |

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note1)

| Symbol          | Parameter                                                                                                                                                  | Conditions                                                                                          | Min                                   | Typ                          | Max  | Units         |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|---------------------------------------|------------------------------|------|---------------|
| $V_F$           | LV Diode Reverse Voltage<br>(Positive Voltage)                                                                                                             | $I_F = 10 \text{ mA}$ ; $T_A = 25^\circ\text{C}$                                                    | 6.8                                   | 8.2                          | 9.2  | V             |
|                 | LV Diode Forward Voltage<br>(Negative Voltage)                                                                                                             | $I_F = 10 \text{ mA}$ ; $T_A = 25^\circ\text{C}$                                                    | -1.05                                 | -0.9                         | -0.6 | V             |
| $I_{LEAK}$      | LV Channel Leakage Current<br>(Pins 1 and 2)                                                                                                               | $T_A = -30^\circ\text{C}$ to $65^\circ\text{C}$ ; $V_{IN} = 3.3 \text{ V}$ ,<br>$V_N = 0 \text{ V}$ |                                       |                              | 100  | nA            |
|                 | LV Channel Leakage Current<br>(Pin 3 only)                                                                                                                 | $T_A = -30^\circ\text{C}$ to $65^\circ\text{C}$ ; $V_{IN} = 3.3 \text{ V}$ ,<br>$V_N = 0 \text{ V}$ |                                       |                              | 100  | nA            |
| $C_{IN}$        | LV Channel Input Capacitance                                                                                                                               | At 1 MHz, $V_N = 0 \text{ V}$ , $V_{IN} = 1.65 \text{ V}$                                           |                                       | 1.2                          | 1.5  | pF            |
| $\Delta C_{IN}$ | LV Channel Input Capacitance<br>Matching                                                                                                                   | At 1 MHz, $V_N = 0 \text{ V}$ , $V_{IN} = 1.65 \text{ V}$                                           |                                       | 0.02                         |      | pF            |
| $I_{LEAK\_HV}$  | HV Channel Leakage Current                                                                                                                                 | $T_A = 25^\circ\text{C}$ ; $V_{CC} = 11 \text{ V}$ , $V_N = 0 \text{ V}$                            |                                       | 0.1                          | 1.0  | $\mu\text{A}$ |
| $C_{IN\_HV}$    | HV Channel Input Capacitance                                                                                                                               | At 1 MHz, $V_N = 0 \text{ V}$ , $V_{IN} = 2.5 \text{ V}$                                            |                                       | 53                           |      | pF            |
| $V_{F\_HV}$     | HV Diode Breakdown Voltage<br>Positive Voltage                                                                                                             | $I_F = 10 \text{ mA}$ ; $T_A = 25^\circ\text{C}$                                                    | 14.6                                  |                              | 17.7 | V             |
| $V_{ESD}$       | ESD Protection<br>Peak Discharge Voltage at any<br>channel input, in system<br>Contact discharge per<br>IEC 61000-4-2 standard                             | $T_A = 25^\circ\text{C}$                                                                            | $\pm 8$ (Pin 1-3)<br>$\pm 15$ (Pin 4) |                              |      | kV            |
| $V_{CL}$        | LV Channel Clamp Voltage (Pin 1-3)<br>Positive Transients<br>Negative Transients                                                                           | $T_A = 25^\circ\text{C}$ , $I_{PP} = 1 \text{ A}$ , $t_P = 8/20 \mu\text{S}$                        |                                       | +9.64<br>-1.75               |      | V             |
| $R_{DYN}$       | Dynamic Resistance<br>LV Channel Positive Transients<br>LV Channel Negative Transients<br>HV Channel Positive Transients<br>HV Channel Negative Transients | $I_{PP} = 1 \text{ A}$ , $t_P = 8/20 \mu\text{S}$<br>Any I/O pin to Ground                          |                                       | 0.72<br>0.59<br>1.20<br>0.36 |      | $\Omega$      |

1. All parameters specified at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.

## PERFORMANCE INFORMATION

## Input Channel Capacitance Performance Curves for Low Voltage Pins

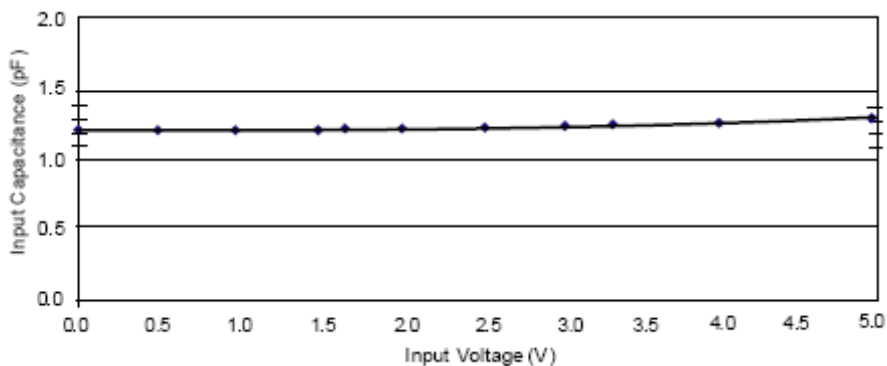


Figure 1. Typical Variation of  $C_{IN}$  vs.  $V_{IN}$   
(Low Voltage Inputs,  $f = 1$  MHz,  $V_N = 0$  V)

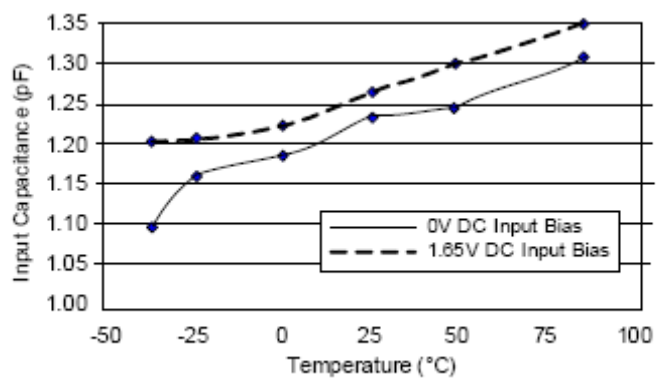


Figure 2. Typical Variation of  $C_{IN}$  vs. Temp  
(Low Voltage Inputs,  $f = 1$  MHz,  $V_N = 0$  V)

## PERFORMANCE INFORMATION (Cont'd)

## Typical Filter Performance for Low Voltage Pins

Nominal conditions unless specified; otherwise, 50  $\Omega$  environment.

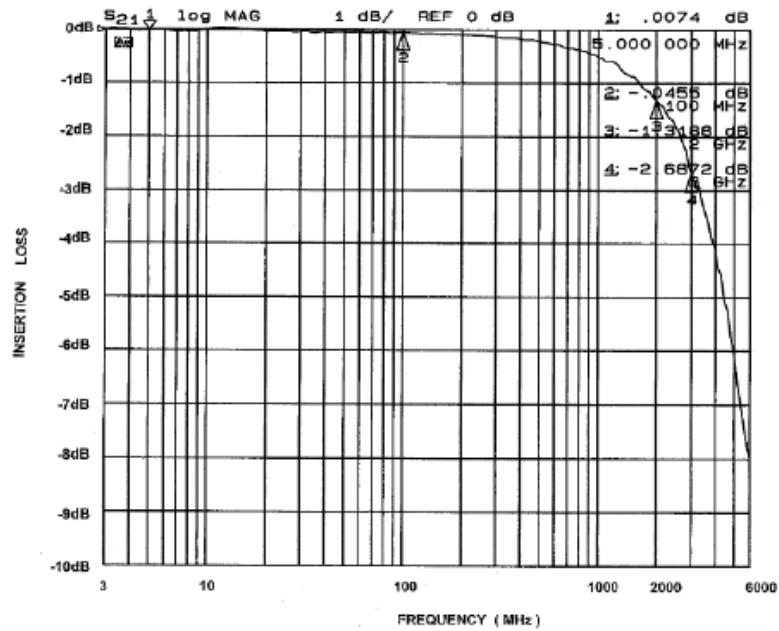


Figure 3. Channel 1 vs. All GND Pins (0 V DC Bias)

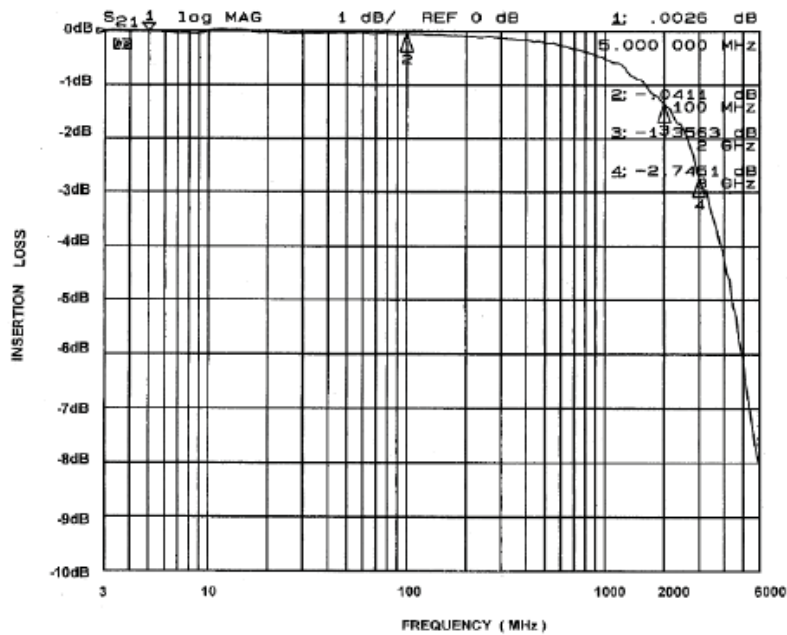


Figure 4. Channel 2 vs. All GND Pins (0 V DC Bias)

## PERFORMANCE INFORMATION (Cont'd)

## Typical Filter Performance for Low Voltage Pins

Nominal conditions unless specified; otherwise, 50  $\Omega$  environment.

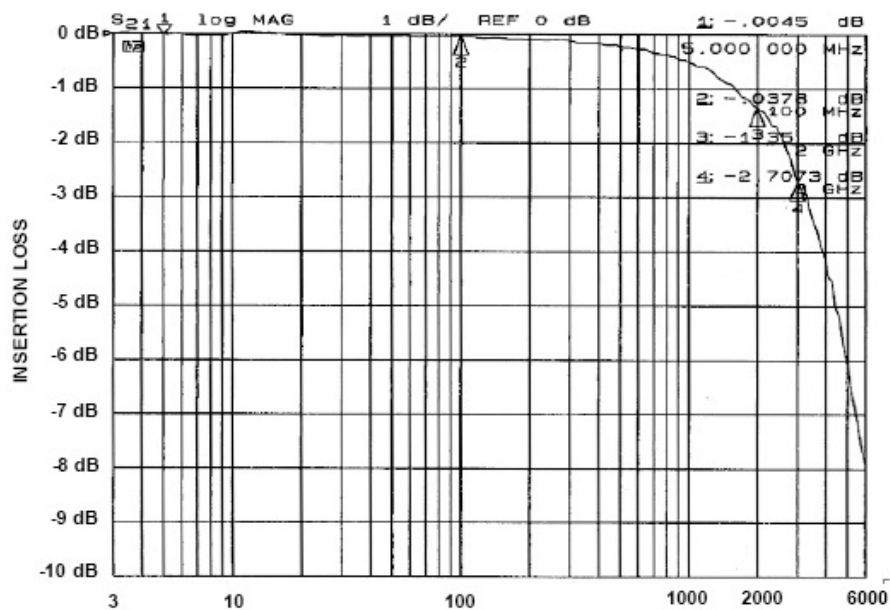
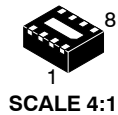
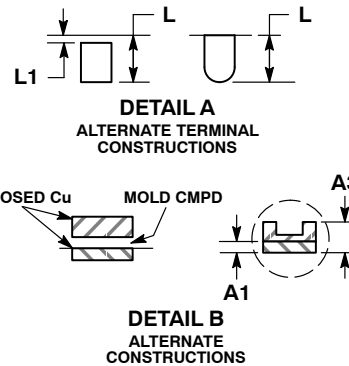
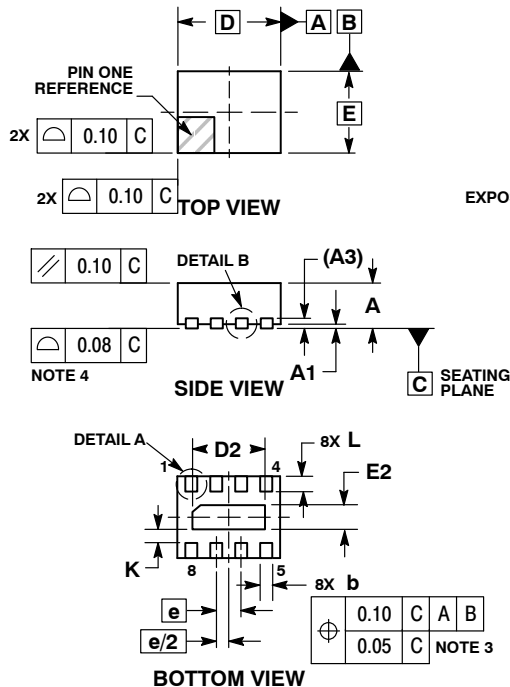


Figure 5. Channel 3 vs. All GND Pins (0 V DC Bias)

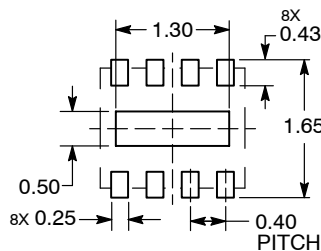

**WDFN8, 1.7x1.35, 0.4P**  
**CASE 511BF**  
**ISSUE O**

DATE 21 JUL 2010



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.70 | 0.80 |
| A1          | 0.00 | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.15 | 0.25 |
| D           | 1.7  | BSC  |
| E2          | 1.10 | 1.30 |
| E           | 1.35 | BSC  |
| E2          | 0.30 | 0.50 |
| e           | 0.40 | BSC  |
| K           | 0.22 | REF  |
| L           | 0.15 | 0.35 |
| L1          | ---  | 0.15 |

**RECOMMENDED SOLDERING FOOTPRINT\***


DIMENSION: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                              |                                                                                                                                                                                  |
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